

CMOS Delay-9 (H.0) Interconnect Delay

20170118

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References

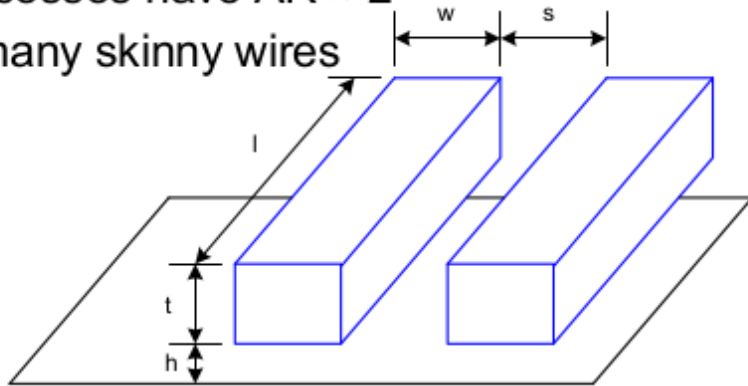
Some Figures from the following sites

[1] <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>
Weste & Harris Book Site

[2] en.wikipedia.org

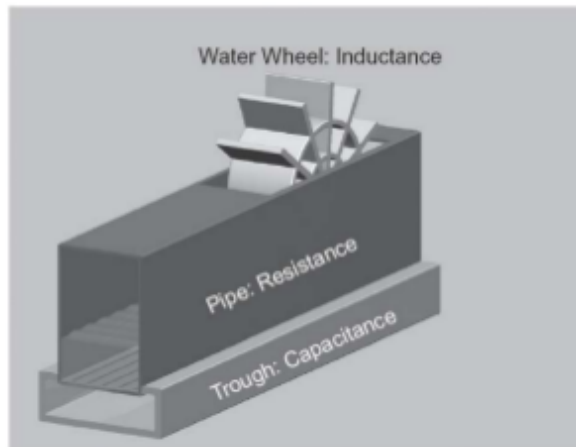
Wire Geometry

- ❑ Pitch = $w + s$
- ❑ Aspect ratio: $AR = t/w$
 - Old processes had $AR \ll 1$
 - Modern processes have $AR \approx 2$
 - Pack in many skinny wires



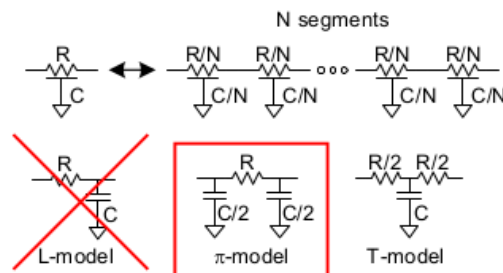
Interconnect Modeling

- Current in a wire is analogous to current in a pipe
 - Resistance: narrow size impedes flow
 - Capacitance: trough under the leaky pipe must fill first
 - Inductance: paddle wheel inertia opposes changes in flow rate
 - Negligible for most wires



Lumped Element Models

- ❑ Wires are a distributed system
 - Approximate with lumped element models



- ❑ 3-segment π -model is accurate to 3% in simulation
- ❑ L-model needs 100 segments for same accuracy!
- ❑ Use single segment π -model for Elmore delay

Wire Resistance

□ $\rho = \text{resistivity } (\Omega \cdot \text{m})$

$R =$

- $R_{\square} = \text{sheet resistance } (\Omega/\square)$
 - \square is a dimensionless unit(!)
- Count number of squares
 - $R = R_{\square} * (\# \text{ of squares})$

