CMOS Delay-9 (H.0) Interconnect Delay

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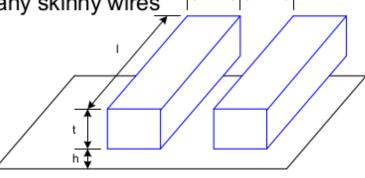
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References Some Figures from the following sites [1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html Weste & Harris Book Site [2] en.wikipedia.org

Wire Geometry

- ☐ Pitch = w + s
- ☐ Aspect ratio: AR = t/w
 - Old processes had AR << 1
 - Modern processes have AR ≈ 2

Pack in many skinny wires

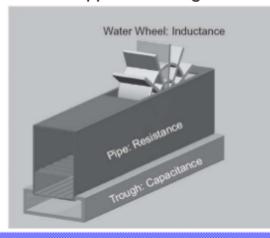


14: Wires

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Interconnect Modeling

- ☐ Current in a wire is analogous to current in a pipe
 - Resistance: narrow size impedes flow
 - Capacitance: trough under the leaky pipe must fill first
 - Inductance: paddle wheel inertia opposes changes in flow rate
 - Negligible for most wires



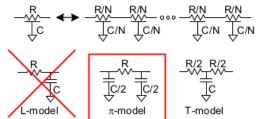
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Lumped Element Models

- ☐ Wires are a distributed system
 - Approximate with lumped element models

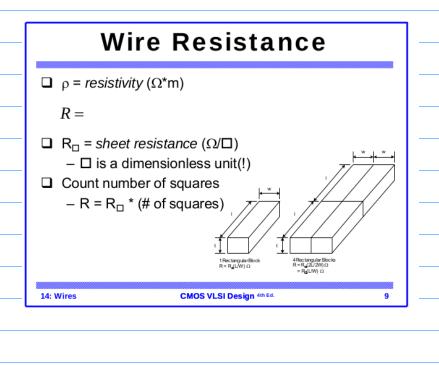
N segments



- \Box 3-segment π -model is accurate to 3% in simulation
- ☐ L-model needs 100 segments for same accuracy!
- $lue{}$ Use single segment π -model for Elmore delay

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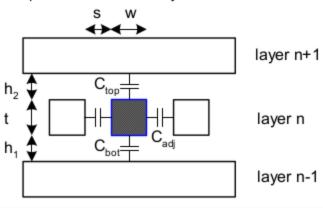
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Wire Capacitance

- Wire has capacitance per unit length
 - To neighbors
 - To layers above and below

$$\Box C_{total} = C_{top} + C_{bot} + 2C_{adj}$$



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Diffusion & Polysilicon

- Diffusion capacitance is very high (1-2 fF/μm)
 - Comparable to gate capacitance
 - Diffusion also has high resistance
 - Avoid using diffusion runners for wires!
- □ Polysilicon has lower C but high R
 - Use for transistor gates
 - Occasionally for very short wires between gates

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Wire RC Delay

Estimate the delay of a 10x inverter driving a 2x inverter at the end of the 1 mm wire. Assume wire capacitance is 0.2 fF/μm and that a unit-sized inverter has R = 10 KΩ and C = 0.1 fF.

$$- t_{od} = 800 \Omega$$

$$1000 \Omega \Rightarrow 1000 \text{ fF} 100 \text{ fF} 0.6 \text{ fF}$$
Driver Wire Load

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* A Step tapered wire
* A tree with sized segments
* Varieties of wiring trees
* Steiner Tree
* Wire Sizing