CMOS Delay-9 (H.0)
Interconnect Delay

20170120

References

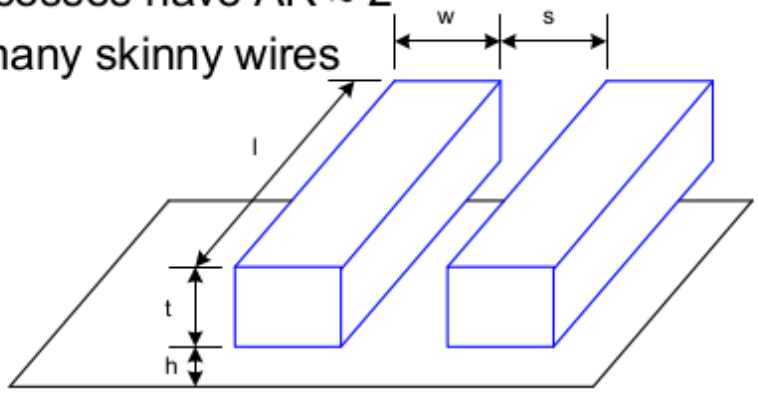
Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org

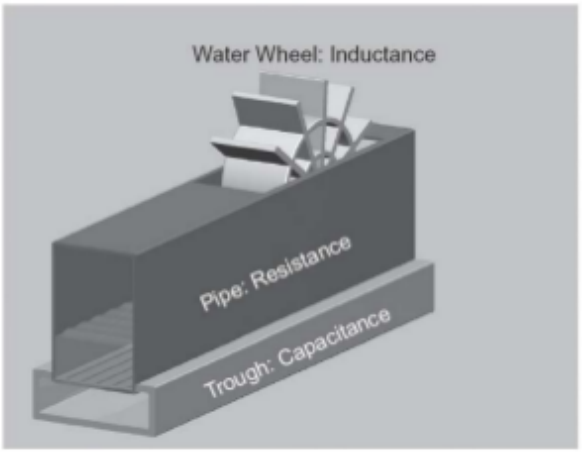
Wire Geometry

- Pitch = w + s
- Aspect ratio: AR = t/w
  - Old processes had AR << 1
  - Modern processes have AR ≈ 2
    - Pack in many skinny wires



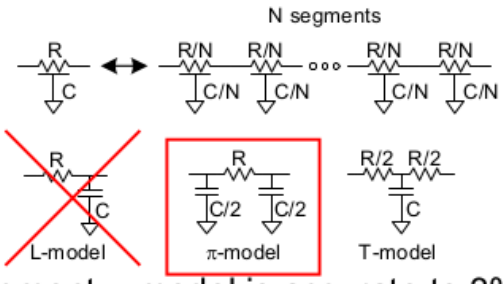
Interconnect Modeling

- Current in a wire is analogous to current in a pipe
  - Resistance: narrow size impedes flow
  - Capacitance: trough under the leaky pipe must fill first
  - Inductance: paddle wheel inertia opposes changes in flow rate
    - Negligible for most wires



Lumped Element Models

- Wires are a distributed system
  - Approximate with lumped element models



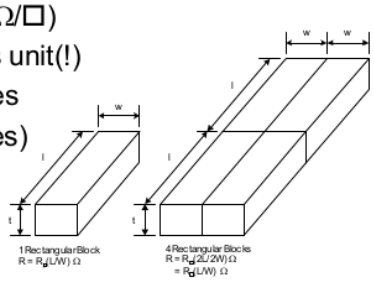
- 3-segment π-model is accurate to 3% in simulation
- L-model needs 100 segments for same accuracy!
- Use single segment π-model for Elmore delay

Wire Resistance

- ρ = *resistivity* (Ω*m)

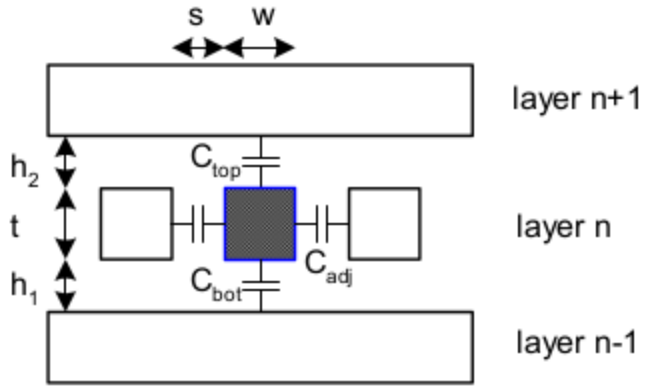
$$R =$$

- $R_{\square}$ = *sheet resistance* (Ω/□)
  - □ is a dimensionless unit(!)
- Count number of squares
  - $R = R_{\square}$ * (# of squares)



Wire Capacitance

- Wire has capacitance per unit length
  - To neighbors
  - To layers above and below
- $C_{total} = C_{top} + C_{bot} + 2C_{adj}$

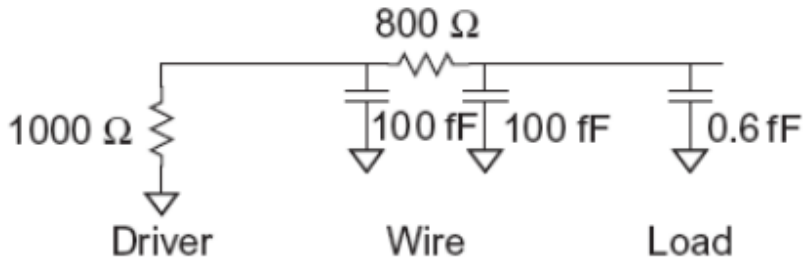


Diffusion & Polysilicon

- Diffusion capacitance is very high (1-2 fF/μm)
  - Comparable to gate capacitance
  - Diffusion also has high resistance
  - Avoid using diffusion *runners* for wires!
- Polysilicon has lower C but high R
  - Use for transistor gates
  - Occasionally for very short wires between gates

Wire RC Delay

- Estimate the delay of a 10x inverter driving a 2x inverter at the end of the 1 mm wire. Assume wire capacitance is 0.2 fF/μm and that a unit-sized inverter has R = 10 KΩ and C = 0.1 fF.
  - t_{pd} =



* A Step tapered wire

* A tree with sized segments

* Varieties of wiring trees

* Steiner Tree

* Wire Sizing