FPGA Implementation (1A)

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Based on

Implementation Steps

- Translate
- Map
- Place & Route
- Generate Program File

Implementation Steps

- Translate (.ngc → .ngd)
- Map (.ngd → .ncd)
- Place & Route (.ncd → .ncd)
- Generate Program File (.ncd → .bit)

Translate

- Translate Report
- Floor plan design
- Post-translation simulation model

Map

- Mapping report
- Post-mapping static timing
- Post-mapping floor plan design
- Post-mapping simulation model

Place and Route

- Place-and-route report
- Clock region report
- Asynchronous delay report
- Pad report

References

[1] ftp://ftp.geoinfo.tuwien.ac.at/navratil/HaskellTutorial.pdf
[2] https://www.umiacs.umd.edu/~hal/docs/daume02yaht.pdf