Timer / Counter Architecture

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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Based on

ARM System-on-Chip Architecture, 2nd ed, Steve Furber

Introduction to ARM Cortex-M Microcontrollers
– Embedded Systems, Jonathan W. Valvano

Digital Design and Computer Architecture,
D. M. Harris and S. L. Harris

ARM assembler in Raspberry Pi
Roger Ferrer Ibáñez

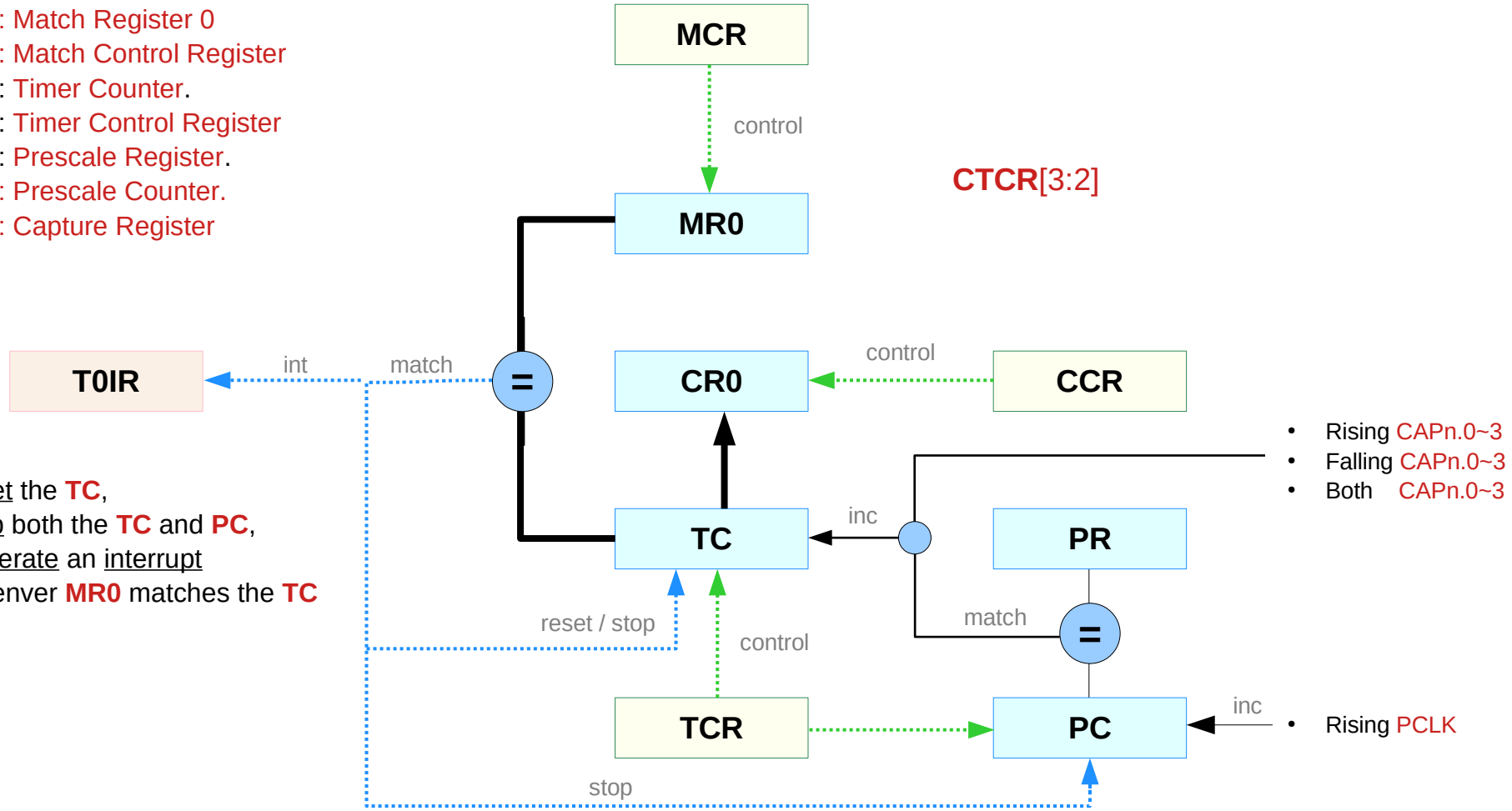
https://thinkingeek.com/arm-assembler-raspberry-pi/

NXP LPC214x Timers

http://www.ocfreaks.com/lpc2148-interrupt-tutorial/

Timer / Counter

MR0 : Match Register 0
MCR : Match Control Register
TC : Timer Counter.
TCR : Timer Control Register
PR : Prescale Register.
PC : Prescale Counter.
CR : Capture Register



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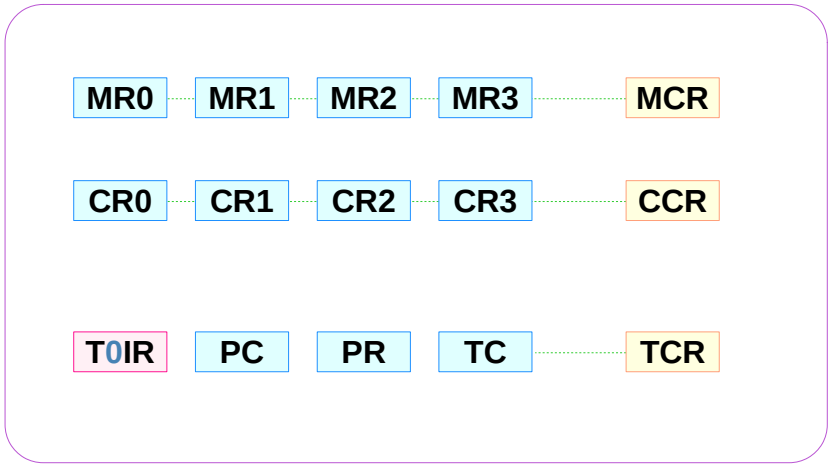
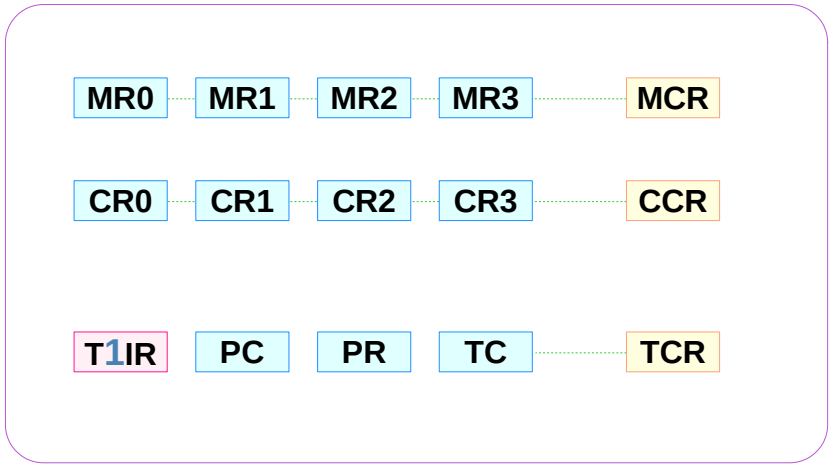
Registers in each timer

TIMER**0**



MR0,1,2,3 : Match Registers
CR0,1,2,3 : Capture Register
MCR : Match Control Register
TC : Timer Counter
TCR : Timer Control Register
PR : Prescale Register
PC : Prescale Counter
T0IR : Interrupt Register

TIMER**1**



MR0,1,2,3 : Match Registers
CR0,1,2,3 : Capture Register
MCR : Match Control Register
TC : Timer Counter
TCR : Timer Control Register
PR : Prescale Register
PC : Prescale Counter
T1IR : Interrupt Register

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Interrupt Register (IR)

The **IR** can be read to identify which of
8 possible interrupt sources are pending.

The **IR** can be written to clear interrupts.

TIMER/ COUNTER0	**T0IR**
TIMER/ COUNTER1	**T1IR**

The Interrupt Register consists of
four bits for the match interrupts and
four bits for the capture interrupts.

If an interrupt is generated
then the corresponding bit in the **IR** will be high.
Otherwise, the bit will be low.

Writing a logic one to the corresponding IR bit
will reset the interrupt.
Writing a zero has no effect

Bit 0	: MR0 Interrupt	flag for match channel 0
Bit 1	: MR1 Interrupt	flag for match channel 1
Bit 2	: MR2 Interrupt	flag for match channel 2
Bit 3	: MR3 Interrupt	flag for match channel 3
Bit 4	: CR0 Interrupt	flag for capture channel 0 event
Bit 5	: CR1 Interrupt	flag for capture channel 1 event
Bit 6	: CR2 Interrupt	flag for capture channel 2 event
Bit 7	: CR3 Interrupt	flag for capture channel 3 event

A high bit signifies the interrupt is generated

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Match Registers : MR0 ~ MR3

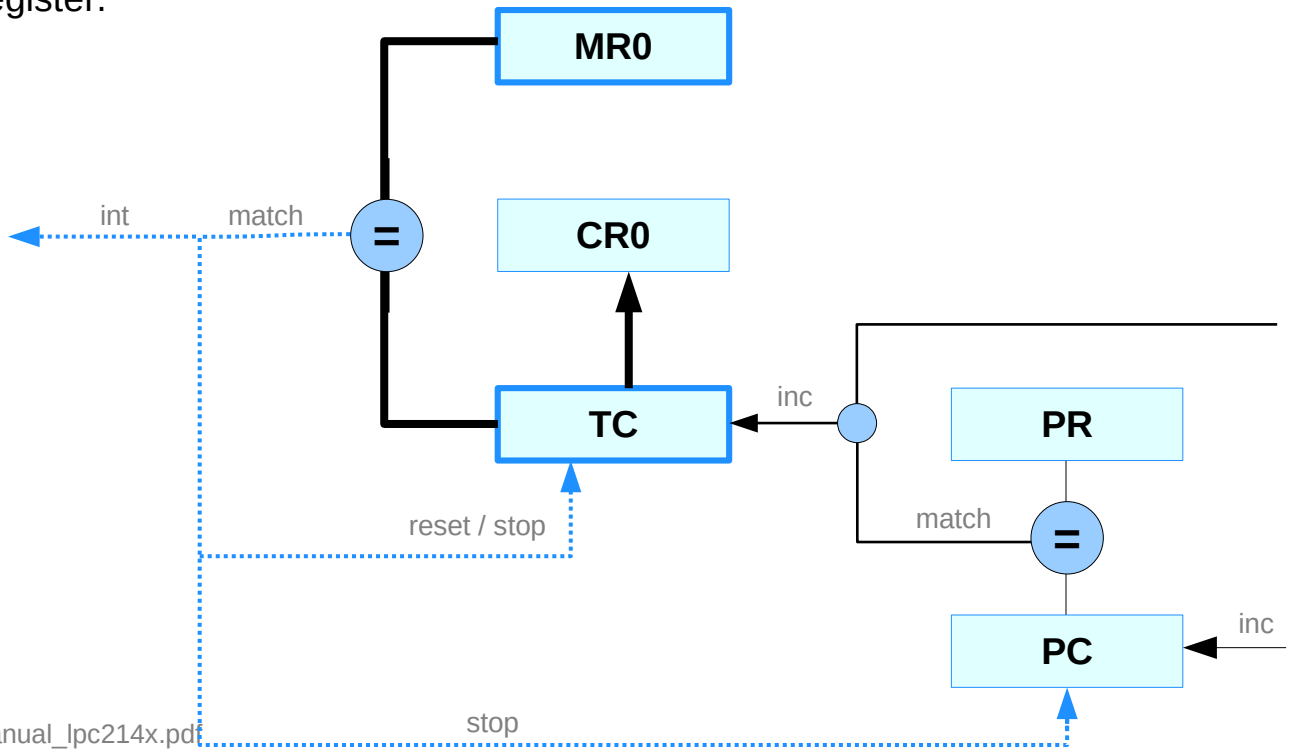
The Match register values are
continuously compared
to the Timer Counter value.

When the two values are equal,
actions can be triggered automatically.

Actions are controlled by the **MCR** register.

The possible actions are to
generate an interrupt,
reset the Timer Counter,
or stop the timer.

MR0 (Match Register 0)
can be enabled through the **MCR**
to reset the **TC**,
stop both the **TC** and **PC**,
and/or generate an interrupt
whenver **MR0** matches the **TC**



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Match Control Register (MCR)

"n" represents the Timer number, 0 or 1.

Interrupt on MR0: MR0I = 1
an interrupt is generated
when MR0 matches the value in the **TC**

Reset on MR0: MR0R = 1
the **TC** will be reset if MR0 *matches* it.

Stop on MR0: MR0S = 1
the **TC** and **PC** will be stopped and
TCR[0] will be set to 0 if MR0 matches the TC

MCR[0]:	MR0I
MCR[1]:	MR0R
MCR[2]:	MR0S
MCR[3]:	MR1I
MCR[4]:	MR1R
MCR[5]:	MR1S
MCR[6]:	MR2I
MCR[7]:	MR2R
MCR[8]:	MR2S
MCR[9]:	MR3I
MCR[10]:	MR3R
MCR[11]:	MR3S

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TC, PR, PC

TC : Timer Counter.

The 32-bit **TC** is incremented
every **PR+1** cycles of **PCLK**.

The **TC** is controlled through the **TCR**

PR : Prescale Register.

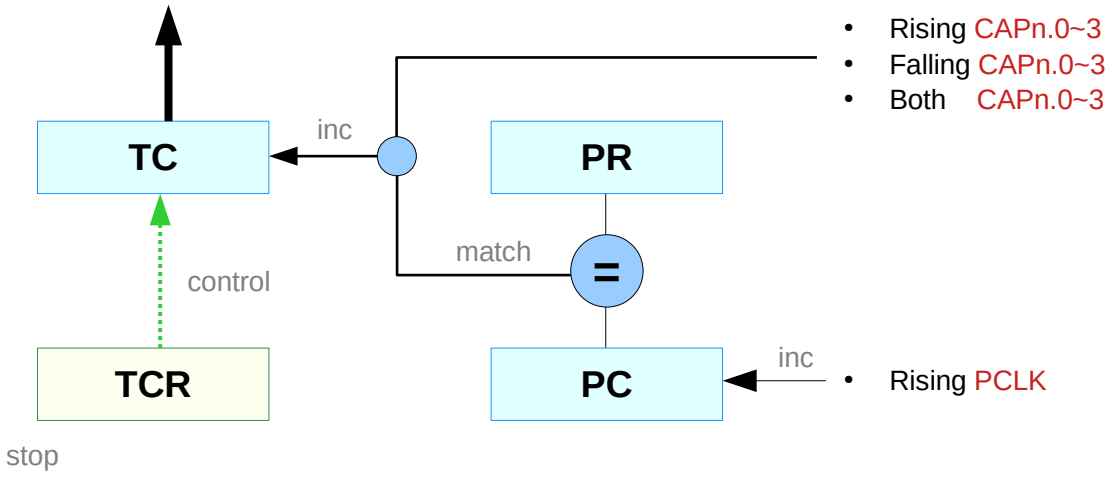
The Prescale Counter is equal to this value,
the next clock increments the **TC**
and clears the **PC**

PC : Prescale Counter.

The 32-bit **PC** is a counter
which is incremented to the value stored in **PR**.

When the value in **PR** is reached,
the **TC** is incremented and the **PC** is cleared.

The **PC** is observable and controllable
through the bus interface



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Timer Control Register (TCR)

TCR[0] : Counter Enable

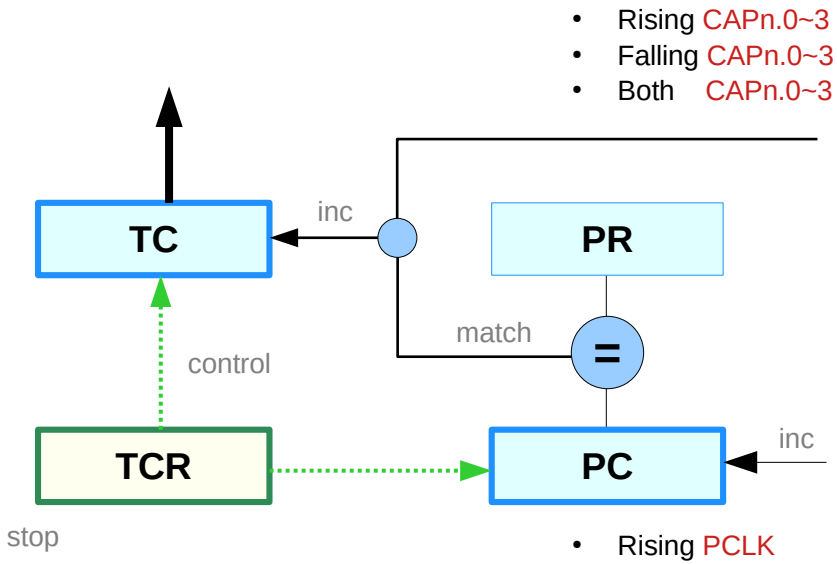
When one, the Timer Counter (**TC**) and
Prescale Counter (**PC**) are enabled for counting.
When zero, the counters are disabled.

TCR[1] : Counter Reset

When one, the Timer Counter (**TC**) and
Prescale Counter (**PC**) are are synchronously reset
on the next positive edge of **PCLK**.
The counters remain reset
until TCR[1] is returned to zero.

TCR[7:2] : Reserved,

user software should not write ones to reserved bits.
The value read from a reserved bit is not defined.



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Capture Register

Each capture register is associated with a device pin and may be loaded with the **Timer Counter** value when a specified event occurs on that pin.

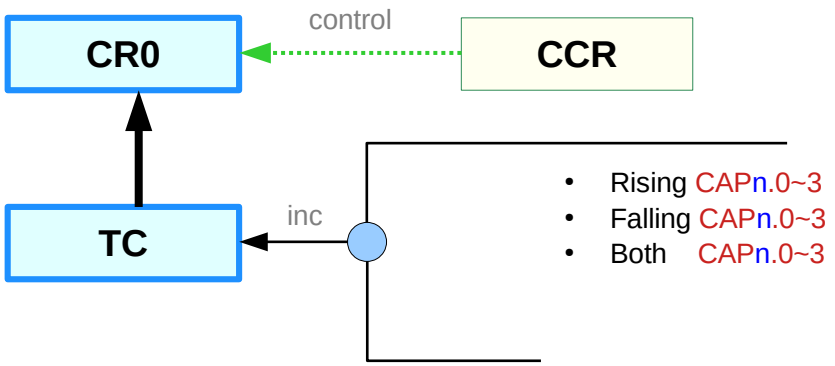
The settings in the Capture Control Register register determine whether the capture function is enabled, and whether a capture event happens on the rising edge of the associated pin, the falling edge, or on both edges.

CR0: Capture Register 0.

CR0 is loaded with the value of **TC** when there is an event on the **CAPn.0**

CAP0.0 for **TIMER0**
CAP1.0 for **TIMER1**, respectively

TIMER**0**		
	Match	MR0, MR1, MR2, MR3
	Capture	**CR0, CR1, CR2, CR3**
TIMER**1**		
	Match	MR0, MR1, MR2, MR3
	Capture	**CR0, CR1, CR2, CR3**



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Capture Control Register (CCR)

The **Capture Control Register** is used to control

whether one of the four **Capture Registers** is loaded with the value in the **Timer Counter** when the capture event occurs

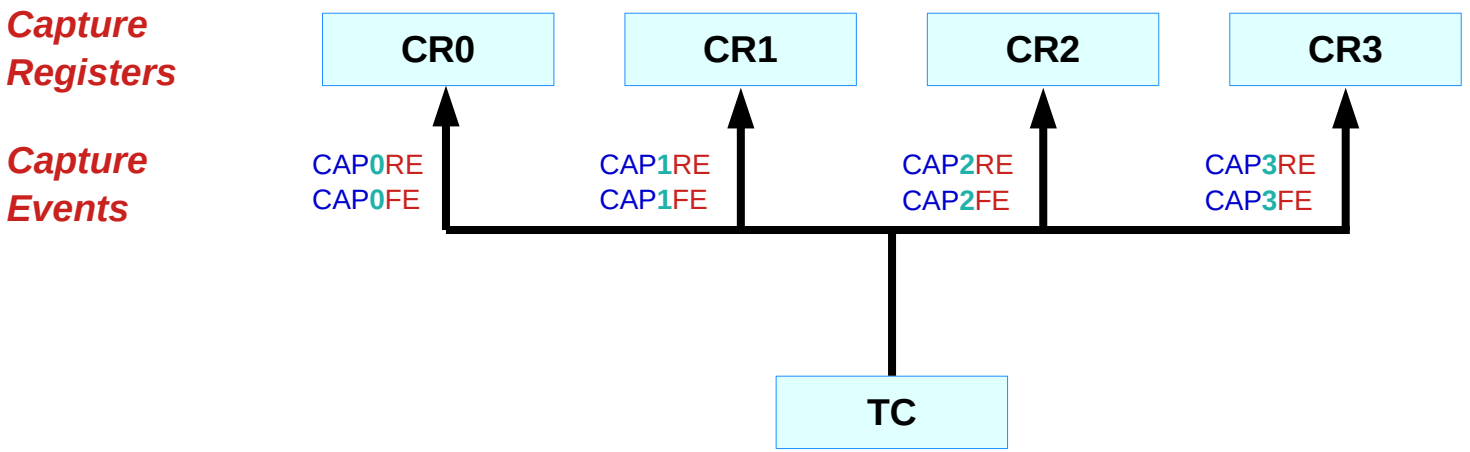
CR0, **CR1**, **CR2**, **CR3**

whether an **interrupt** is generated by the capture event.

RE, FE

I

Setting both the rising and falling bits at the same time is a valid configuration, resulting in a capture event for both edges.



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4 capture channels per timer

Up to four 32-bit capture channels per timer,
that can take a snapshot of the timer value
when an input signal transitions.

A capture event may also optionally generate an interrupt

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Capture Control Register (CCR)

"n" represents the Timer number, 0 or 1.

Capture on CAPn.0 rising edge: CAP0RE
a sequence of 0 then 1 on CAPn.0 will cause **CR0** to be loaded with the contents of **TC**.

Capture on CAPn.0 falling edge: CAP0FE
a sequence of 1 then 0 on CAPn.0 will cause **CR0** to be loaded with the contents of **TC**.

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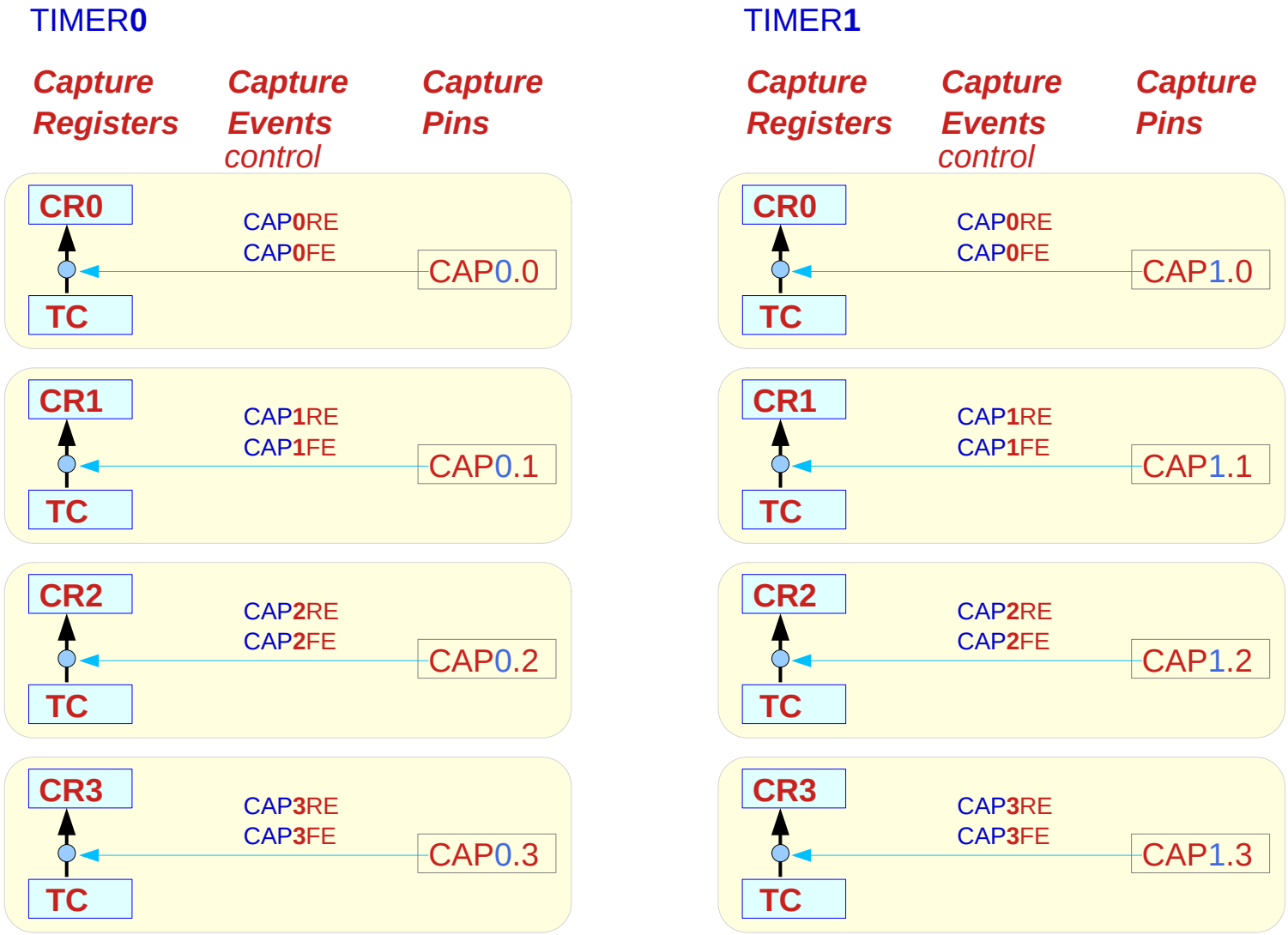
Capture Events



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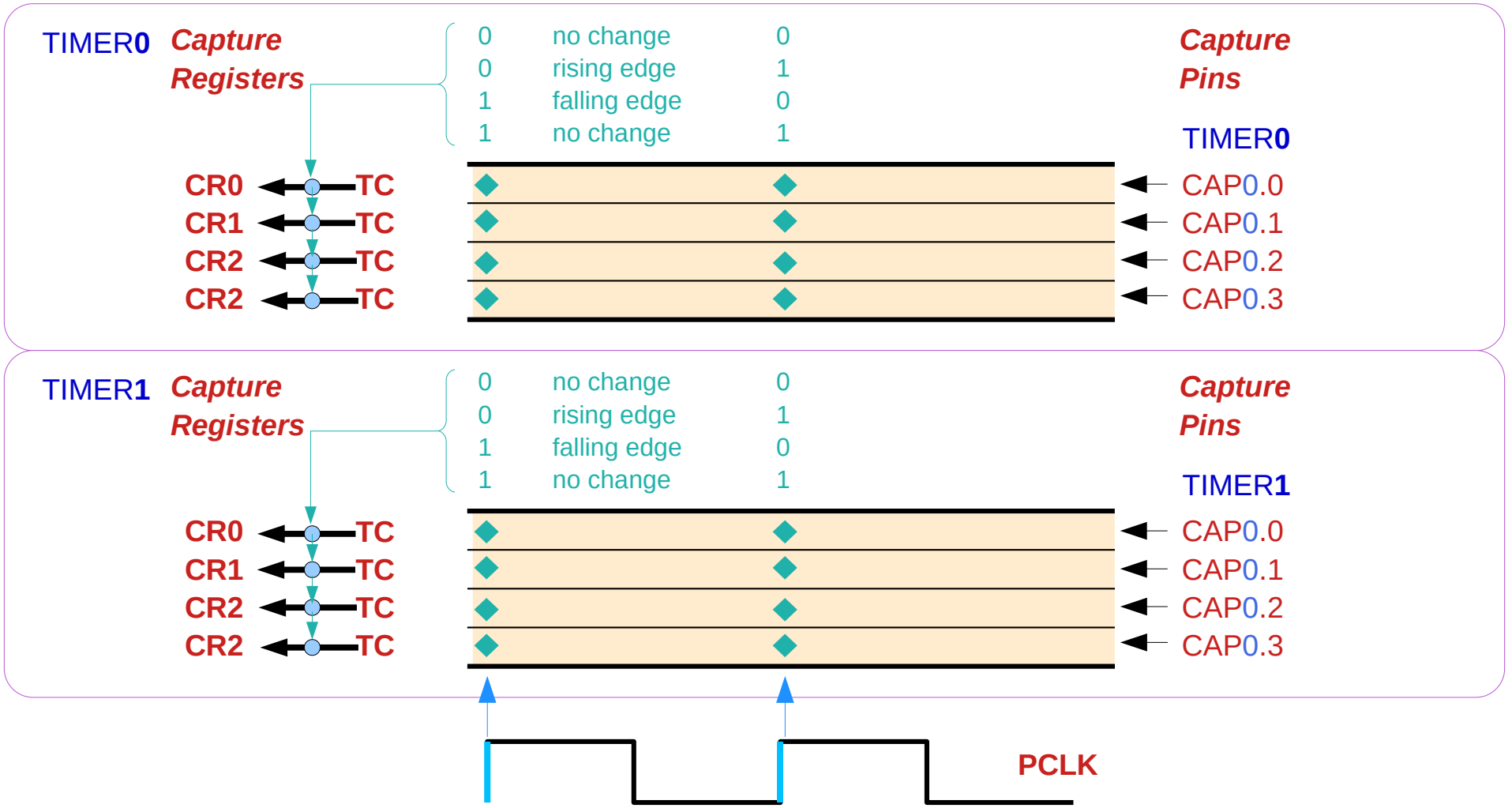
Four capture channels for each timer



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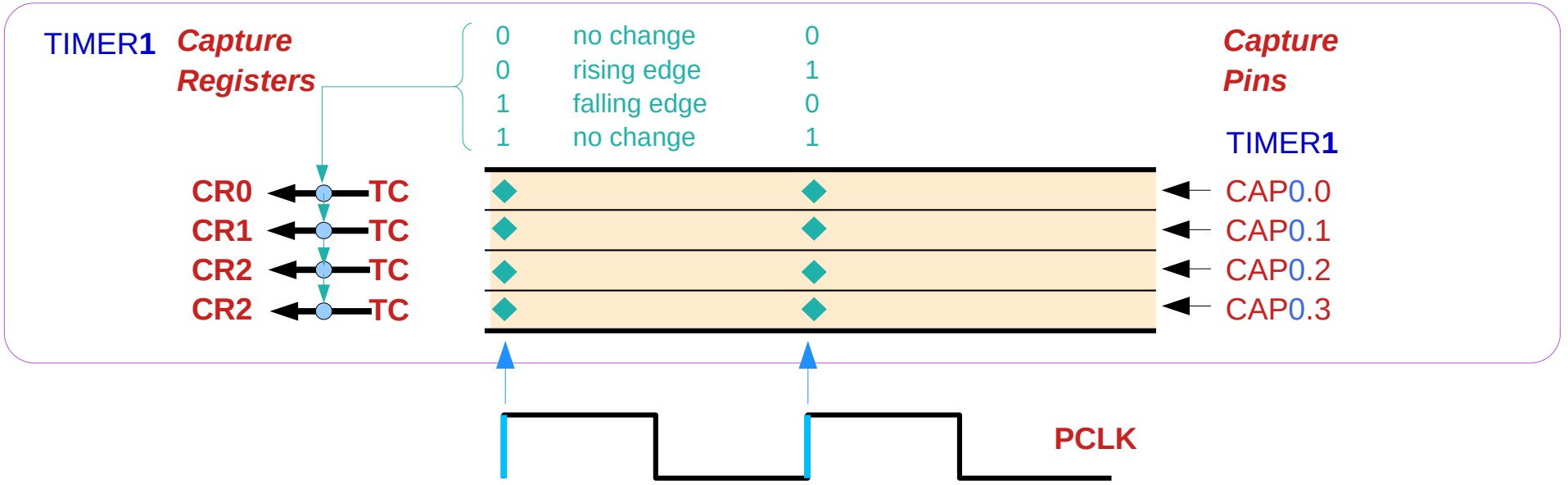
Capture Events

capture register	capture event enabled	capture pins	
		CAP0.0	CAP1.0
CR0	CAP0RE	CAP0.0	CAP1.0
	CAP0FE	CAP0.0	CAP1.0
	CAP0RE & CAP0FE	CAP0.1	CAP1.1
CR1	CAP1RE	CAP0.1	CAP1.1
	CAP1FE	CAP0.1	CAP1.1
	CAP1RE & CAP0FE	CAP0.2	CAP1.2
CR2	CAP2RE	CAP0.2	CAP1.2
	CAP2FE	CAP0.2	CAP1.2
	CAP2RE & CAP0FE	CAP0.3	CAP1.3
CR3	CAP3RE	CAP0.3	CAP1.3
	CAP3FE	CAP0.3	CAP1.3
	CAP3RE & CAP0FE		
TIMER0, or 1	TIMER0, or 1	TIMER0	TIMER1



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Capture Control Register (CCR)

"n" represents the Timer number, 0 or 1.

Capture on CAPn.0 rising edge: CAP0RE = 1
a sequence of 0 then 1 on CAPn.0
will cause **CR0** to be loaded
with the contents of **TC**.

Capture on CAPn.0 falling edge: CAP0FE = 1
a sequence of 1 then 0 on CAPn.0
will cause **CR0** to be loaded
with the contents of **TC**

Interrupt on CAPn.0 event: CAP0I = 1
a **CR0** load due to a CAPn.0 event
will generate an interrupt.

CCR[0]:	CAP**0**RE
CCR[1]:	CAP**0**FE
CCR[2]:	CAP**0**I
CCR[3]:	CAP**1**RE
CCR[4]:	CAP**1**FE
CCR[5]:	CAP**1**I
CCR[6]:	CAP**2**RE
CCR[7]:	CAP**2**FE
CCR[8]:	CAP**2**I
CCR[9]:	CAP**3**RE
CCR[10]:	CAP**3**FE
CCR[11]:	CAP**3**I

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Timer / Counter Capture Pins (1)

Capture Signals -
A transition on a capture pin can be configured
to load one of the Capture Registers
with the value in the Timer Counter
and optionally to generate an interrupt.

Capture functionality can be selected
from a number of pins.
(*physically more than one pin can exist*)

- CAP0.0 (3 pins)
- CAP0.1 (2 pins)
- CAP0.2 (3 pin)
- CAP0.3 (1 pin)

- CAP1.0 (1 pin)
- CAP1.1 (1 pin)
- CAP1.2 (2 pins)
- CAP1.3 (2 pins)

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Timer / Counter Capture Pins (2)

When more than one pin is selected
for a Capture input on a single TIMER0/1 channel,
the pin with the lowest Port number is used. only one pin is used per channel

If for example pins 30 (P0.6) and 46 (P0.16) are selected for CAP0.2,
only pin 30 will be used by TIMER0 to perform CAP0.2 function.

Here is the list of all CAPTURE signals,
together with pins on where they can be selected:

- CAP0.0 (3 pins) : P0.2, P0.22 and P0.30
- CAP0.1 (2 pins) : P0.4 and P0.27
- CAP0.2 (3 pin) : P0.6, P0.16 and P0.28
- CAP0.3 (1 pin) : P0.29

- CAP1.0 (1 pin) : P0.10
- CAP1.1 (1 pin) : P0.11
- CAP1.2 (2 pins) : P0.17 and P0.19
- CAP1.3 (2 pins) : P0.18 and P0.21

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Timer mode and Counter mode

Timer Mode

PC is incremented on rising **PCLK**

Counter Mode

TC is incremented on rising, falling, both edges on the **CAP** input

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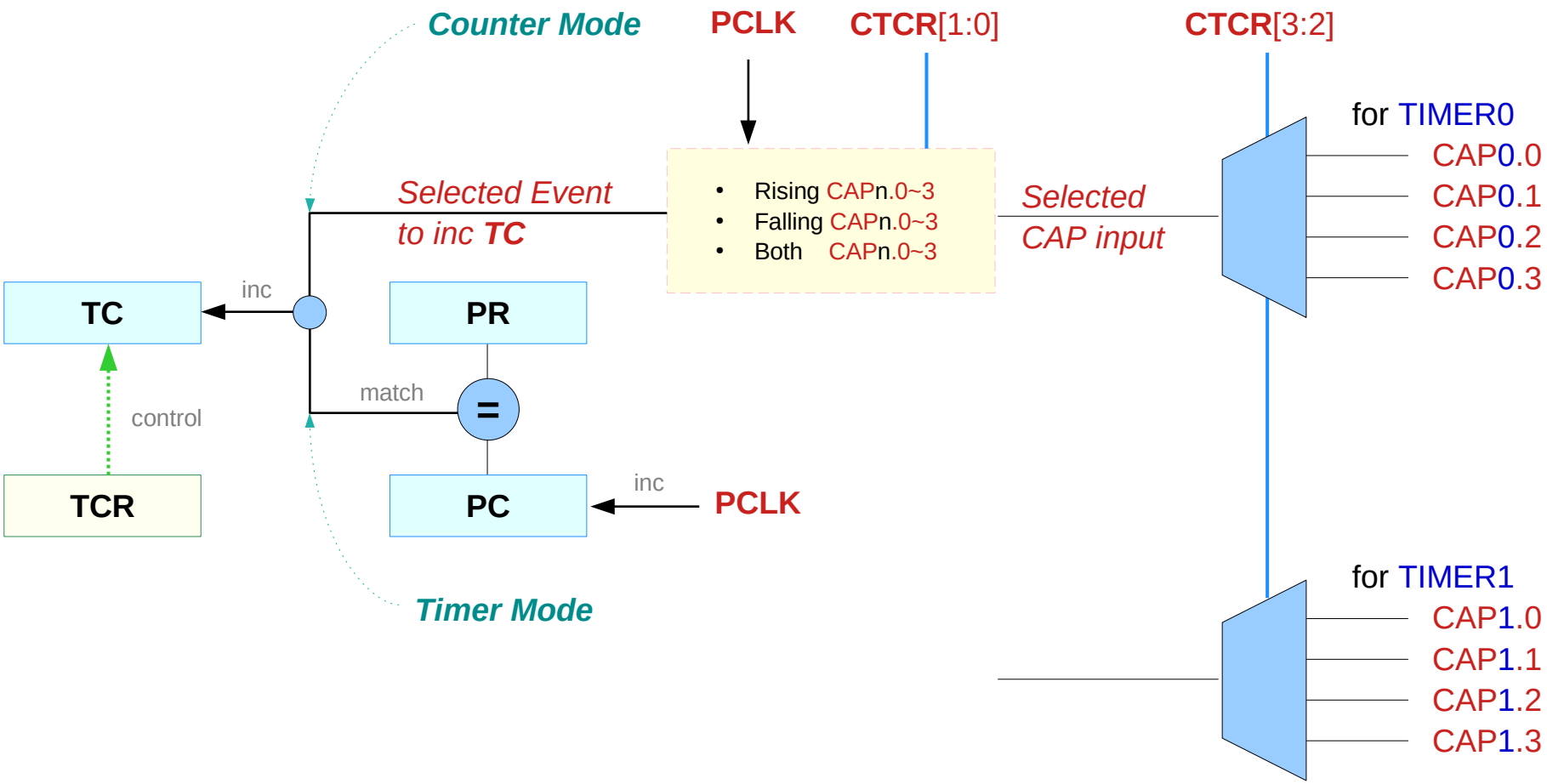
Timer / Counter Capture Pins



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CounTer Control Register (CTCR)

The **Count Control Register** (**CTCR**) is used

1) to select between Timer and Counter mode

2) to select the pin (Bits 3:2)
and edge(s) (Bits 1:0) for counting
in Counter mode

Bits 1:0 Counter / Timer Mode

00	Timer mode,	rising PCLK
01	Counter mode,	rising CAP input
10	Counter mode,	falling CAP input
11	Counter mode,	both CAP input

Bits 3:2 Count Input Select

00	CAPn.0
01	CAPn.1
10	CAPn.2
11	CAPn.3

for TIMER0	for TIMER1
CAP0.0	CAP1.0
CAP0.1	CAP1.1
CAP0.2	CAP1.2
CAP0.3	CAP1.3

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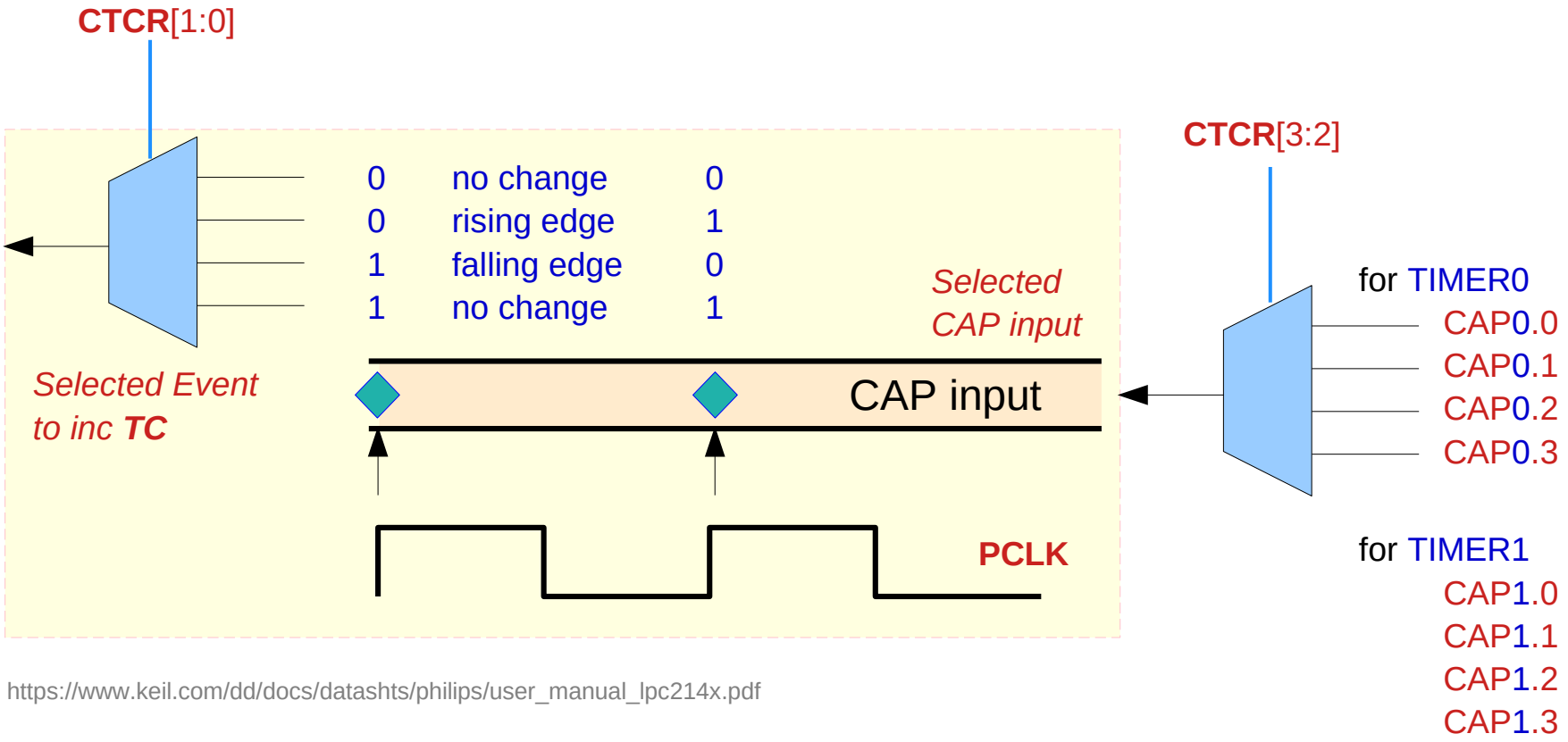
CounTer Control Register (CTCR)

When Counter Mode is chosen, (CTCR[1:0] = 01,10,11)
the CAP input (selected by the CTCR[3:2])
is sampled on every rising edge of the **PCLK** clock.

After comparing two consecutive samples of
this CAP input, one of the following four events
is recognized:
rising edge, falling edge,
either of edges or no changes
in the level of the selected CAP input.



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CounTer Control Register (CTCR)

Only if the identified event corresponds
to the one selected by bits 1:0 in the **CTCR** register,
the **Timer Counter** register will be incremented

Bits 1:0	Counter / Timer Mode	
00	Timer mode,	rising PCLK
01	Counter mode,	rising CAP input
10	Counter mode,	falling CAP input
11	Counter mode,	both CAP input

Bits 3:2	Count Input Select
00	CAPn.0
01	CAPn.1
10	CAPn.2
11	CAPn.3

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CTCR – Counter / Timer Mode

Bits	Mode	This field selects which
1:0	Timer / Counter	rising **PCLK** edges can increment Timer's Prescale Counter (**PC**), or clear **PC** and increment Timer Counter (**TC**).

00	Timer Mode	every rising **PCLK** edge
01	Counter Mode	**TC** is incremented on rising edges on the **CAP** input selected by bits 3:2.
10	Counter Mode	**TC** is incremented on falling edges on the **CAP** input selected by bits 3:2.
11	Counter Mode	**TC** is incremented on both edges on the **CAP** input selected by bits 3:2

Timer Mode	**PC** is incremented on rising **PCLK**
Counter Mode	**TC** is incremented on rising, falling, both edges on the **CAP** input

- Rising PCLK
- Rising CAPn.0~3
- Falling CAPn.0~3
- Both CAPn.0~3

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CTCR – CAP Select

Bits	Select	When bits 1:0 in this register are not 00 (Timer Mode),
3:2	Counter Input	these bits select which CAP pin is sampled for clocking:
00	CAPn.0	CAP0.0 for TIMER0 and CAP1.0 for TIMER1
01	CAPn.1	CAP0.1 for TIMER0 and CAP1.1 for TIMER1
10	CAPn.2	CAP0.2 for TIMER0 and CAP1.2 for TIMER1
11	CAPn.3	CAP0.3 for TIMER0 and CAP1.3 for TIMER1

Note: If Counter mode is selected for a particular CAPn input in the TnCTCR,
the 3 bits for that input in the Capture Control Register (TnCCR)
must be programmed as 000.

However, capture and/or interrupt can be selected
for the other 3 CAPn inputs in the same timer.

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U0IIR

The **U0IIR** provides a status code that denotes
the priority and source of a pending interrupt

the interrupts are frozen during an **U0IIR** access.

if an interrupt occurs during an **U0IIR** access,
the interrupt is recorded for the next **U0IIR** access

given the status of U0IIR[3:0],
an interrupt handler routine can determine
the cause of the interrupt and
how to clear the active interrupt.

The **U0IIR** must be read
in order to clear the interrupt prior to exiting the ISR

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References

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[2] http://blog.bobuhiro11.net/2014/01-13-baremetal.html
[3] http://www.valvers.com/open-software/raspberry-pi/
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