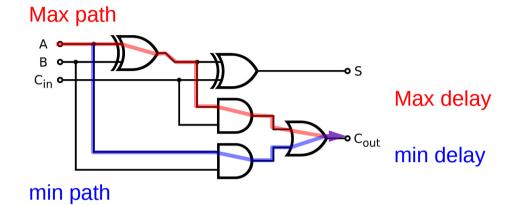
# Path Delay

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Please send corrections (or suggestions) to youngwlim@hotmail.com.
This document was produced by using OpenOffice and Octave.

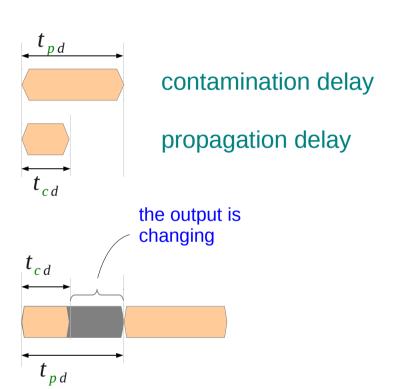
### Path Delay

Max-Path
Min-Path
Critical Path
Timing Check
False Path
Multi-Cycle Path

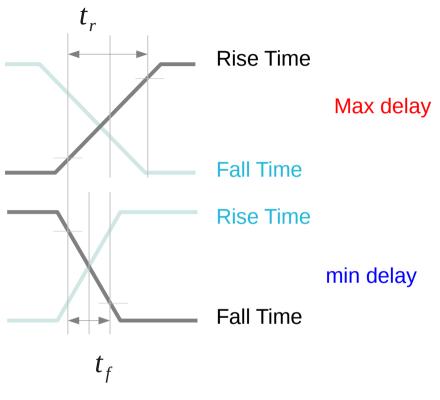
### Max Path / Min Path



$$t_{cd} \leq t_{delay} \leq t_{pd}$$
 min delay Max delay

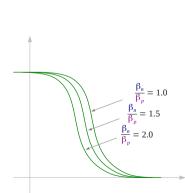


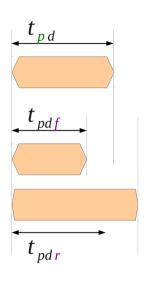
### Rise / Fall Times

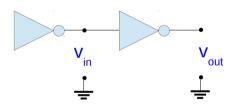


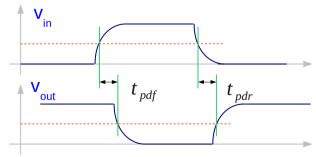
$$\frac{\beta_n}{\beta_p} > 1 \qquad \frac{R_n}{R_p} < 1$$

$$\frac{t_f}{t_r} = \frac{2.2 \,\tau_n}{2.2 \,\tau_p} \qquad \frac{\tau_n}{\tau_p} = \frac{R_n C_{out}}{R_p C_{out}} = \frac{R_n}{R_p} < 1$$









### **PVT Variation**

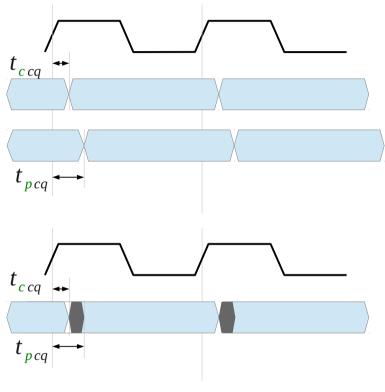
Process

Voltage

Temperature

High temperature Max delay
Low temperature min delay

### FF Output Delay



contamination delay

propagation delay

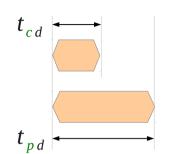
flipflop clock-to-q

$$t_{ccq} \leq t_{delay} \leq t_{pcq}$$

min delay

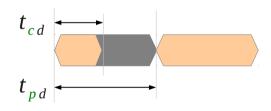
Max delay

## Path Delay



contamination delay

propagation delay



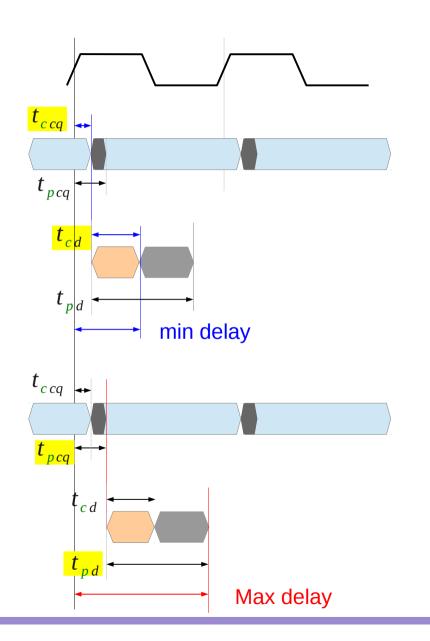
combinational logic delay

$$t_{cd} \leq t_{delay} \leq t_{pd}$$

min delay

Max delay

### Reg-to-Reg Delay (1)



$$t_{ccq} \leq t_{FF} \leq t_{pcq}$$

min delay

Max delay

$$t_{cd} \leq t_{comb} \leq t_{pd}$$

min delay

Max delay

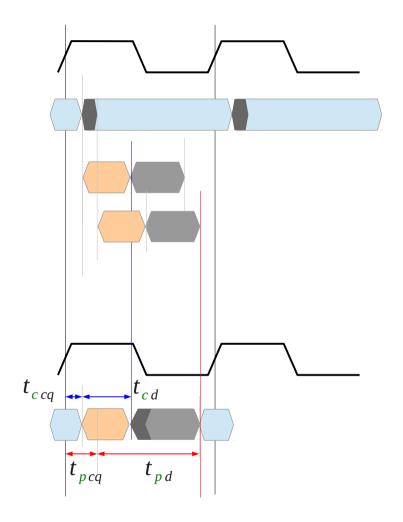
$$t_{ccq} + t_{cd} \le t_{delay} \le t_{pcq} + t_{pd}$$

min delay

Max delay

9

### Reg-to-Reg Delay (2)



$$t_{ccq} \leq t_{FF} \leq t_{pcq}$$

min delay

Max delay

$$t_{cd} \leq t_{comb} \leq t_{pd}$$

min delay

Max delay

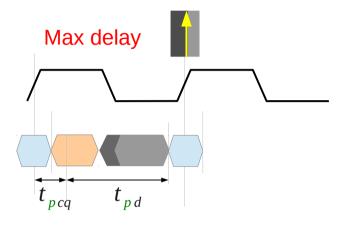
$$t_{ccq} + t_{cd} \le t_{delay} \le t_{pcq} + t_{pd}$$

min delay

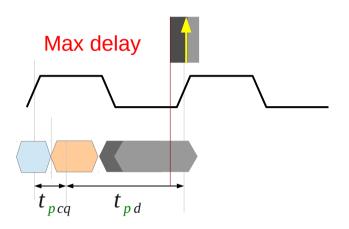
Max delay

### Setup Time / Hold Time

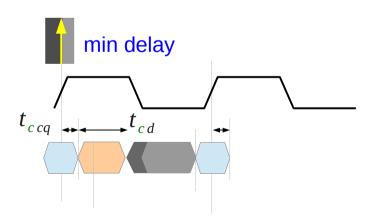
#### **Setup Time OK**



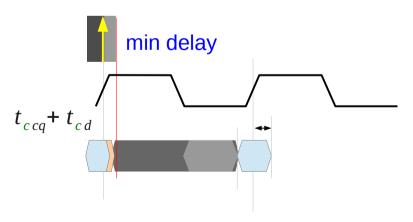
### **Setup Time Violation**



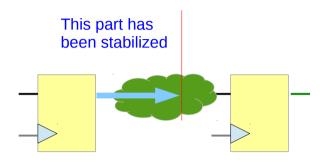
#### **Hold Time OK**

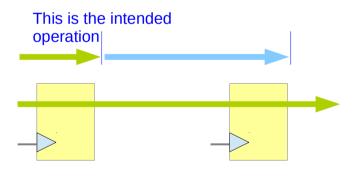


#### **Hold Time Violation**



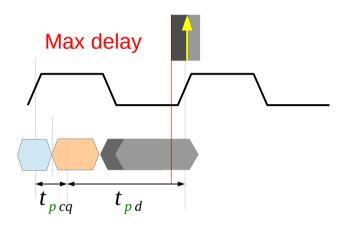
## Setup Time / Hold Time



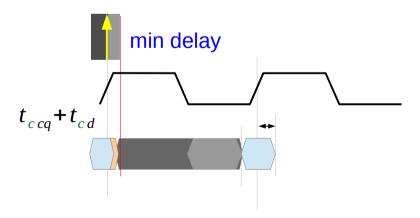


Since the delay is too small signal passes through the 2nd FF

### **Setup Time Violation**



#### **Hold Time Violation**



### False Path

# Multi-Cycle Path

#### References

- [1] http://en.wikipedia.org/
- [2] http://www.allaboutcircuits.com/
- [3] W. Wolf, "Modern VLSI Design: Systems on Silicon
- [4] N. Weste, D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective"
- [5] J. P. Uyemura, "Introduction to VLSI Circuits and Systems"
- [6] https://en.wikiversity.org/wiki/The\_necessities\_in\_SOC\_Design
- [7] https://en.wikiversity.org/wiki/The\_necessities\_in\_Digital\_Design
- [8] https://en.wikiversity.org/wiki/The\_necessities\_in\_Computer\_Design
- [9] https://en.wikiversity.org/wiki/The\_necessities\_in\_Computer\_Architecture
- [10] https://en.wikiversity.org/wiki/The\_necessities\_in\_Computer\_Organization