

CMOS Sequential Circuits (H.1)

20151215

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References

Some Figures from the following sites

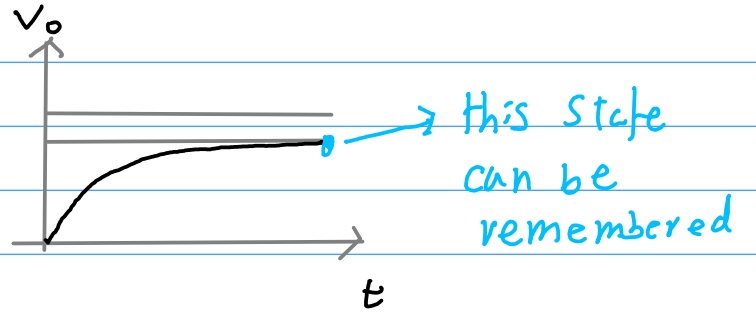
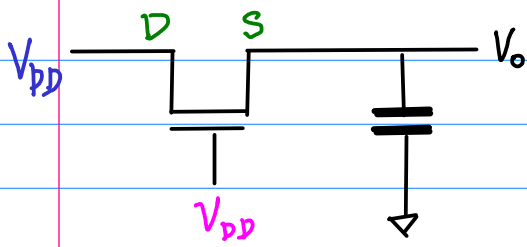
[1] <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>
Weste & Harris Book Site

[2] en.wikipedia.org

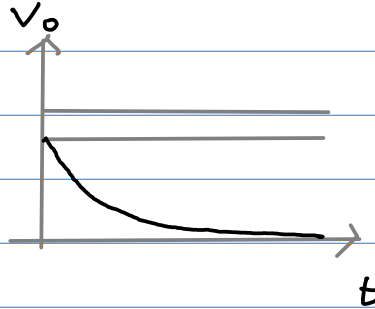
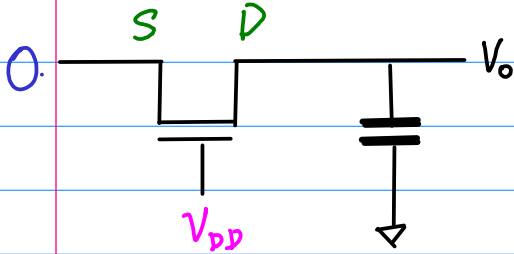
[3] Digital Integrated Circuits : A Design Perspective,
Jan M. Rabaey,
(<http://bwracs.eecs.berkeley.edu/Classes/lcBook/>)

[4] Digital Electronics and Design with VHDL
Pedroni

Charge

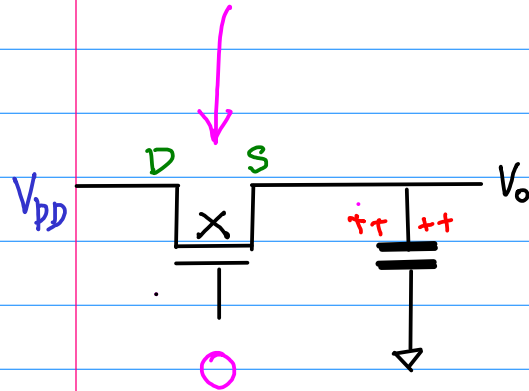
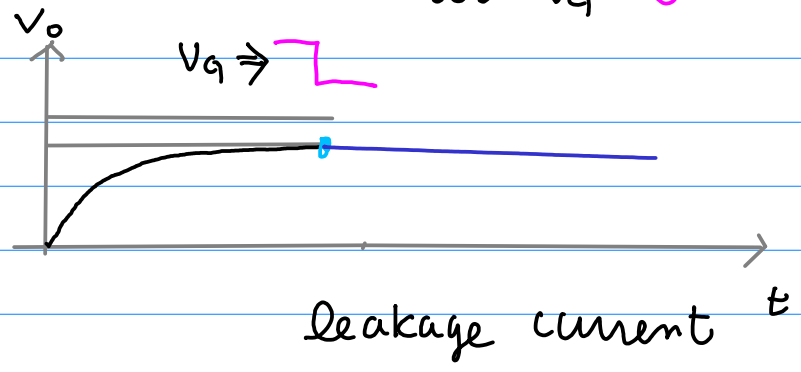
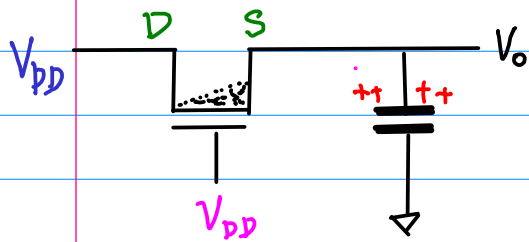


Discharge



Charge

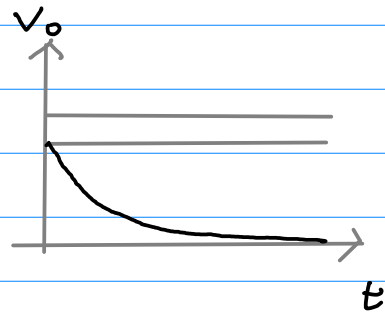
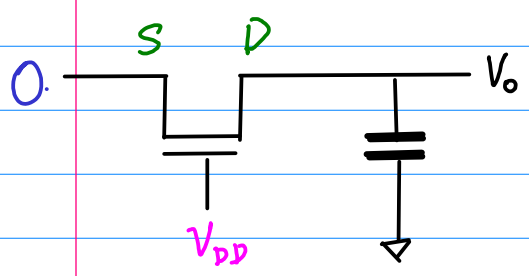
this state
can be
remembered
after $V_G = 0$



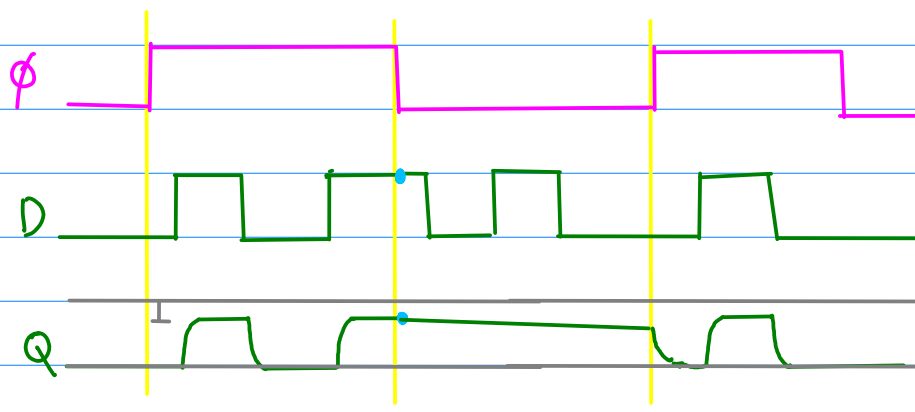
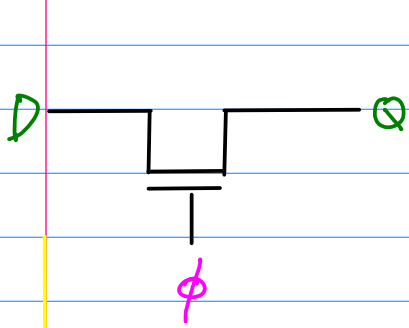
cut off
High Impedance

p-n junction
reverse-biased

Discharge

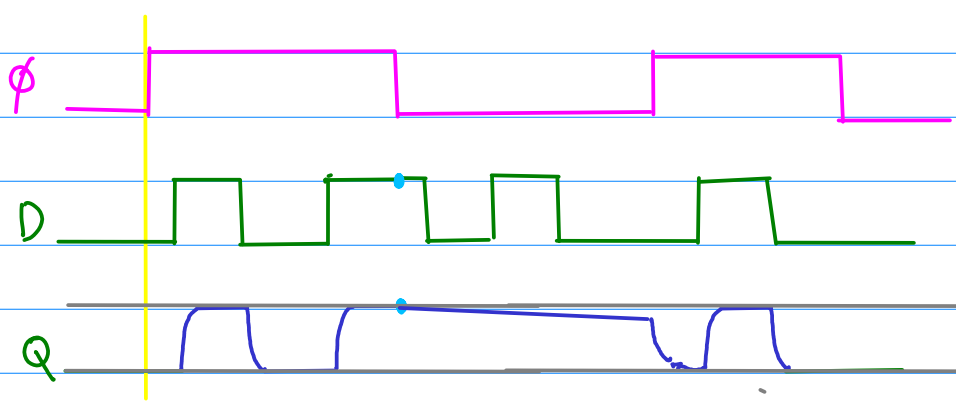
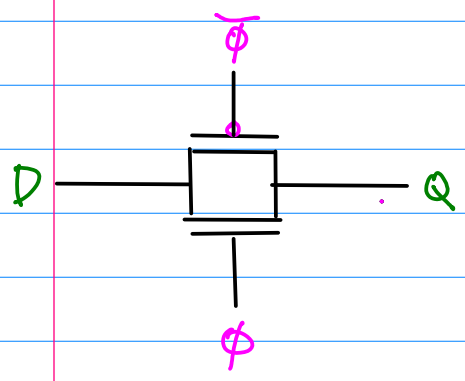


(a) PG (Pass Gate) Latch



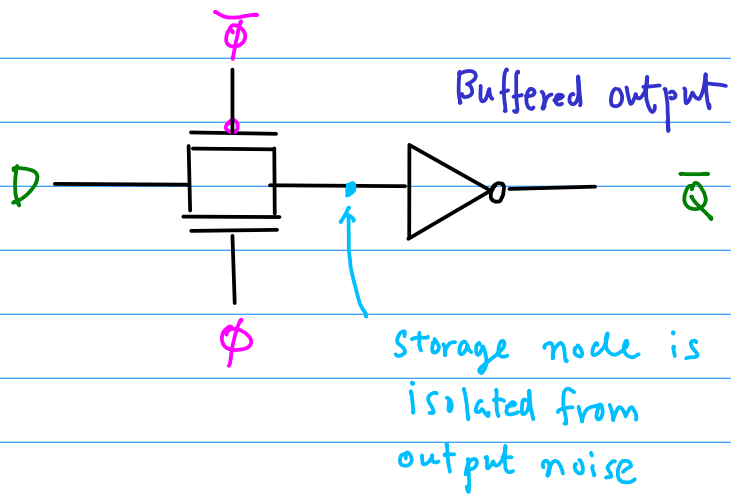
weak 1 leakage

(b) TG (Transmission Gate) Latch

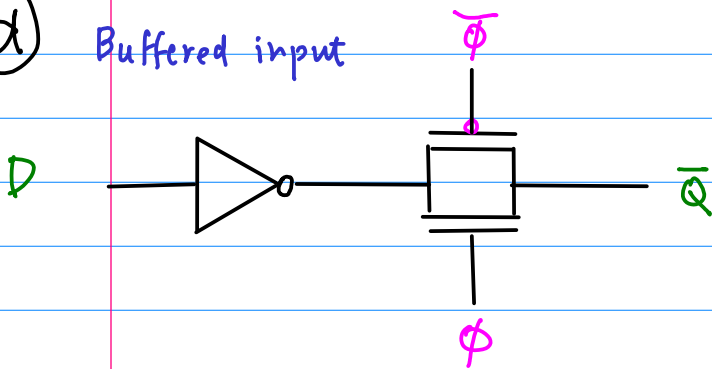


rail-to-rail output swing
 (0 ~ V_{DD}) (strong 1, strong 0)

(c)



(d)



equivalent to Tri-state Inverters

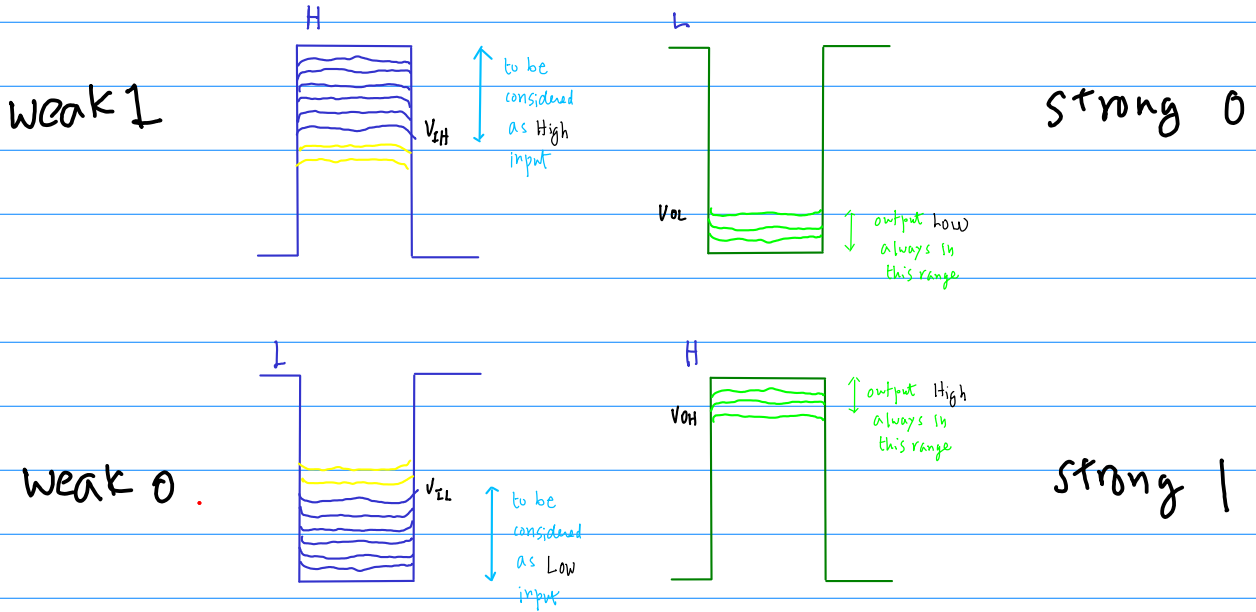
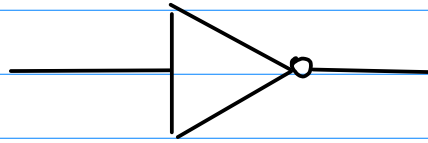
but low logic effort

fast dynamic latch

subthreshold leakage \rightarrow floating storage node
can hold "1" only for
the short period time

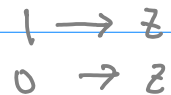
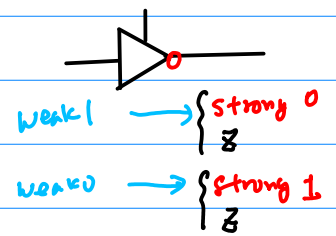
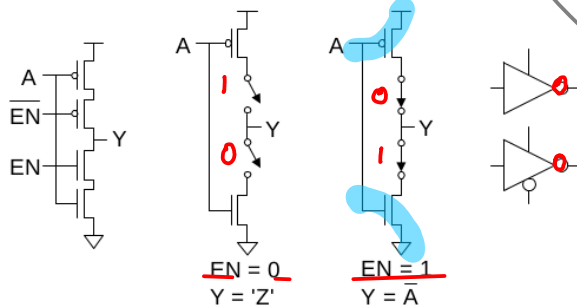
\rightarrow Feedback

Restored Output

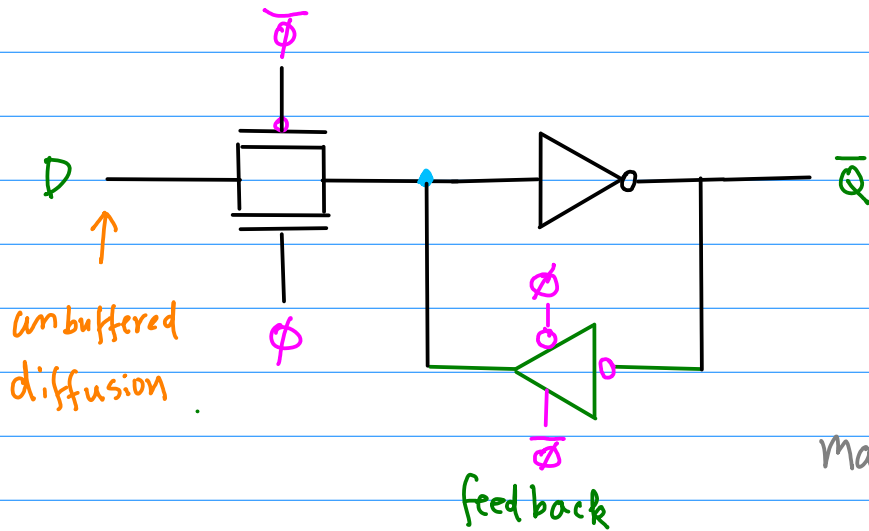


Tristate Inverter

- Tristate inverter produces restored output → can make a signal strong.
- Violates conduction complement rule
- Because we want a Z output



(E)



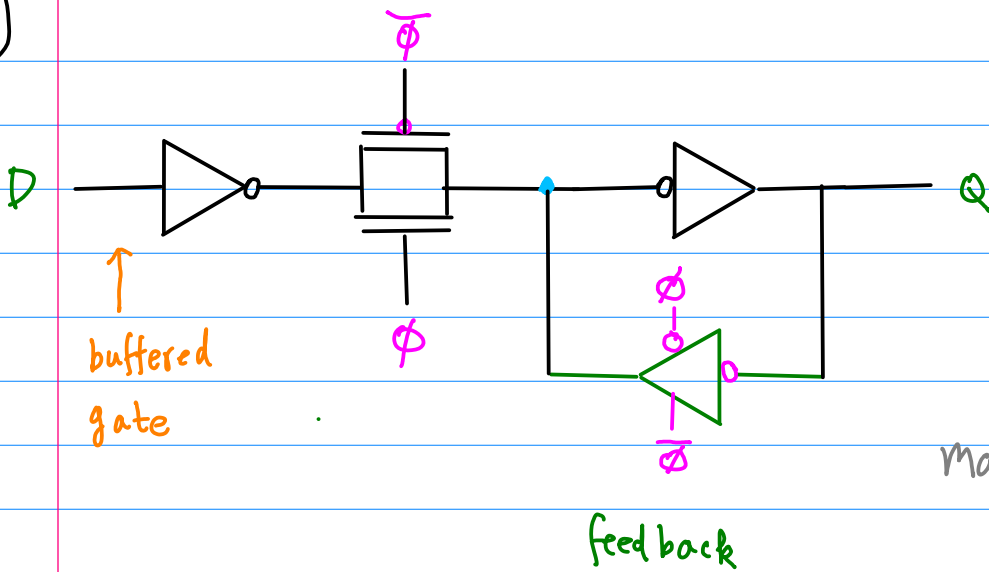
unbuffered diffusion

feedback

Maintain a correct level \bar{Q}

floating \rightarrow static

(F)



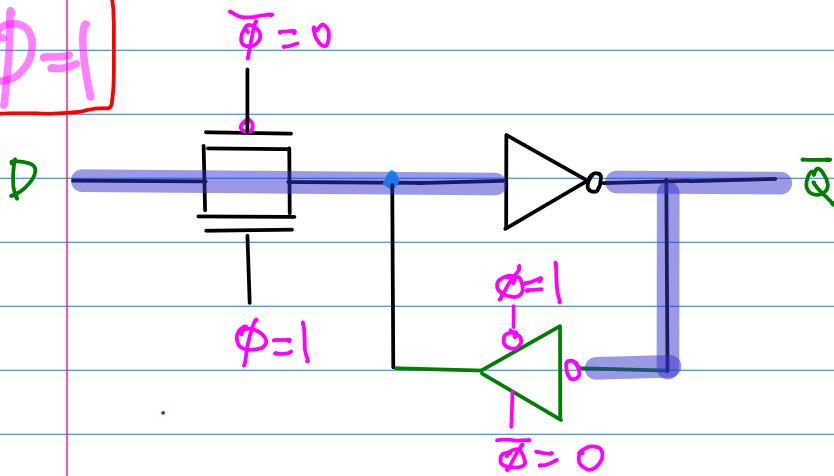
buffered gate

feedback

Main

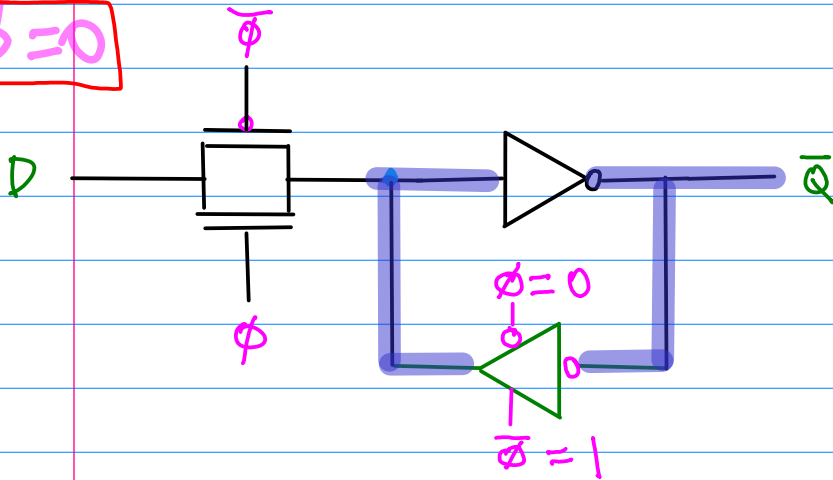
* large noise spark at the output
can contaminate the storage node

$\phi = 1$

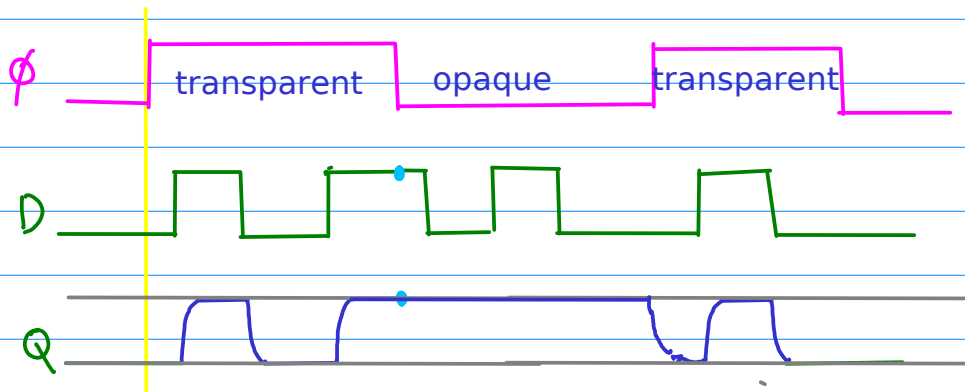


transparent

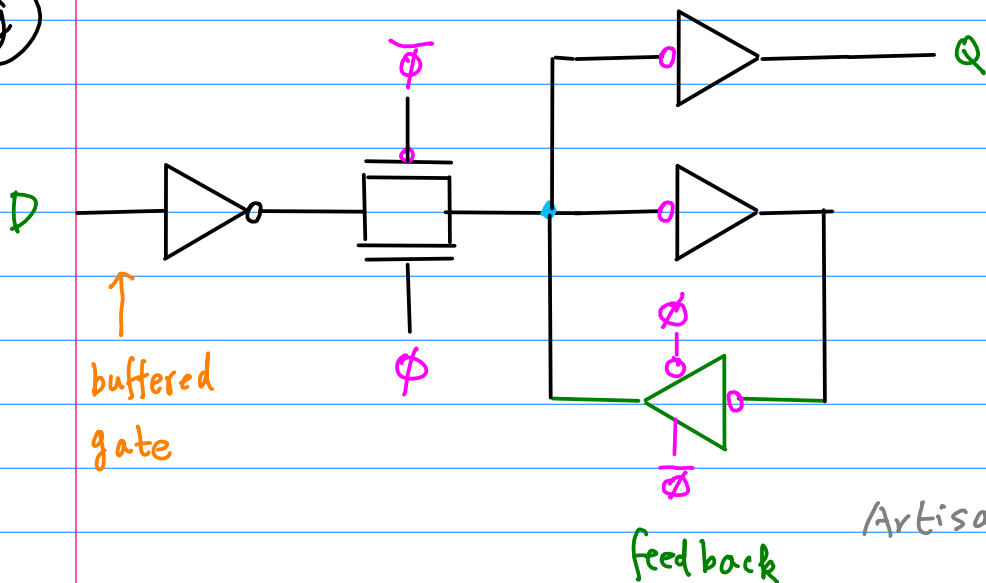
$\phi = 0$



opaque



g



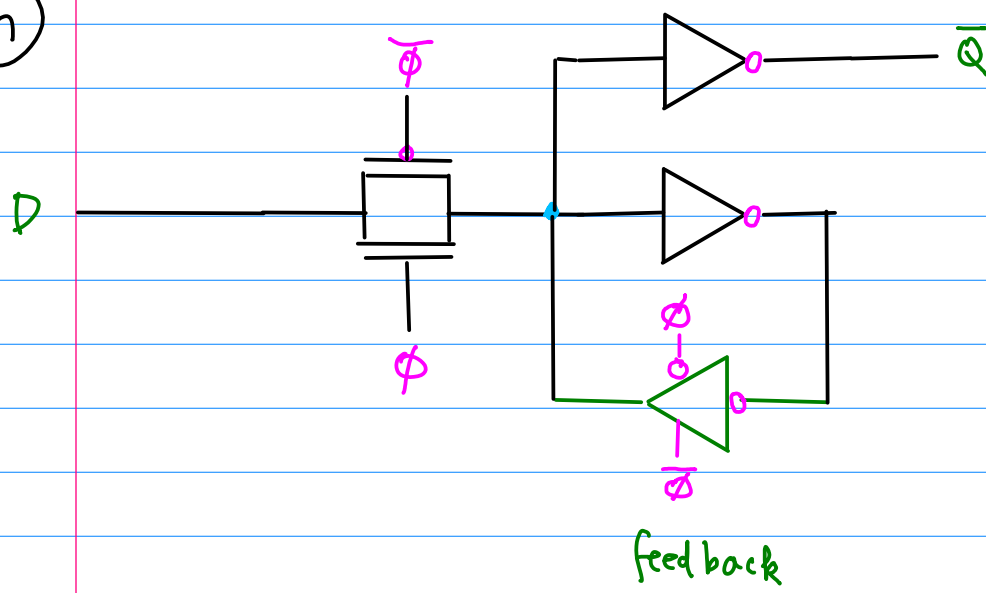
↑
buffered
gate

transparent
static
rail to rail swing
isolated from output
noise
input: gate ~~diff~~

Artisan standard cell library

Suitable for
- not delay critical
- not area critical

h



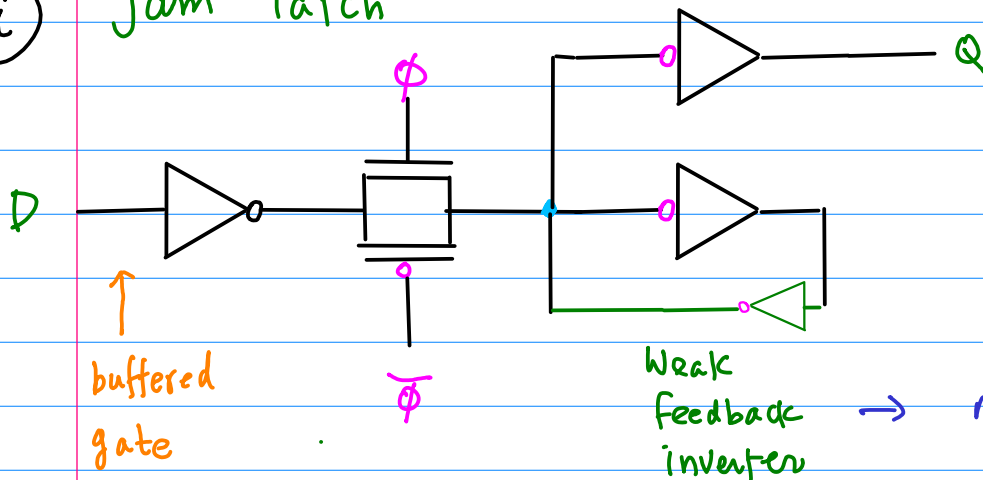
Semi custom
datapath
application

simpler,
faster

Intel

i

jam latch

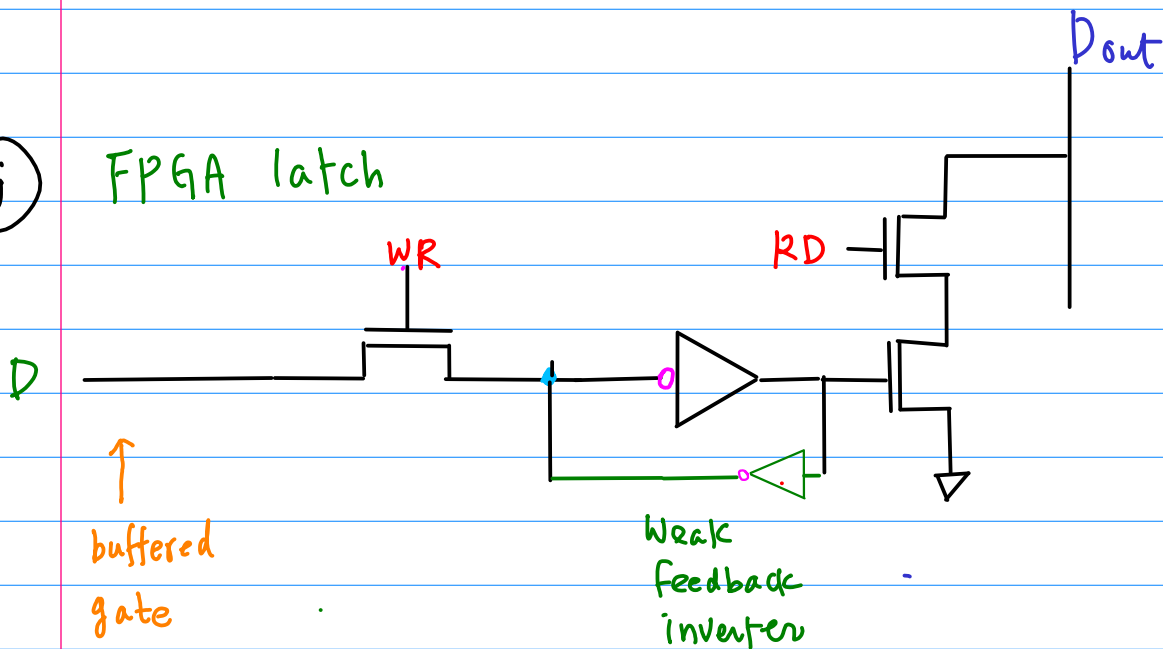


→ reduce clock loads
REMOVE 2 transistors

tri state must overpower the feedback inverter

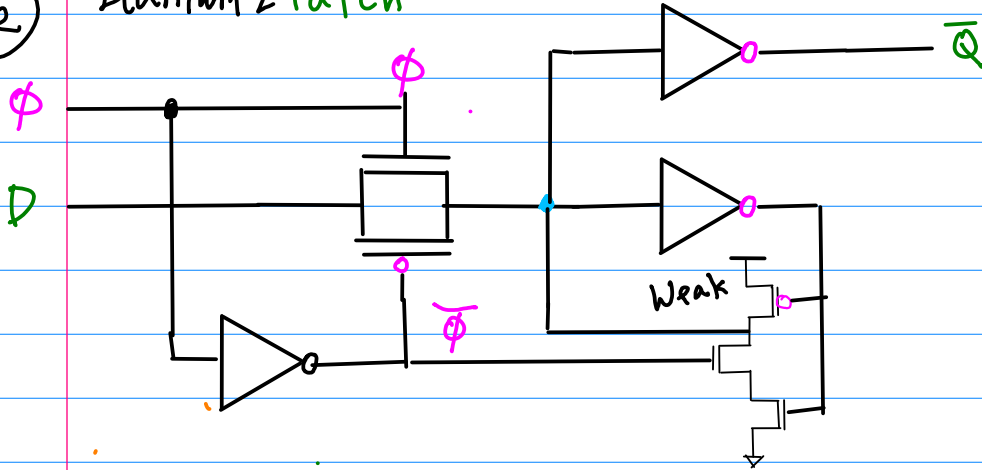
j

FPGA latch



(12)

Itanium 2 latch



Pull down - clocked $\bar{\phi}$
Pull up - weak pMOS

