

Inter-System Communications

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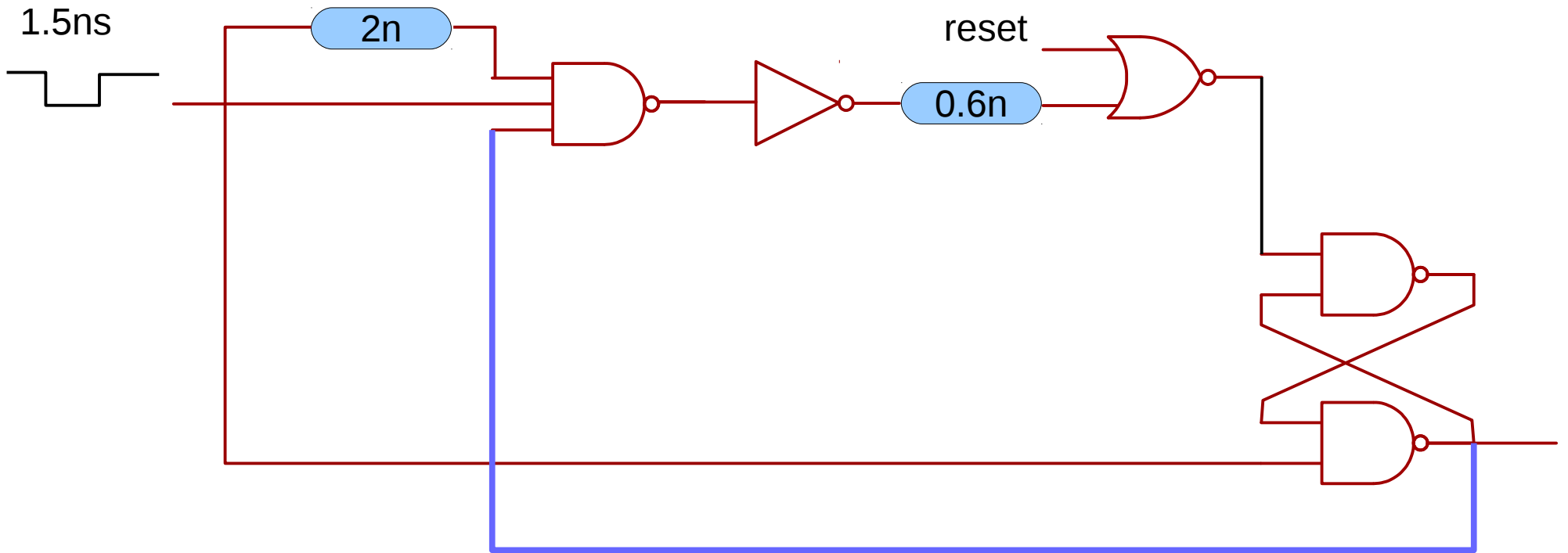
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Asynchronous Design

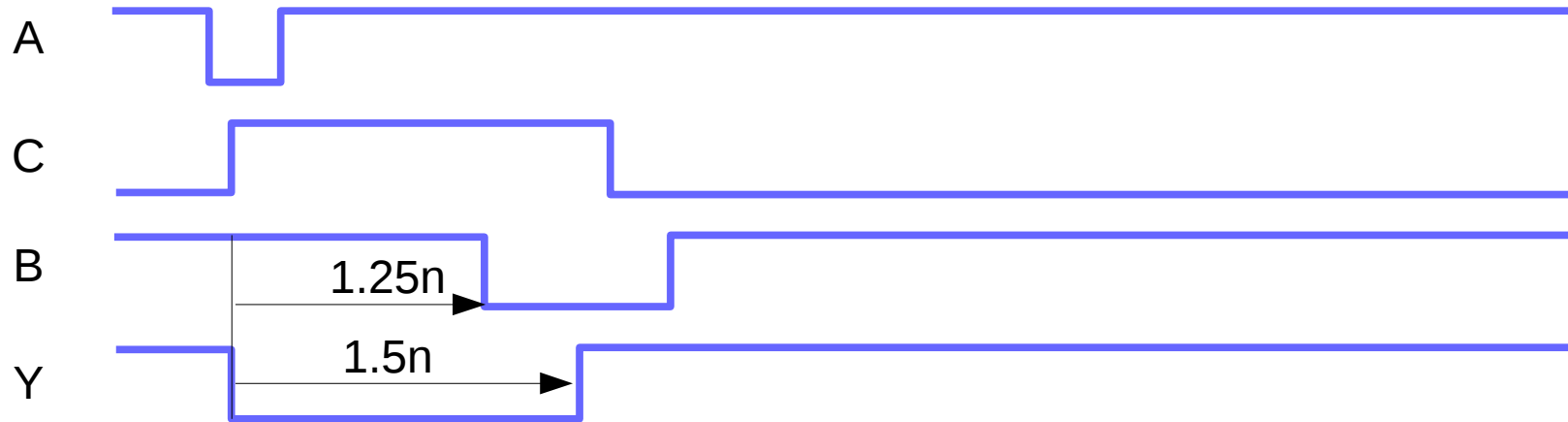
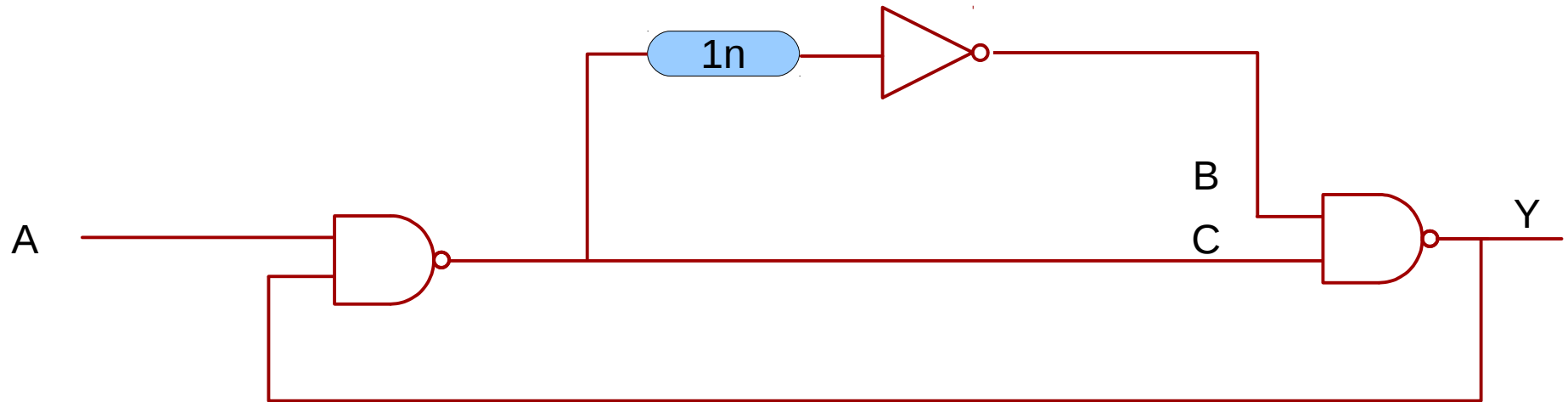
Based on

DRAM Circuit Design, Brent Keeth

Delay-Chain Logic



One-shot Design



Module Interface

References

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- [9] DRAM Circuit Design, Brent Keeth