SRAM based FPGAs (2A)

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Based on

The VLSI Handbook, edited by Wai-Kai Chen, CRC

SRAM based connection

Any horizontal line and any vertical line can be connected
At some cross points by controlling a flip-flop

a flip-flop has one : connect
a flip-flop has zero : disconnect

A flip-flop is a one memory cell of SRAM

- a pass transistor
- a transmission gate
- Multiplexer

A horizontal and a vertical line are
the input of one block and the output of other block

Manufacturer of SRAM based FPGAs

SRAM based FPGAs : Xilinx and Atmel

Focus on Xilinx XC4000

Switch Matrix

A logic block contain SRAM and flip-flops

Each block is connected to nearby one-line segment

A switch matrix :

- a square shaped representation
- a set of multiplexers
- connecting one outgoing line segment of a block
  - and one incoming line segment of another block
- connecting many line segments
  - to form long lines
- connecting global long lines
  - to form longer lines with a fewer number of segments
  - without causing much delay

Routing channels in a LBA

Each logic block has
- SRAMs for table look-up function
- Several flip-flops

These memory elements can be used

Xilinx calls logic block CLB (Configurable Logic Block)

Configurable Logic Block (1)

- A pair of flip-flops
  - Edge triggered D-type flip-flop
  - rising edge or falling edge is selected
  - Common clock input K
  - Clock Enable input EC
  - Asynchronous Set/Reset S/R input
  - XQ, YQ outputs
  - D input is selected from DIN, F', G', and H'

Configurable Logic Block (2)

- 2 independent 4-input function generators
  - realized by SRAM
  - Any 4-input logic function
  - F' and G' outputs
  - F1~F4, G1~G4 inputs
  - Dedicated arithmetic / logic unit
    - For fast generation of carry / borrow
    - Adders / substractors / accumulators / comparators

- Multiplexers map
  - 4 control inputs C1~C4
    - onto H1, DIN, S/R, EC

Configurable Logic Block (3)

- 3rd function generator
  - F', G', H1 : 3 inputs
  - H' output
- CLB outputs X and Y
  - X is selected from H' and F'
  - Y is selected from H' and G'
- A CLB can realize
  - Any two independent 4-input functions
  - Any one 5-input function
  - Any one 4-input function and *some* 5-input functions
  - Some 9-input functions
- Realizing variety of functions in a single logic block
  - Size
  - speed

References

[1] ftp://ftp.geoinfo.tuwien.ac.at/navratil/HaskellTutorial.pdf
[2] https://www.umiacs.umd.edu/~hal/docs/daume02yaht.pdf