Wafer (1A)

Young Won Lim
4/30/13

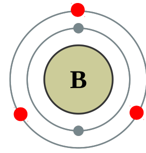
Copyright (c) 2011-2013 Young W. Lim.

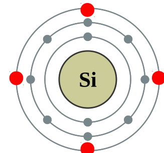
Permission is granted to copy, distribute and/or modify this document under the terms of the GNU Free Documentation License, Version 1.2 or any later version published by the Free Software Foundation; with no Invariant Sections, no Front-Cover Texts, and no Back-Cover Texts. A copy of the license is included in the section entitled "GNU Free Documentation License".

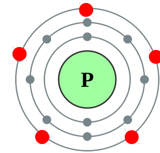
Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

Periodic Table





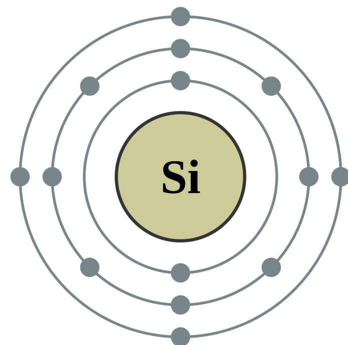


Group → / ↓ Period	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
1	1 H																	2 He
2	3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
3	11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
4	19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
5	37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
6	55 Cs	56 Ba		72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
7	87 Fr	88 Ra		104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Cn	113 Uut	114 Fl	115 Uup	116 Lv	117 Uus	118 Uuo

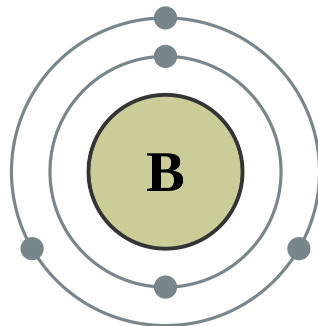
Lanthanides	57 La	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu
Actinides	89 Ac	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr

Acceptor & Donor

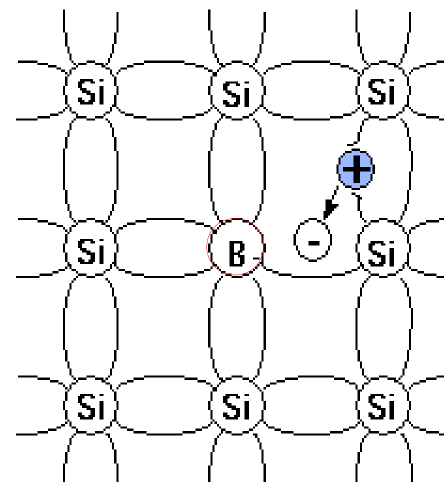
Intrinsic



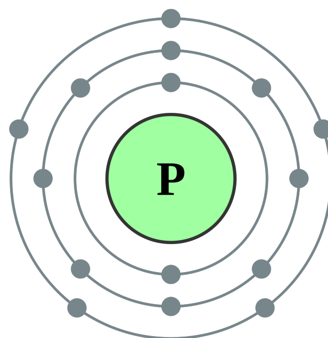
Acceptor



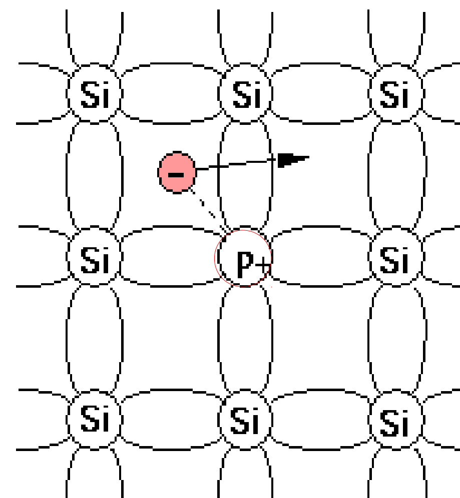
p-type



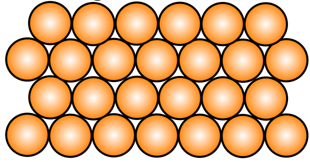
Donor



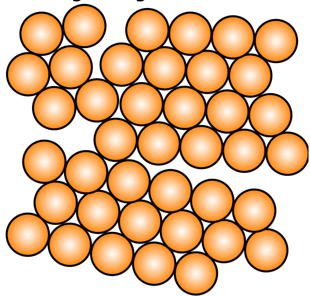
n-type



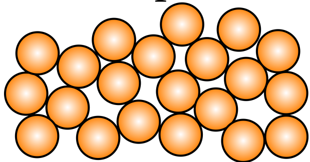
Polycrystal



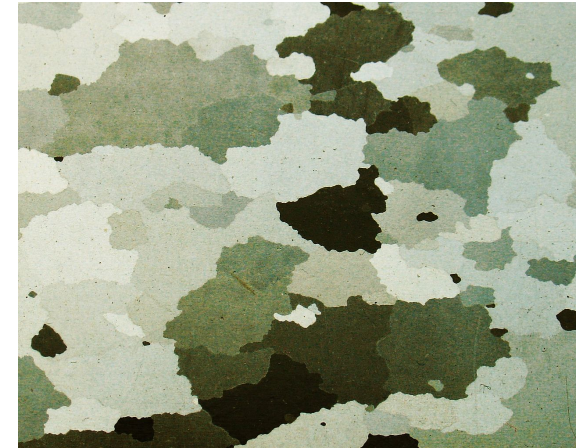
Microscopically, a crystal has atoms in a near-perfect periodic arrangement;



a polycrystal is composed of many microscopic crystals (called "crystallites" or "grains");



an amorphous solid, such as glass, has no periodic arrangement even microscopically.



A photo of electrical steel (coating removed) showing polycrystalline structure

Polycrystalline materials
solids that are composed of many crystallites of varying size and orientation. The variation in direction can be random (called random texture) or directed, possibly due to growth and processing conditions. Fiber texture is an example of the latter.

Single Crystal Silicon

Polycrystalline

- composed of a number of smaller crystals or crystallites.
- a material consisting of multiple small silicon crystals.
- recognized by a visible grain, a "metal flake effect".
- semiconductor grade polycrystalline silicon → single crystal silicon
- the randomly associated crystallites of silicon in "polycrystalline silicon" are converted to a large "single" crystal.
- poly is used both at the macro-scale and micro-scale (component) level.

Single crystal silicon

- the crystalline framework is homogeneous
- recognized by an even external coloring
- the crystal lattice of the entire sample is continuous and unbroken with no grain boundaries.
- large single crystals are exceedingly rare in nature
- also difficult to produce in the laboratory.
- used to manufacture most Si-based microelectronic devices.
- as much as 99.9999% pure.

Single Crystalline Silicon Formation

Wafers are formed of highly pure (99.9999999% purity),
nearly defect-free single crystalline material.

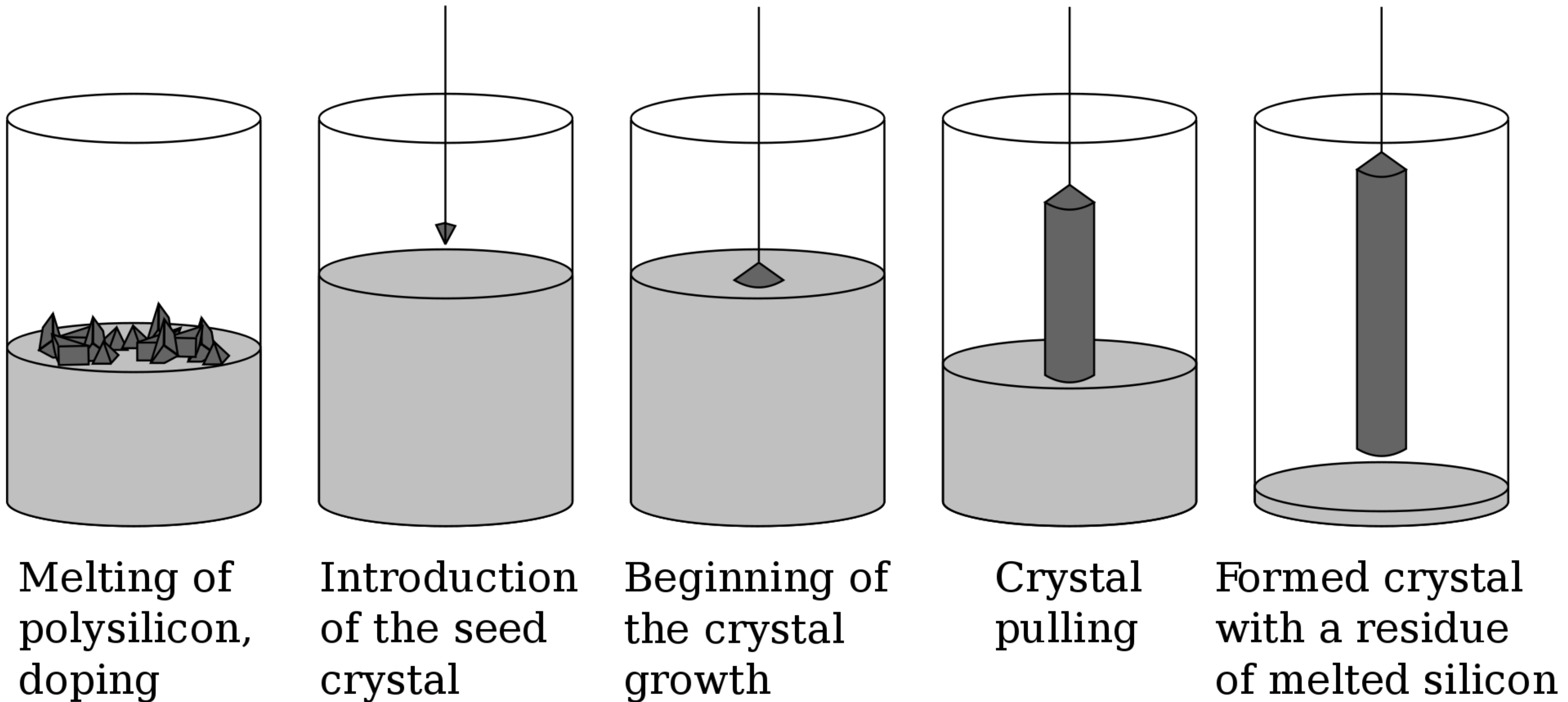
Czochralski growth

- invented by the Polish chemist Jan Czochralski.
- high purity monocrystalline semiconductor (silicon or germanium)
- a cylindrical ingot is formed by pulling a seed crystal from a 'melt'.
- impurity atoms in order to dope the crystal (n-type, p-type)
- The ingot is then sliced with a wafer saw (wire saw)
- and polished to form wafers.
- The size of wafers for photovoltaics is 100–200 mm square
- the thickness is 200–300 μm
- Electronics use wafer sizes from 100–300 mm diameter

Bridgman Growth

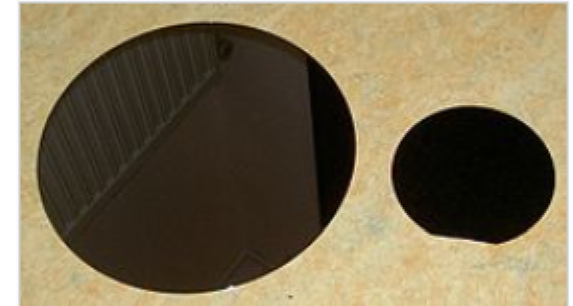
Float Zone Growth

Czochralski Growth



Wafer Production

1. Ingot Growing
2. Shaping
3. Polishing
4. Cleansing


Polished 12" and 6" silicon wafers. The flat cut into the right wafer indicates its doping and crystallographic orientation (see below)

Silicon boule for the production of wafers

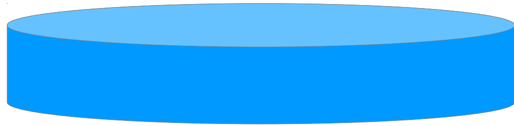
Crystal Growth and Wafer Slicing Process
- Step 1: Obtaining the Sand
- Step 2: Preparing the Molten Silicon Bath
- Step 3: Making the Ingot
- Step 4: Preparing the Wafers

Thickness Sorting
Lapping & Etching Processes
Thickness Sorting and Flatness Checking
Polishing Process
Final Dimensional and Electrical Properties Qualification

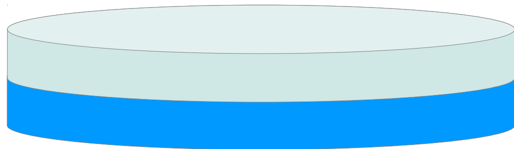
Remove any cracked and damaged surface silicon on the surface

Types of Silicon Wafers

Bulk polished Silicon Wafer



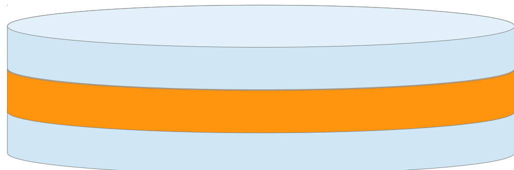
Epi Silicon Wafer



Heavily doped bulk wafers with moderately to lightly doped epitaxial silicon layer

Immunity to latch-up

Silicon on Insulator Wafer



increase performance
Eliminate latch-up

silicon dioxide or sapphire

Epitaxial Growth

the Greek roots epi (above) and taxis (in ordered manner)--> "to arrange upon".

Epitax: the deposition of a crystalline overlayer on a crystalline substrate

Epitaxial growth: there must be one or more preferred orientations of the overlayer with respect to the substrate

the overlayer - an epitaxial film or epitaxial layer

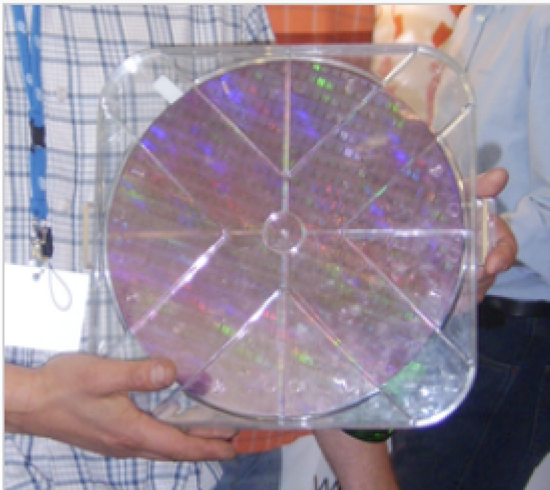
Epitaxial films may be grown from gaseous or liquid precursors.

- VPE (Vapor Phase Epitaxy)
- LPE (Liquid Phase Epitaxy)
- SPE (Solid Phase Epitaxy)

If an epitaxial film is deposited on a substrate of the same composition, the process is called **homoepitaxy**; otherwise it is called **heteroepitaxy**.

Wafer Fabrication (1)

Polished 12" and 6" silicon wafers. The flat cut into the right wafer indicates its doping and crystallographic orientation (see below)



VLSI microcircuits fabricated on a 12-inch (300 mm) silicon wafer, before dicing and packaging

Wafer production

Wafer fabrication
a procedure composed of many repeated sequential processes to produce complete electrical or photonic circuits.

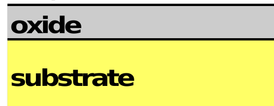
electrical circuit specifications

circuit layout programs (computer aided design)

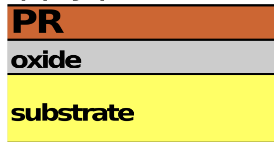
photomask production

Wafer Fabrication (2)

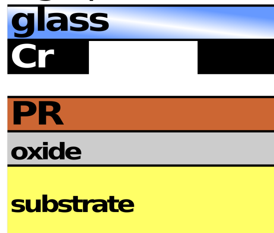
a. Prepare wafer



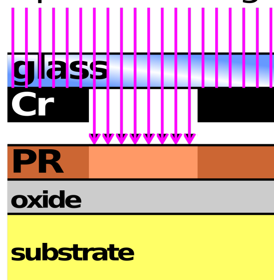
b. Apply photoresist



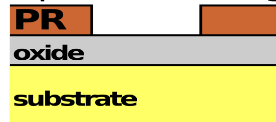
c. Align photomask



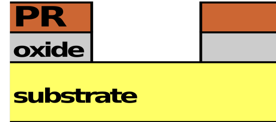
d. Expose to UV light



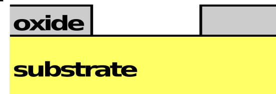
e. Develop and remove photoresist exposed to UV light



f. Etch exposed oxide



g. Remove remaining photoresist



Photolithography

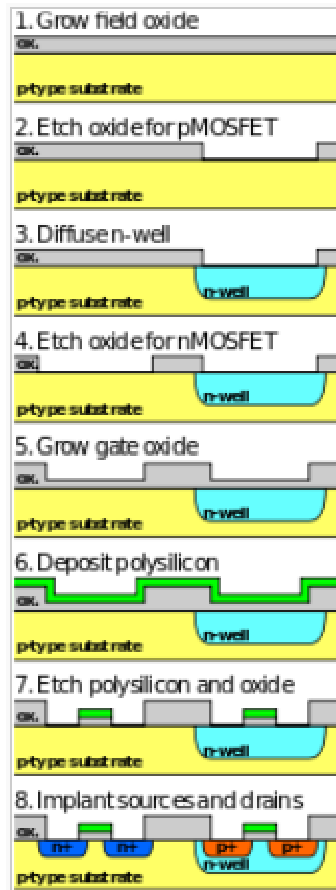
- Apply oxide
- Photoresist application (**PR**)
- Exposure and developing (Cr + glass)
- Etching Oxide
- Photoresist removal

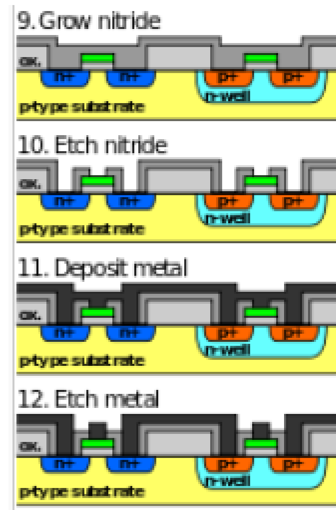
- Silicon wafers start out blank and pure.
- The circuits are built in layers.
- photo-sensitive resistance patterns are photo-masked
- then exposed to short-wave ultraviolet light
- the unexposed areas are thus etched away and cleaned.
- Hot chemical vapors are deposited on to the desired zones and baked
- the vapors are permeated into the desired zones.
- In some cases, ions, such as O2+ or O+, are implanted

These steps are often repeated many hundreds of times

Wafer Fabrication (3)

Simplified illustration of the process of fabrication of a CMOS inverter
Each etch step is detailed in the previous slide





Oxidation Layering
Photo lithography
Etching
Diffusion
Thin Film

- Silicon wafers start out blank and pure.
- The circuits are built in layers.
- photo-sensitive resistance patterns are photo-masked
- then exposed to short-wave ultraviolet light
- the unexposed areas are thus etched away and cleaned.
- Hot chemical vapors are deposited on to the desired zones and baked
- the vapors are permeated into the desired zones.
- In some cases, ions, such as O2+ or O+, are implanted

Thermal Oxidation

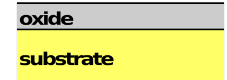
SiO_2 :
* Insulator
* A good diffusion mask
  Very good etching selectivity

Thermal oxidation is a way to
- produces a thin layer of oxide (usually silicon dioxide) on the surface of a wafer : High Temperature Oxide layer (HTO)
- forces an oxidizing agent to diffuse into the wafer at high temperature and react with it.
- may use either water vapor (**wet oxidation**) or molecular oxygen (**dry oxidation**) as the oxidant
- performed in furnaces, at temperatures between 800 and 1200°C.
- a single furnace accepts many wafers at the same time

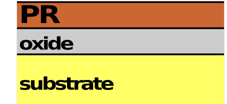
Photolithography

- a process to pattern parts of a thin film or the bulk of a substrate
- uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical "photoresist" on the substrate.
- either engraves the exposure pattern into, or enables deposition of a new material in the desired pattern upon, the material underneath the photo resist.

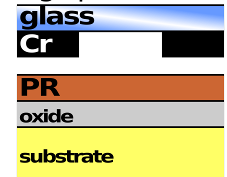
a. Prepare wafer



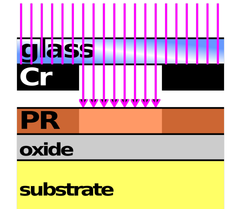
b. Apply photoresist



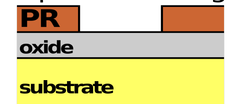
c. Align photomask



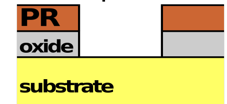
d. Expose to UV light



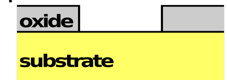
e. Develop and remove photoresist exposed to UV light

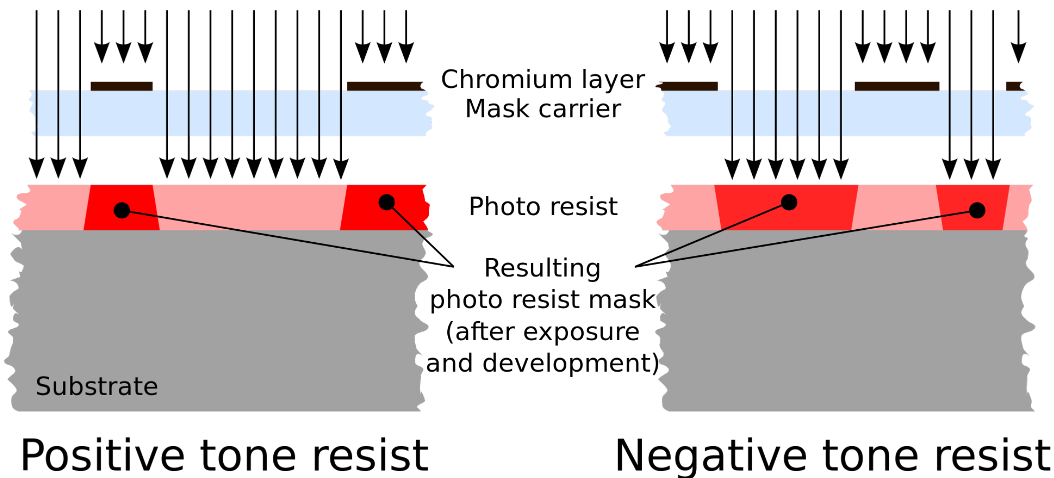


f. Etch exposed oxide



g. Remove remaining photoresist





Etching

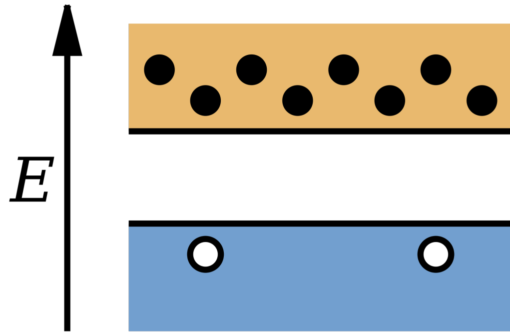
used to chemically remove layers from the surface of a wafer
part of the wafer is protected from the etchant by a "masking" material
the masking material is a photoresist which has been patterned using photolithography.
a more durable mask, such as silicon nitride

Wet etching
liquid-phase ("wet") etchants
the wafer can be immersed in a bath of etchant
buffered hydrofluoric acid (BHF)

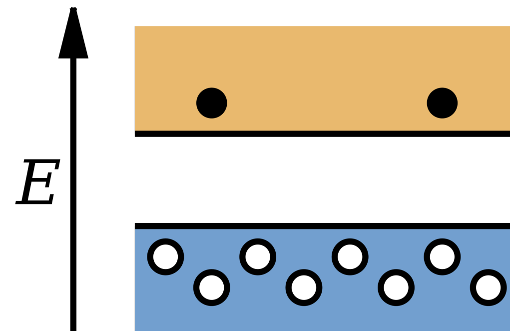
Anisotropic wet etching
Orientation dependent etching
Some wet etchants etch crystalline materials at very different rates depending upon which crystal face is exposed

Plasma etching
Modern VLSI processes avoid wet etching, and use plasma etching instead.
Plasma etchers can operate in several modes by adjusting the parameters of the plasma.

Doping



Extrinsic semiconductors with a larger electron concentration than hole concentration are known as n-type semiconductors. The phrase 'n-type' comes from the negative charge of the electron. In n-type semiconductors, electrons are the majority carriers and holes are the minority carriers. N-type semiconductors are created by doping an intrinsic semiconductor with donor impurities.

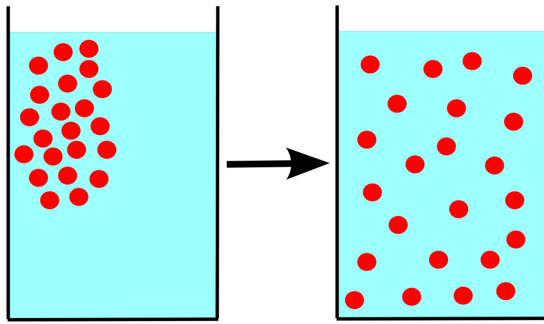


As opposed to n-type semiconductors, p-type semiconductors have a larger hole concentration than electron concentration. The phrase 'p-type' refers to the positive charge of the hole. In p-type semiconductors, holes are the majority carriers and electrons are the minority carriers. P-type semiconductors are created by doping an intrinsic semiconductor with acceptor impurities.

Diffusion : The spread of particles through random motion from regions of higher concentration to regions of lower concentration

Ion implantation : Bombarding the substrate with ions accelerated to high velocities

Diffusion



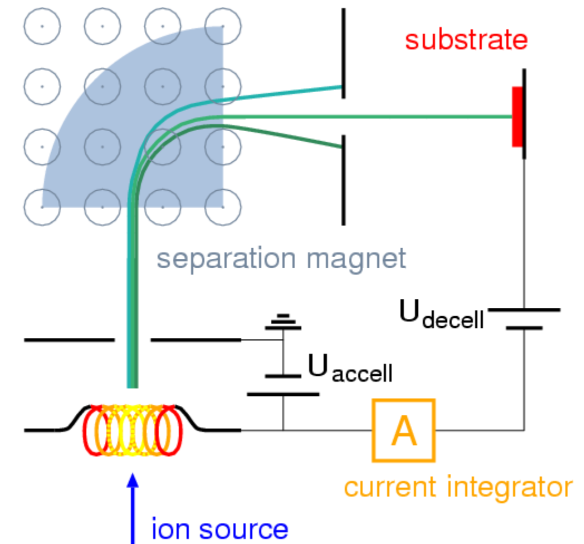
A diffusion process in science. Some particles are dissolved in a glass of water. Initially, the particles are all near one corner of the glass. If the particles all randomly move around ("diffuse") in the water, then the particles will eventually become distributed randomly and uniformly, and organized (but diffusion will still continue to occur, just that there will be no net flux).

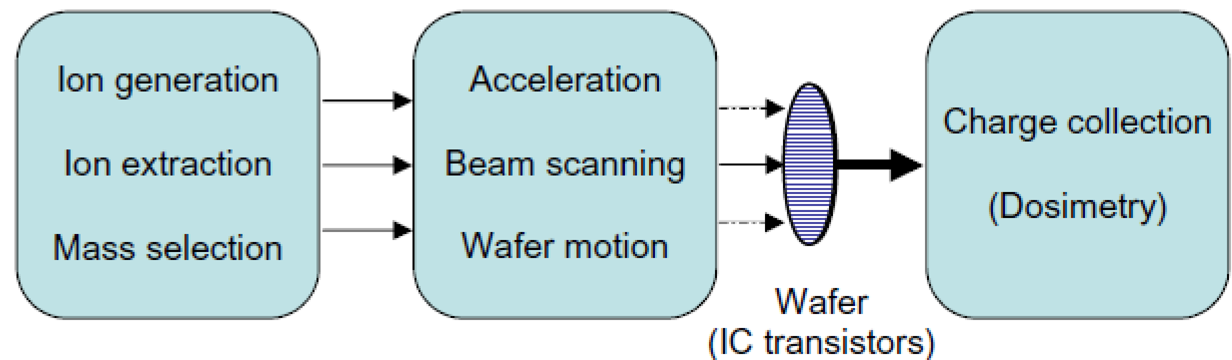
Predeposition : to introduce the required dose of dopant into the substrate.

Drive-In : a subsequent drive-in anneal then redistributes the dopant giving the required junction depth and surface concentration.

Ion Implantation

Ion implantation is a materials engineering process by which ions of a material are accelerated in an electrical field and impacted into a solid. This process is used to change the physical, chemical, or electrical properties of the solid.





Thin Film Deposition

- **thin**: a layer of material ranging from fractions of a nanometer (monolayer) to several micrometers in thickness.
- the act of applying a thin film to a surface
- onto a substrate or onto previously deposited layers
- molecular beam epitaxy: a single layer of atoms

Chemical deposition

Physical deposition

Chemical Deposition

- a fluid precursor undergoes a chemical change at a solid surface, leaving a solid layer.
- like the formation of soot on a cool object when it is placed inside a flame.
- deposition happens on every surface, with little regard to direction;
- tend to be conformal, rather than directional.

A **conformal** film defines a morphologically uneven interface with another body and has a thickness that is the same everywhere along the interface.

- **Plating**
- **Chemical solution deposition** (CSD) or **Chemical bath deposition** (CBD)
- **Spin coating** or **spin casting**
- **Chemical vapor deposition** (CVD)
  - **Plasma enhanced CVD** (PECVD)
- **Atomic layer deposition** (ALD)

Physical Deposition

- mechanical, electromechanical or thermodynamic means
- like the formation of frost
- most engineering materials are held together by relatively high energies
- chemical reactions are not used to store these energies
- require a low-pressure vapor environment to function properly
- most can be classified as physical vapor deposition (PVD).

- **Thermal evaporator**
  - **Electron beam evaporator**
  - **Molecular beam epitaxy** (MBE)
- **Sputtering**
- **Pulsed laser deposition**
- **Cathodic arc deposition** (arc-PVD)
- **Electrohydrodynamic deposition** (Electrospray deposition)

Metallization

coating **metal** on the surface of non-metallic objects.

Plating relies on **liquid precursors**, often a solution of water with a **salt of the metal** to be deposited. Some plating processes are driven entirely by reagents in the solution (usually for noble metals), but by far the most commercially important process is **electroplating**.

Chemical vapor deposition (CVD) generally uses a **gas**-phase precursor, often a **halide** or **hydride** of the element to be deposited. In the case of MOCVD, an **organometallic gas** is used. Commercial techniques often use very low pressures of precursor gas.

Physical vapor deposition (PVD).The material to be deposited is placed in an **energetic, entropic environment**, so that particles of material **escape** its surface. Facing this source is a **cooler surface** which draws energy from these particles as they arrive, allowing them to form a solid layer. The whole system is kept in a vacuum deposition chamber, to allow the particles to travel as freely as possible. Since particles tend to follow a straight path, films deposited by physical means are commonly **directional**, rather than **conformal**.

Dielectric

Insulator: SiO2 Si2N4 SiON

Plasma enhanced CVD (PECVD) uses an ionized vapor, or plasma, as a precursor. Unlike the soot example above, commercial PECVD relies on electromagnetic means (electric current, microwave excitation), rather than a chemical reaction, to produce a plasma.

Spin coating or spin casting, uses a liquid precursor, or sol-gel precursor deposited onto a smooth, flat substrate which is subsequently spun at a high velocity to centrifugally spread the solution over the substrate. The speed at which the solution is spun and the viscosity of the sol determine the ultimate thickness of the deposited film. Repeated depositions can be carried out to increase the thickness of films as desired. Thermal treatment is often carried out in order to crystallize the amorphous spin coated film (orientations).

Atomic layer deposition (ALD) uses gaseous precursor to deposit conformal thin films one layer at a time. Two half reactions, run in sequence and repeated for each layer, in order to ensure total layer saturation. As a result of the stepwise, the process is slower than CVD, however it can be run at low temperatures, unlike CVD.

Mask

References

[1] http://en.wikipedia.org/