Memory Interface (1A)

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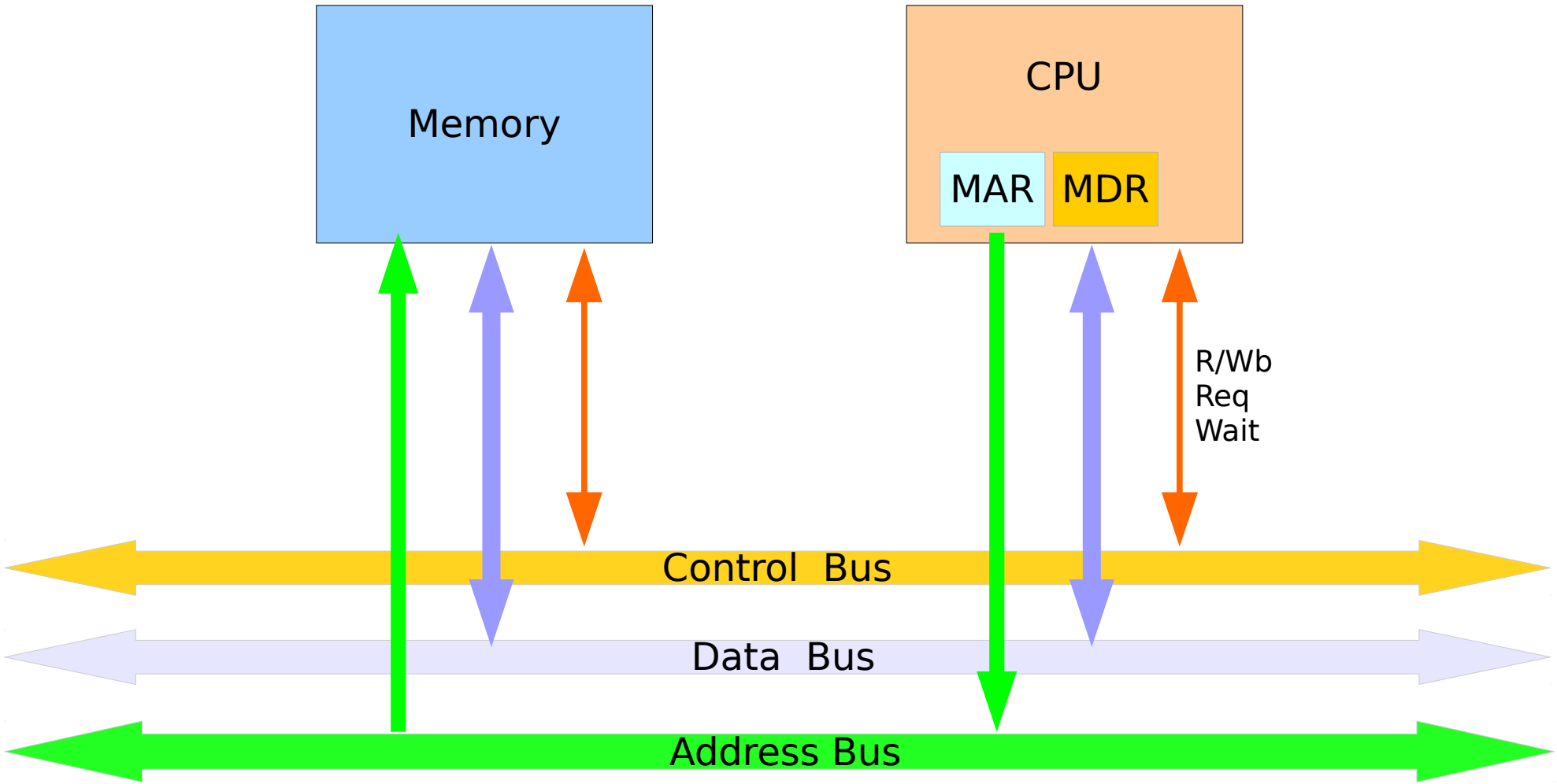
Memory Interface

- MAR (Memory Address Register)
- MDR (Memory Data Register)
- FSM (Finite State Machine)

MAR and MDR

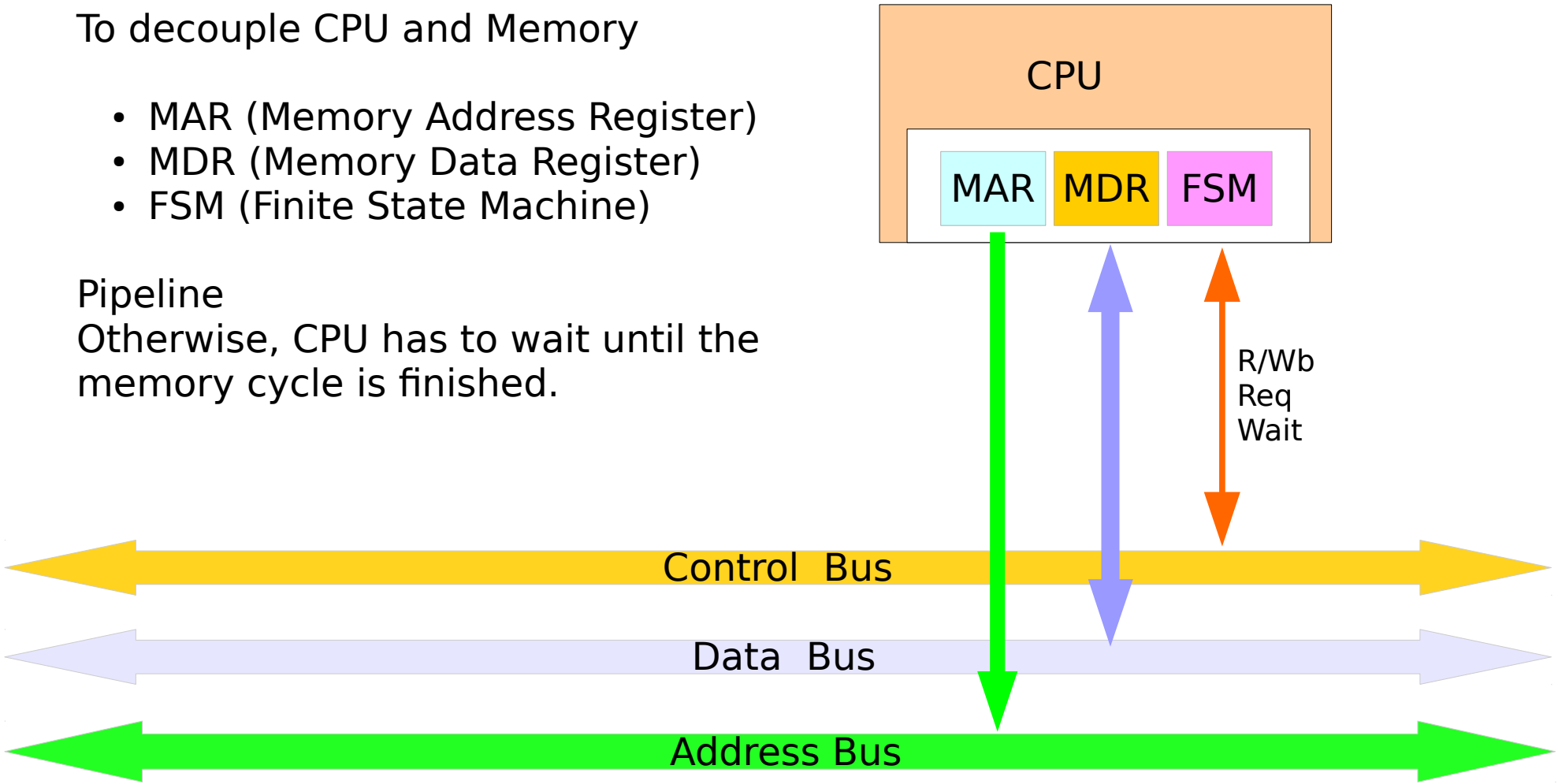

Memory
CPU
MAR
MDR
R/Wb
Req
Wait
Control Bus
Data Bus
Address Bus

MAR and MDR

To decouple CPU and Memory

- MAR (Memory Address Register)
- MDR (Memory Data Register)
- FSM (Finite State Machine)

Pipeline
Otherwise, CPU has to wait until the memory cycle is finished.



CPU-Memory Handshake

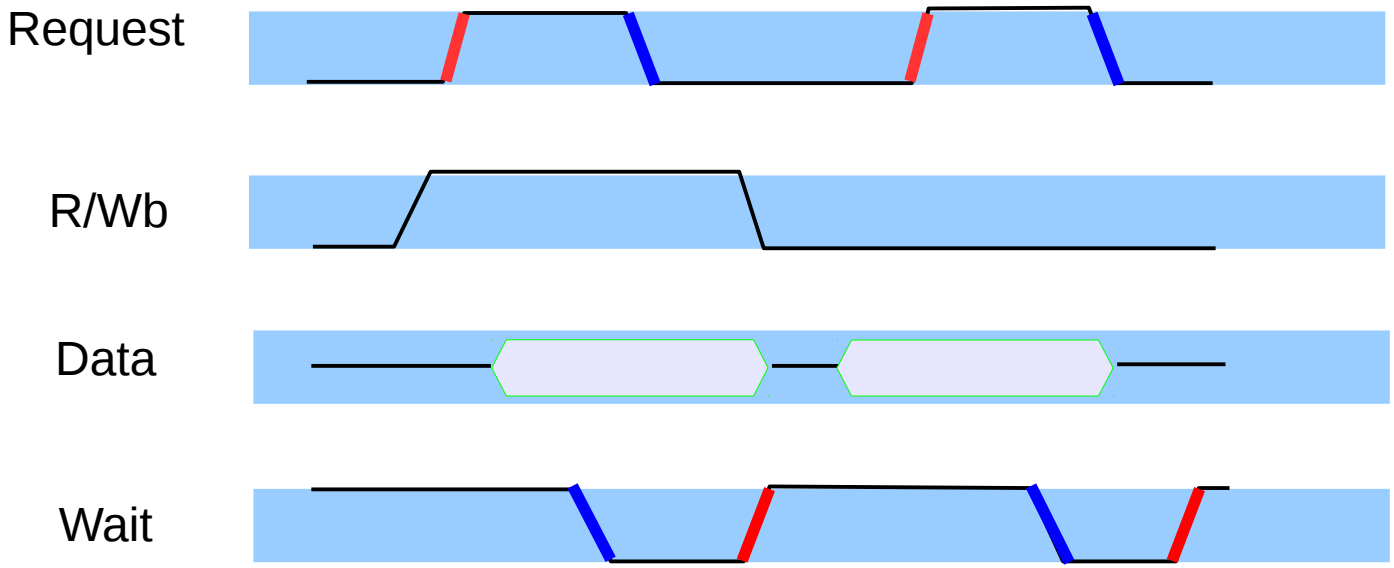
Cycle 1: Request asserted. Read data placed on memory data bus.
Cycle 2: Wait deasserted. CPU latches read data into MBR.
Cycle 3: Request deasserted.
Cycle 4: Wait asserted.

http://www-inst.eecs.berkeley.edu/~cs150/fa05/CLD_Supplement/chapter11/chapter11.doc1.html

CPU-Memory Handshake

No Common Clock → Handshake

Cycle 1: Request asserted. Read data placed on memory data bus.
Cycle 2: Wait deasserted. CPU latches read data into MBR.
Cycle 3: Request deasserted.
Cycle 4: Wait asserted.



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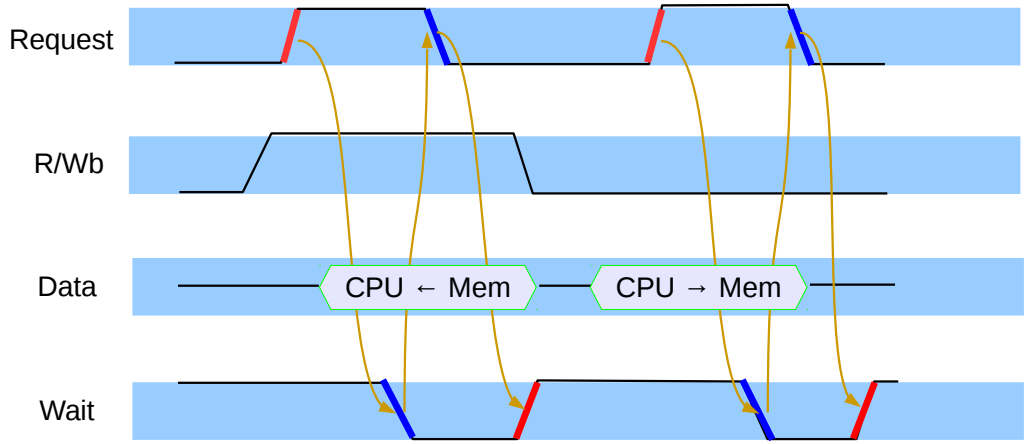
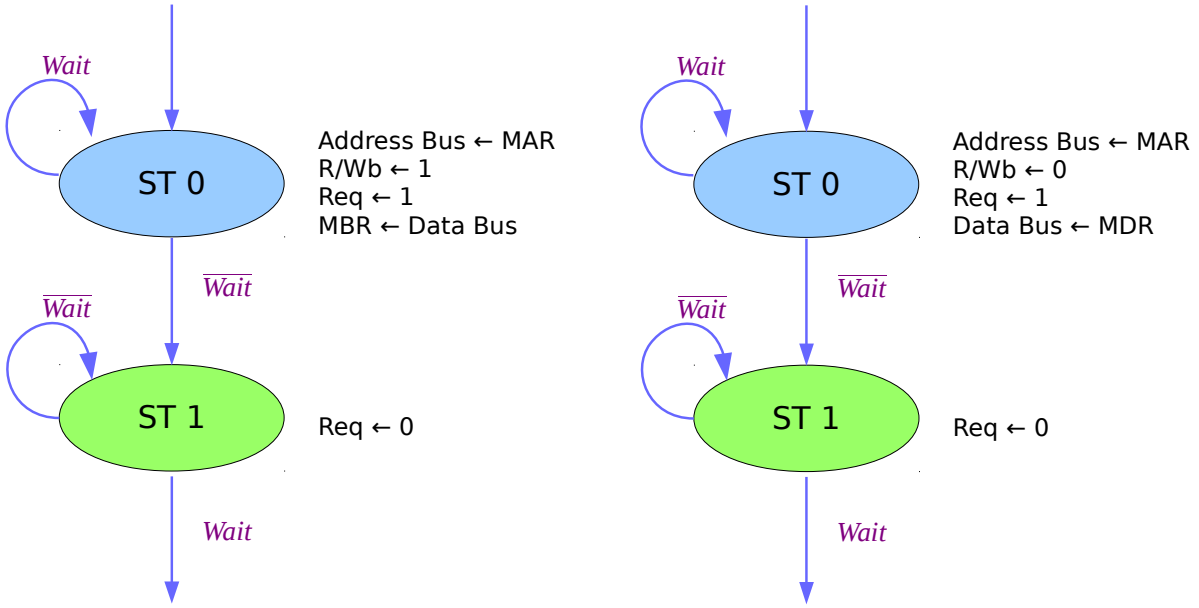
Simole Memory Interface Timing Waveform





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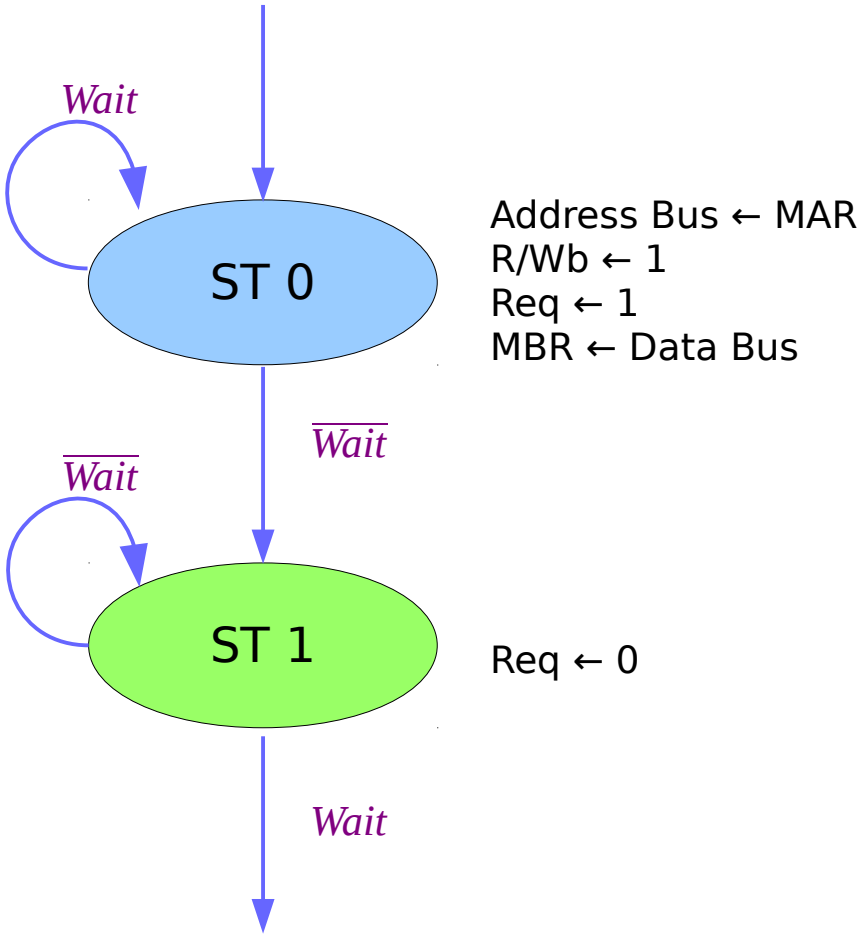
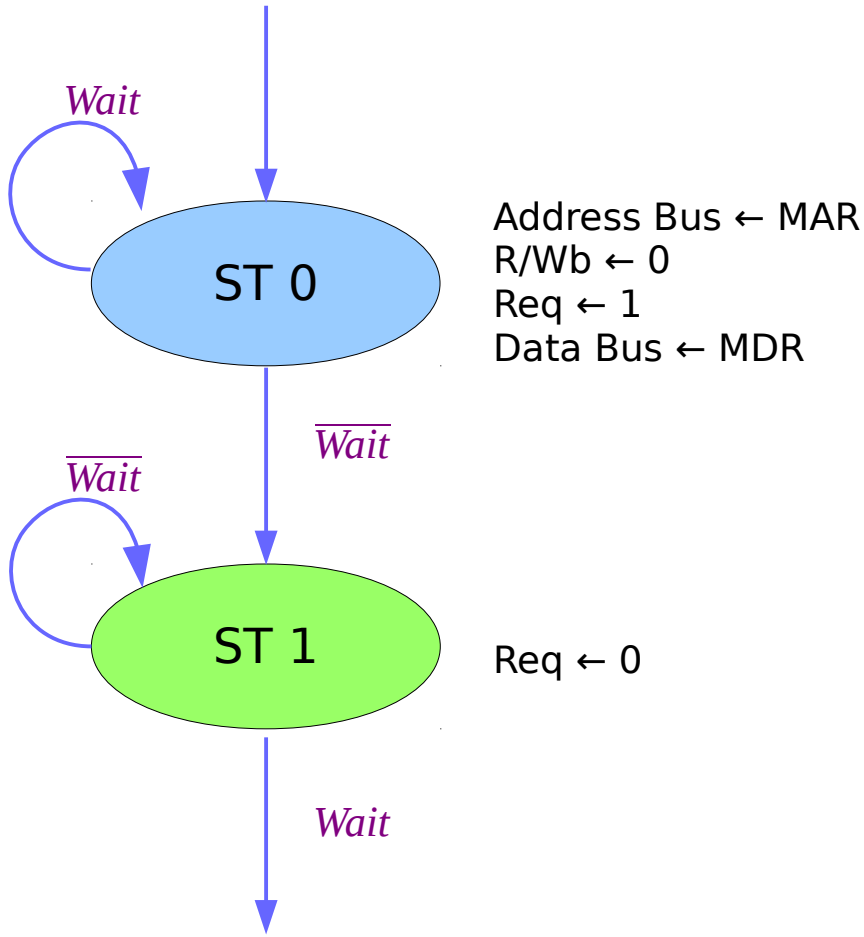
Read & Write FSM





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References

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[3] C A Reference Manual, Samuel P. Harbison & Guy L. Steele Jr.
[4] C Language Express, I. K. Chun