

# CMOS Transistor Size (3G)

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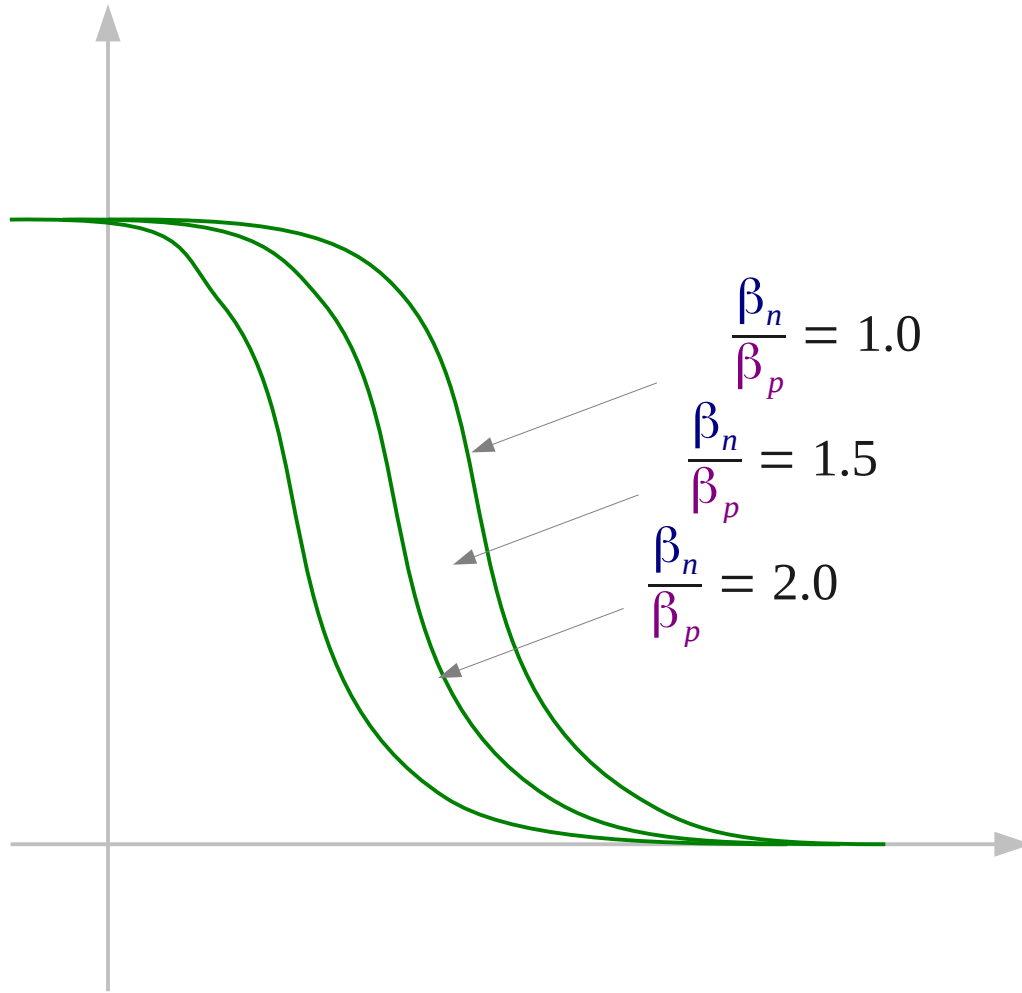
# Transconductance Parameter

When  $V_{GS} > V_t$  and  $V_{DS} < (V_{GS} - V_t)$

$$I_d = k' \frac{W}{L} \left[ (v_{gs} - v_t) v_{ds} - \frac{1}{2} v_{ds}^2 \right]$$

When  $V_{GS} > V_t$  and  $V_{DS} \geq (V_{GS} - V_t)$

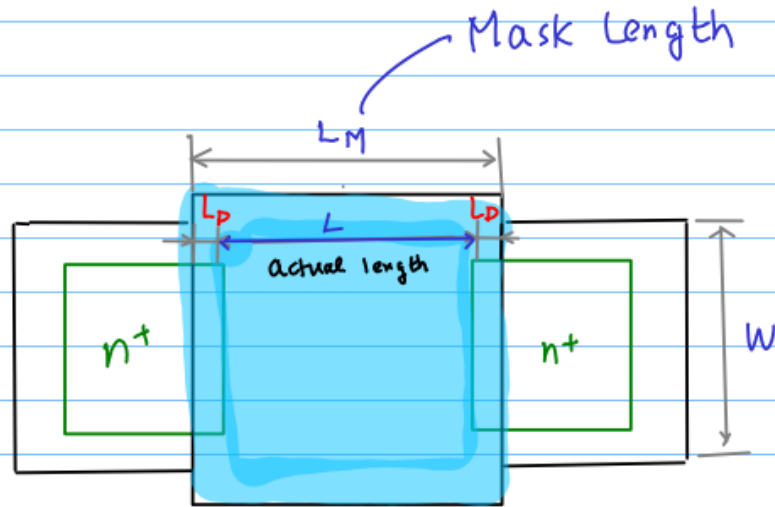
$$I_d = \frac{1}{2} k' \frac{W}{L} (v_{gs} - v_t)^2$$



$$\beta_p = k'_p \left( \frac{W}{L} \right)_p$$

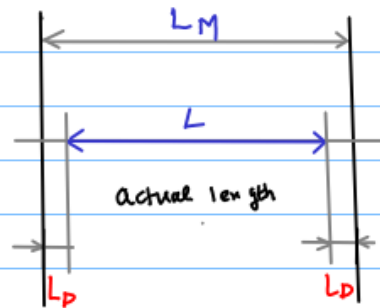
$$\beta_n = k'_n \left( \frac{W}{L} \right)_n$$

# Channel Length

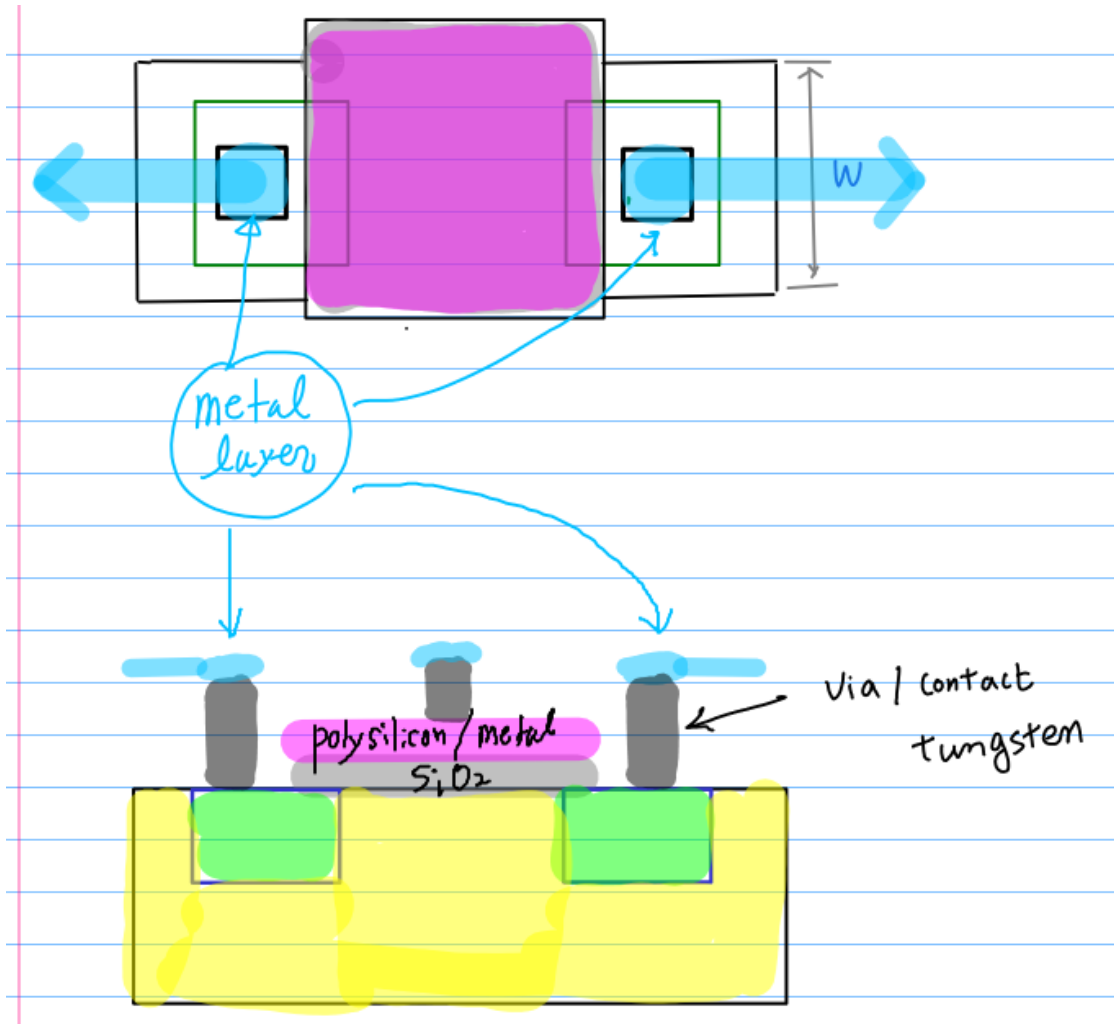


$$L = L_M - 2L_D$$

- ⊙  $L_M$  : Mask Length
- ⊙  $L$  : Channel Length.
- ⊙  $L_D$  : Overlapped Length



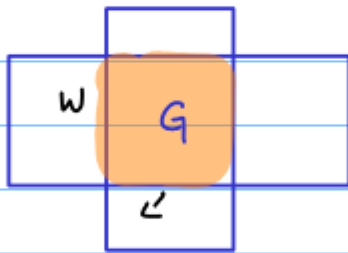
# Transistor Dimensions



# Capacitances of S, D, G

① Oxide Capacitance

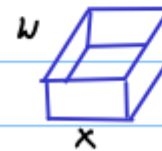
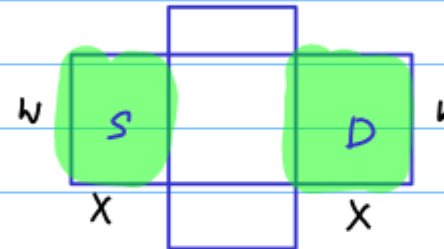
$C_g$



$$C_g = C_{ox} L'W$$

② Junction Capacitance

$C_s, C_D$



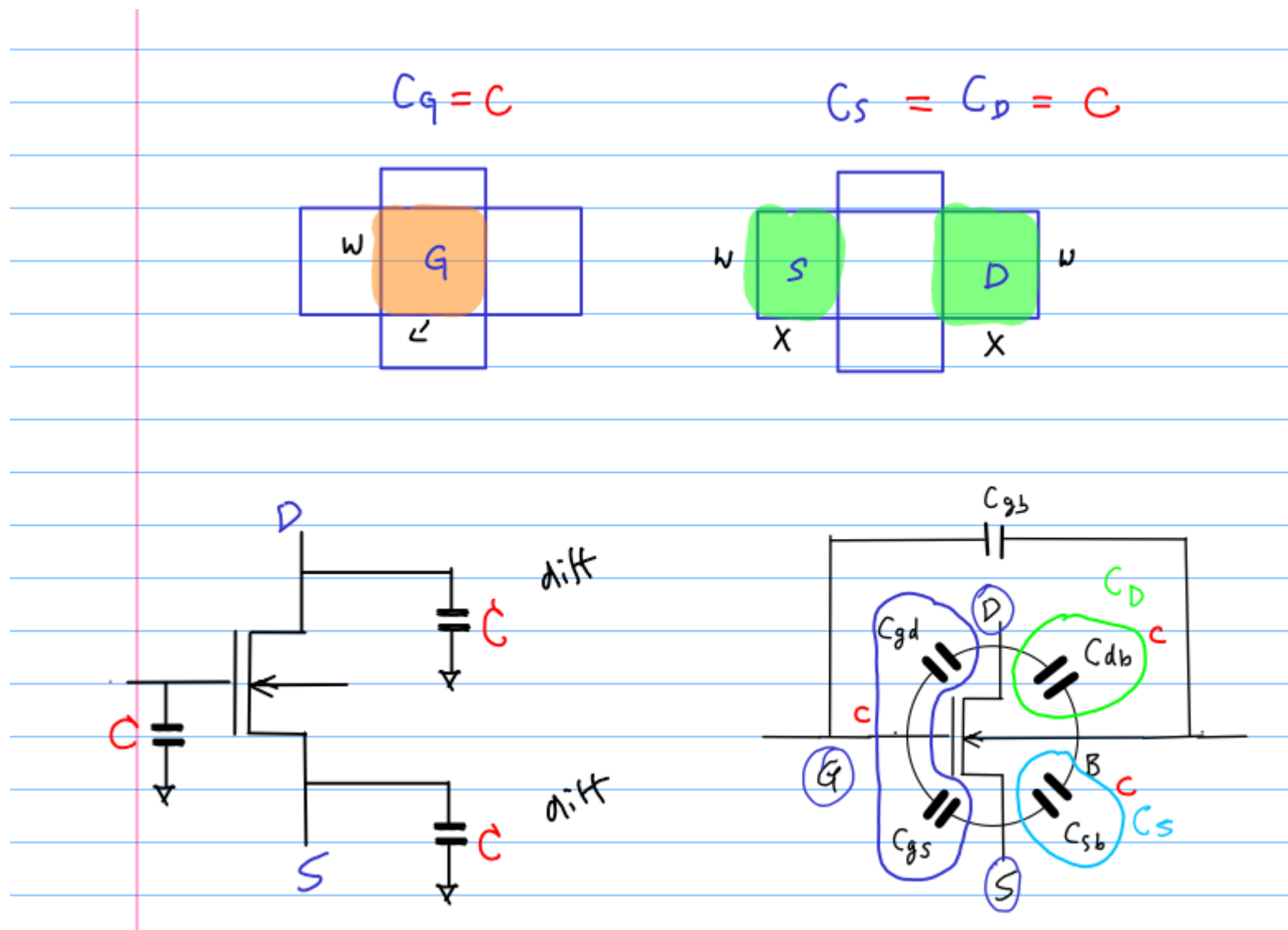
sidewall

bottom

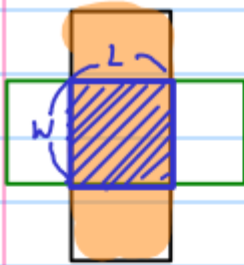
$C_{sw}$

$C_{bot}$

# Assume all the same cap (for hand calculation)



# Equal Size

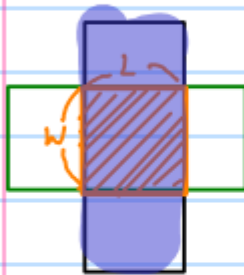


a unit nMOS

effective resistance  $(R)$

with minimum size

min  $W$  & min  $L$



a unit pMOS

effective resistance  $(2R)$

with minimum size

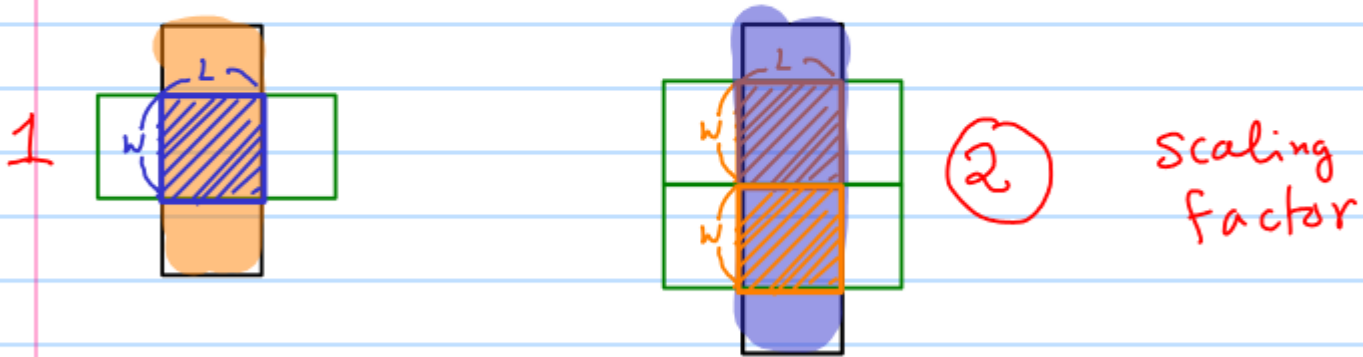
min  $W$  & min  $L$

	$V_{DD} = 5V$	$V_{DD} = 3.3V$
$R_{n, \text{unit}}$	$3.9 \text{ k}\Omega$	$6.8 \text{ k}\Omega$
$R_{p, \text{unit}}$	$14 \text{ k}\Omega$	$25 \text{ k}\Omega$



# Equal Resistance

	$V_{DD} = 5V$	$V_{DD} = 3.3V$
$R_{n, unit}$	$3.9 k\Omega$	$6.8 k\Omega$
$R_{p, unit}$	$14 k\Omega$	$25 k\Omega$



$$R_n \approx R_p$$

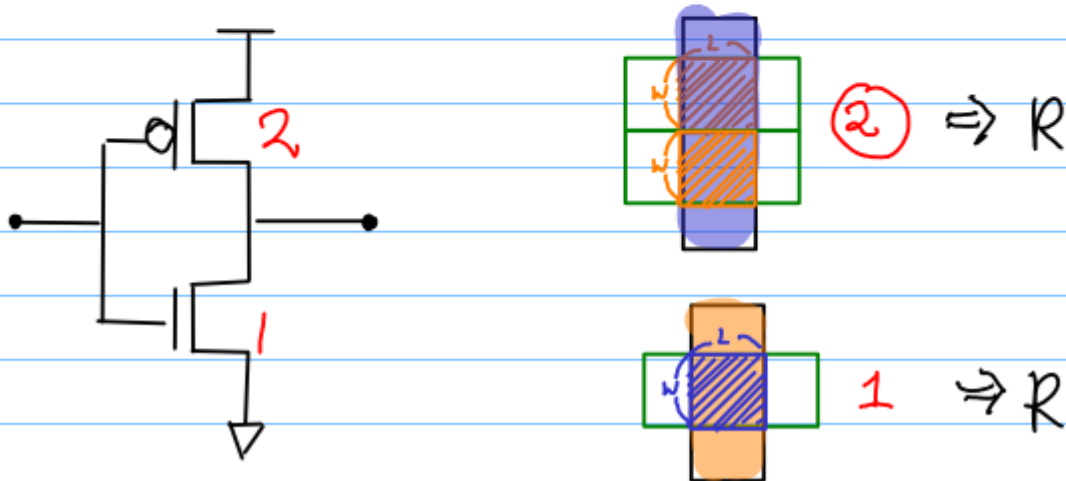
# A Unit Inverter

X1 reference gate

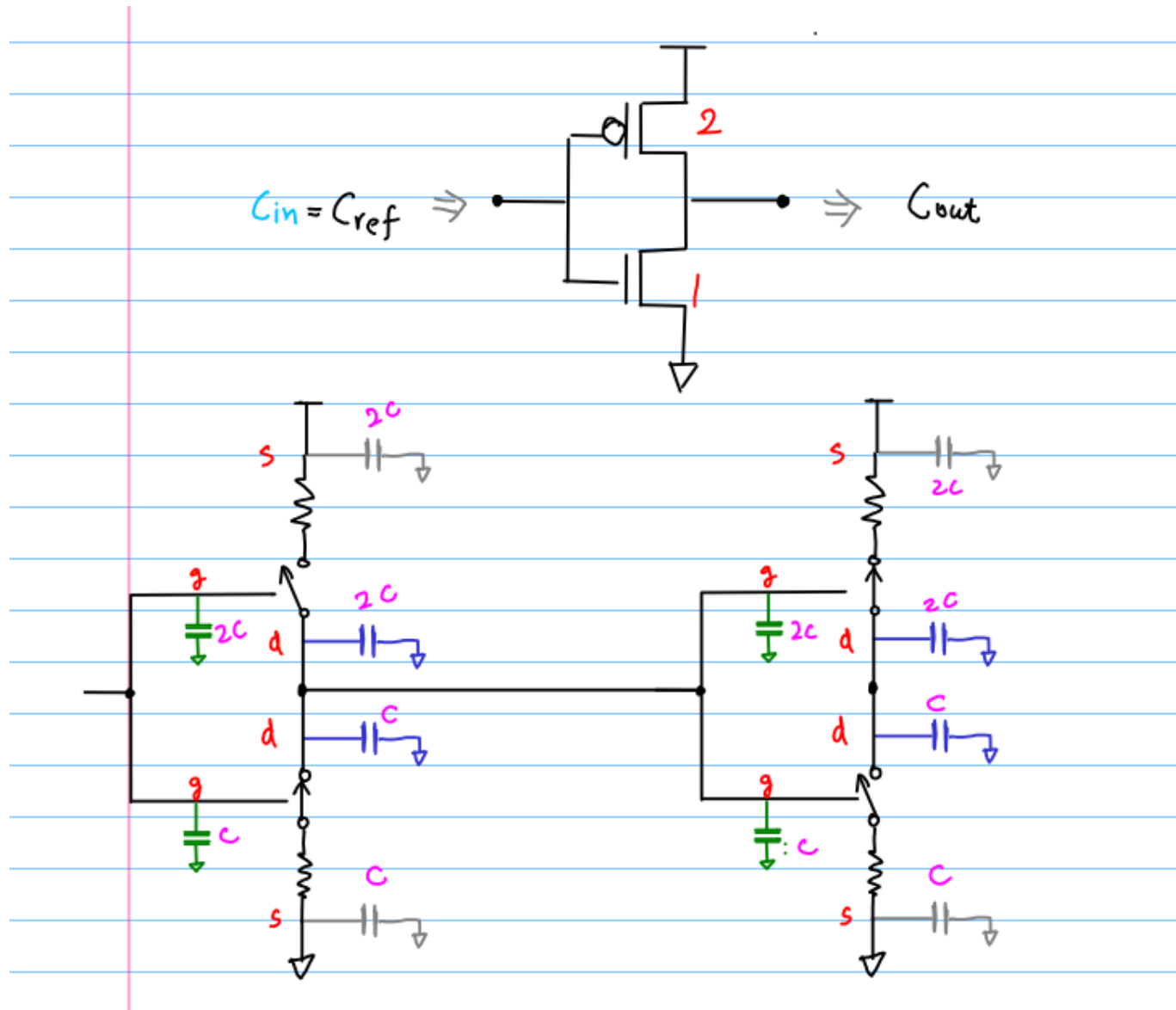
a symmetric inverter

$$\beta_n = \beta_p$$

$$R_n = R_p$$



# Cascade Inverter Modeling



# Characteristic Curve

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## References

- [1] <http://en.wikipedia.org/>
- [2] <http://www.allaboutcircuits.com/>
- [3] W. Wolf, "Modern VLSI Design : Systems on Silicon"
- [4] N. Weste, D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective"
- [5] J. P. Uyemura, "Introduction to VLSI Circuits and Systems"
- [6] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_SOC\\_Design](https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design)
- [7] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_Digital\\_Design](https://en.wikiversity.org/wiki/The_necessities_in_Digital_Design)
- [8] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_Computer\\_Design](https://en.wikiversity.org/wiki/The_necessities_in_Computer_Design)
- [9] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_Computer\\_Architecture](https://en.wikiversity.org/wiki/The_necessities_in_Computer_Architecture)
- [10] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_Computer\\_Organization](https://en.wikiversity.org/wiki/The_necessities_in_Computer_Organization)
- [11] [https://en.wikiversity.org/wiki/Verilog\\_programming\\_in\\_plain\\_view](https://en.wikiversity.org/wiki/Verilog_programming_in_plain_view)