

Endian

Copyright (c) 2013 Young W. Lim.

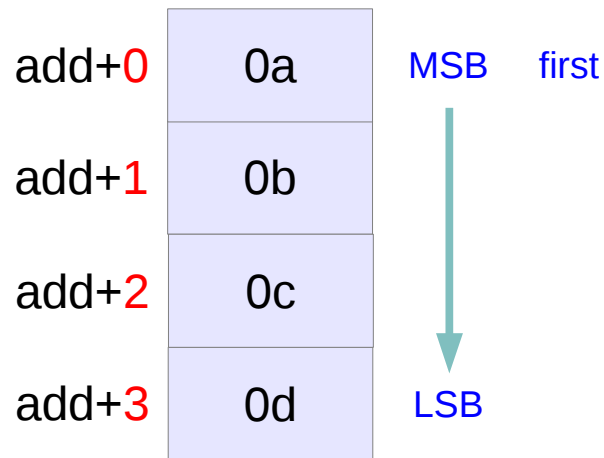
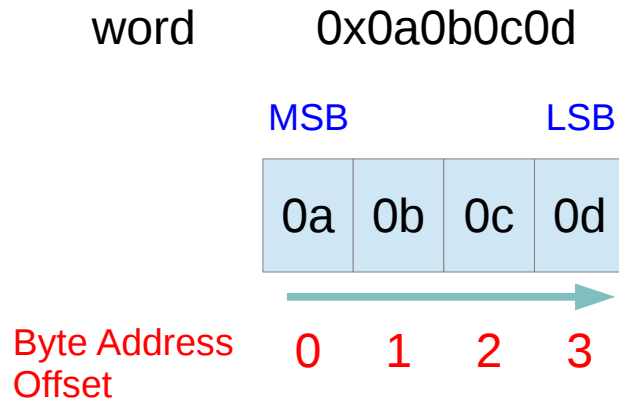
Permission is granted to copy, distribute and/or modify this document under the terms of the GNU Free Documentation License, Version 1.2 or any later version published by the Free Software Foundation; with no Invariant Sections, no Front-Cover Texts, and no Back-Cover Texts. A copy of the license is included in the section entitled "GNU Free Documentation License".

Please send corrections (or suggestions) to youngwlim@hotmail.com.

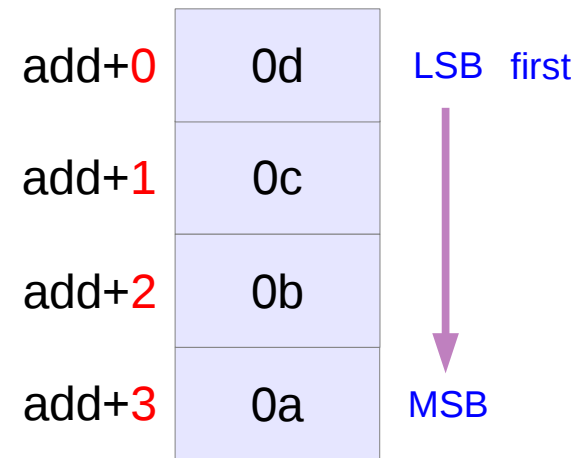
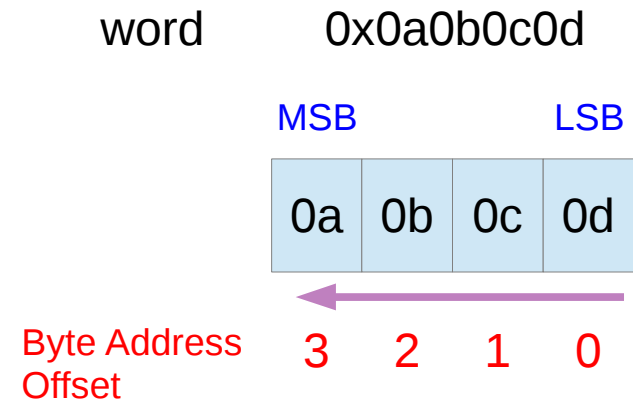
This document was produced by using OpenOffice and Octave.

Byte Order

Big Endian



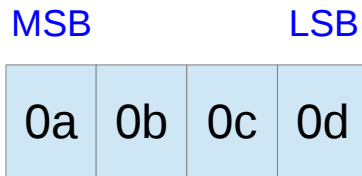
Little Endian



Byte Order in a Memory

Big Endian

word 0x0a0b0c0d



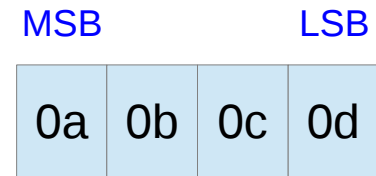
Byte Address
Offset

0 1 2 3

^c 40	^d f3	^e 07	^f 88
⁸ 01	⁹ ef	^a 28	^b 42
⁴ f2	⁵ f1	⁶ ac	⁷ 07
⁰ 0a	¹ 0b	² 0c	³ 0d

Little Endian

word 0x0a0b0c0d



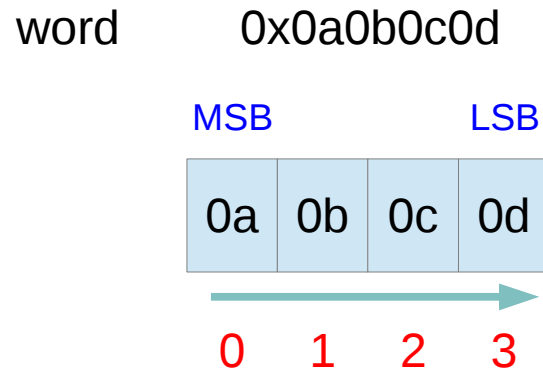
Byte Address
Offset

3 2 1 0

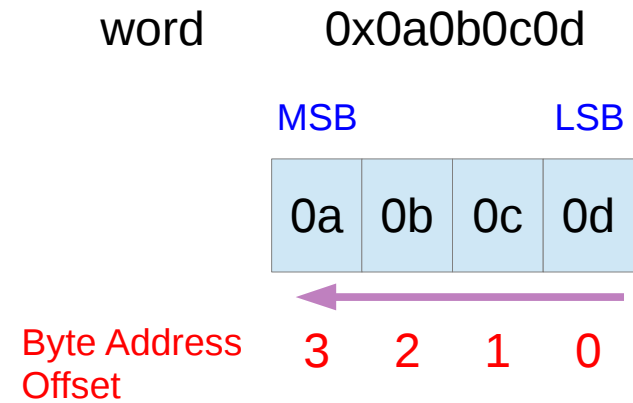
^e 40	^e f3	^d 07	^c 88
^b 01	^a ef	⁹ 28	⁸ 42
⁷ f2	⁶ f1	⁵ ac	⁴ 07
³ 0a	² 0b	¹ 0c	⁰ 0d

Bit Numbering

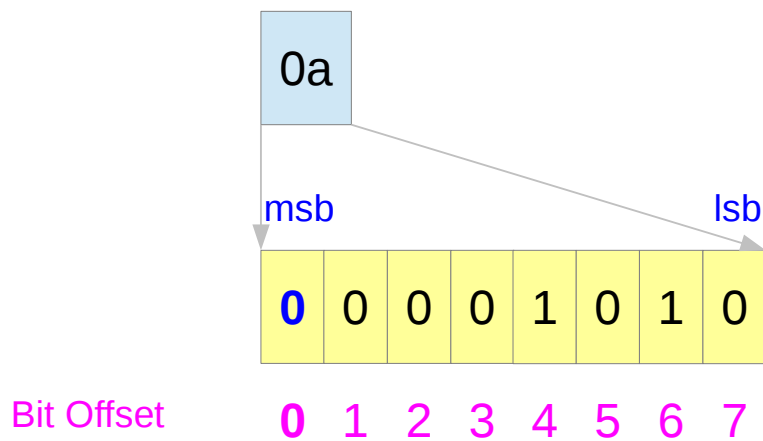
Big Endian



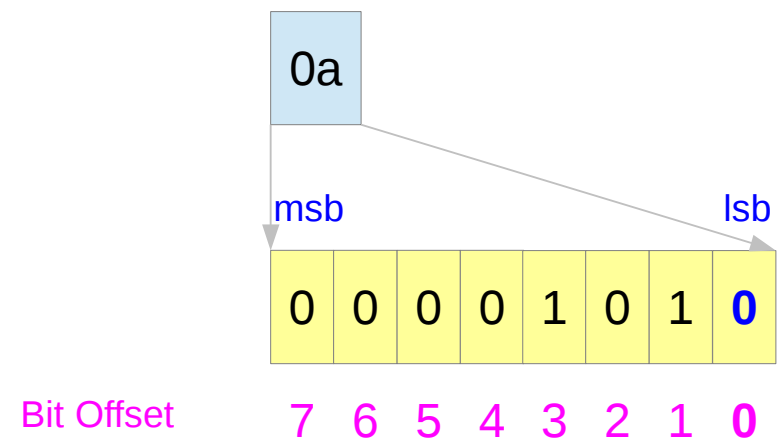
Little Endian



msb 0 numbering



lsb 0 numbering



Example

Big Endian

	0a	0b	0c	0d
	00001010	00001011	00001100	00001101
Bit Offset	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
Byte Address Offset	0	1	2	3

Network Byte Order $W[0:31]$

Host Byte Order $W[31:0]$

Little Endian

	0a	0b	0c	0d
	00001010	00001011	00001100	00001101
Bit Offset	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Byte Address Offset	3	2	1	0

CPU Endian Usage

- Little endian CPUs include Intel and DEC.
- Big endian CPUs include Motorola 680x0, Sun Sparc and IBM (e.g., PowerPC).
- MIPS and ARM can be configured either way.

References

- [1] <http://en.wikipedia.org/>
- [2] D.M. Harris, S. L. Harris, "Digital Design and Computer Architecture"
- [3] <http://www.linuxjournal.com/node/6788/print>