

Pipeline (5D)

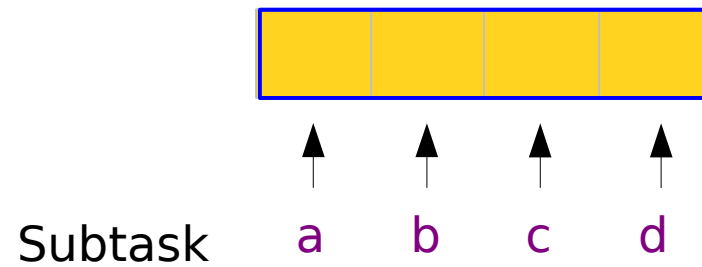
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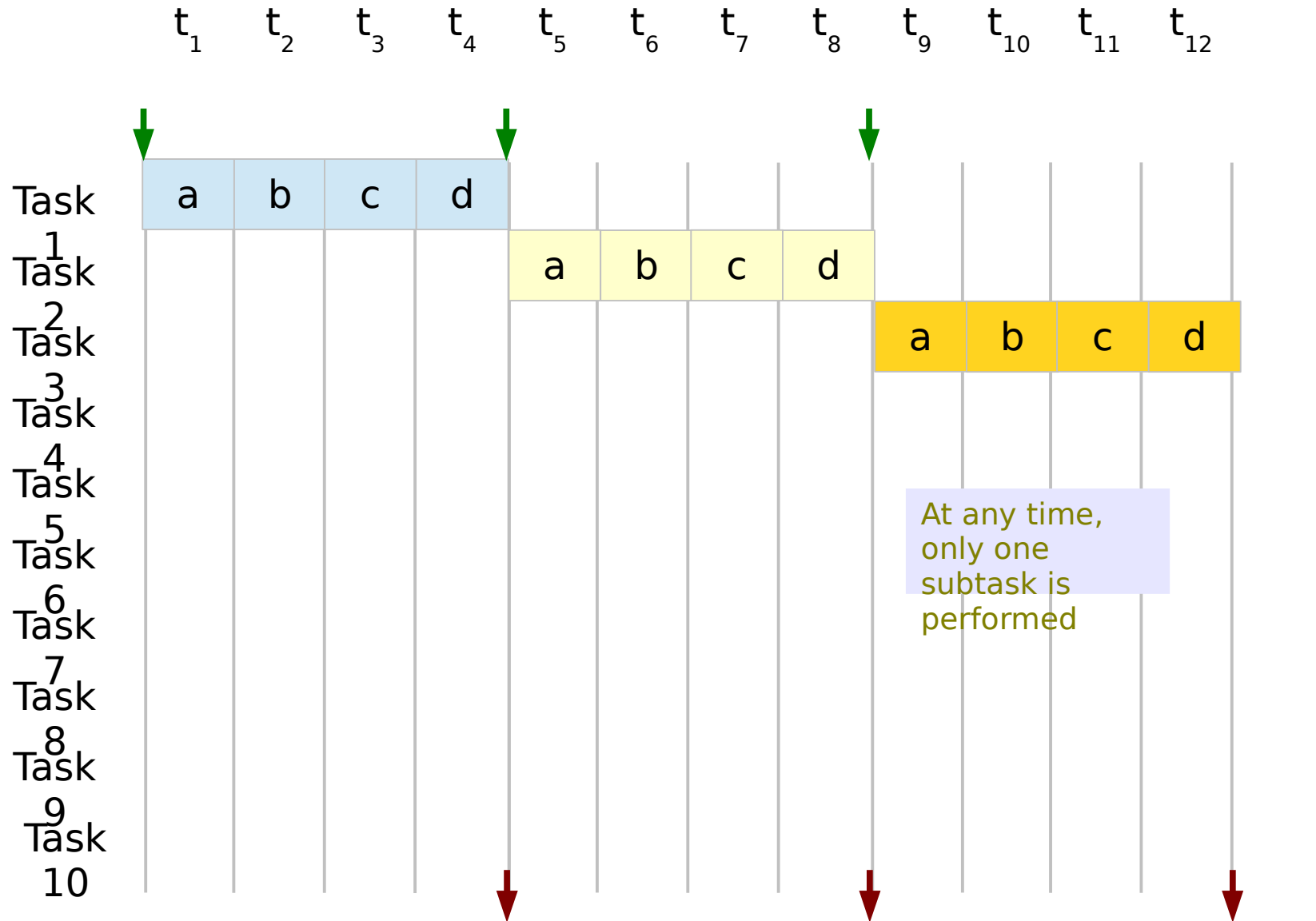
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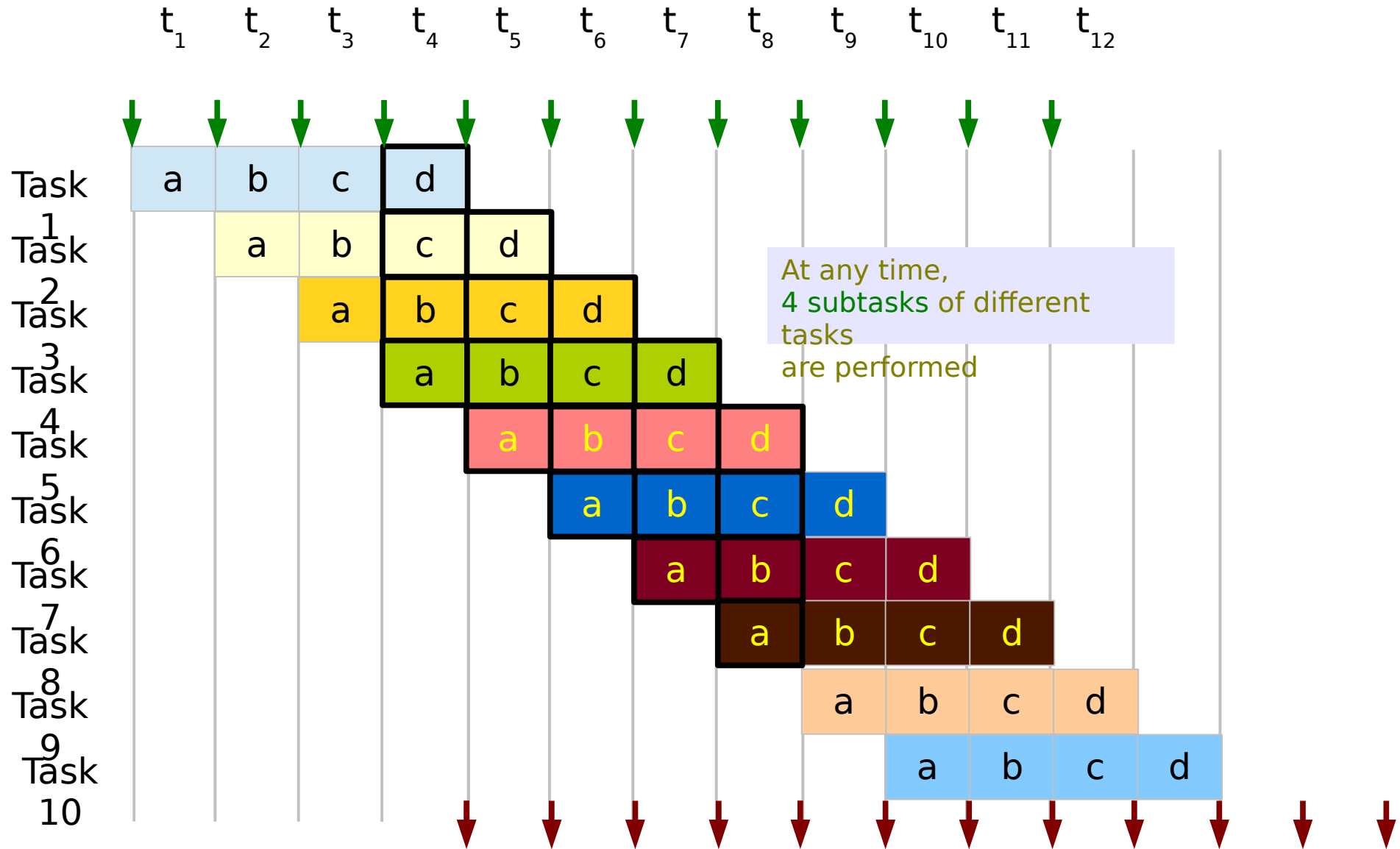
Tasks and Subtasks



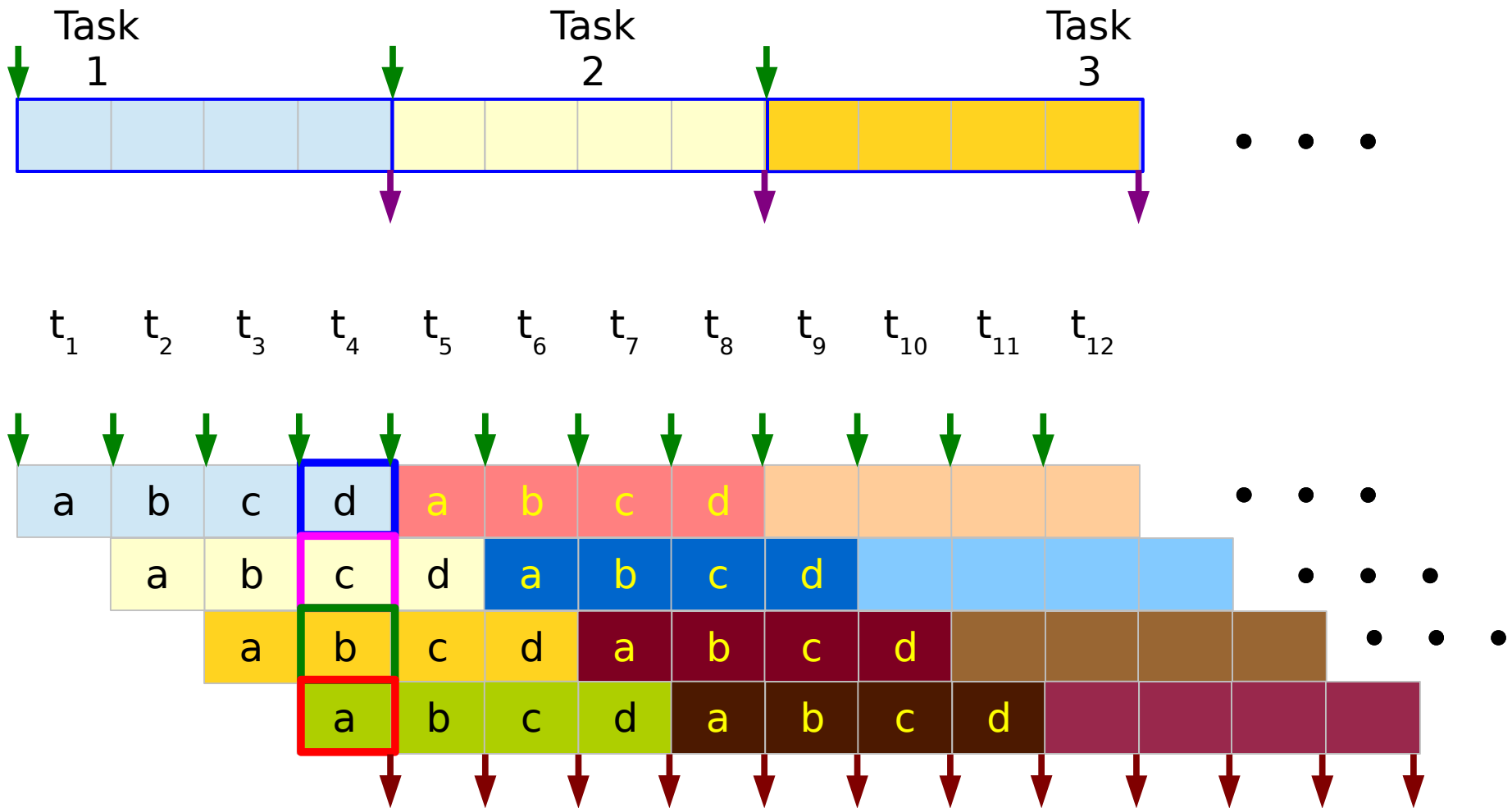
Task vs Time View (1)



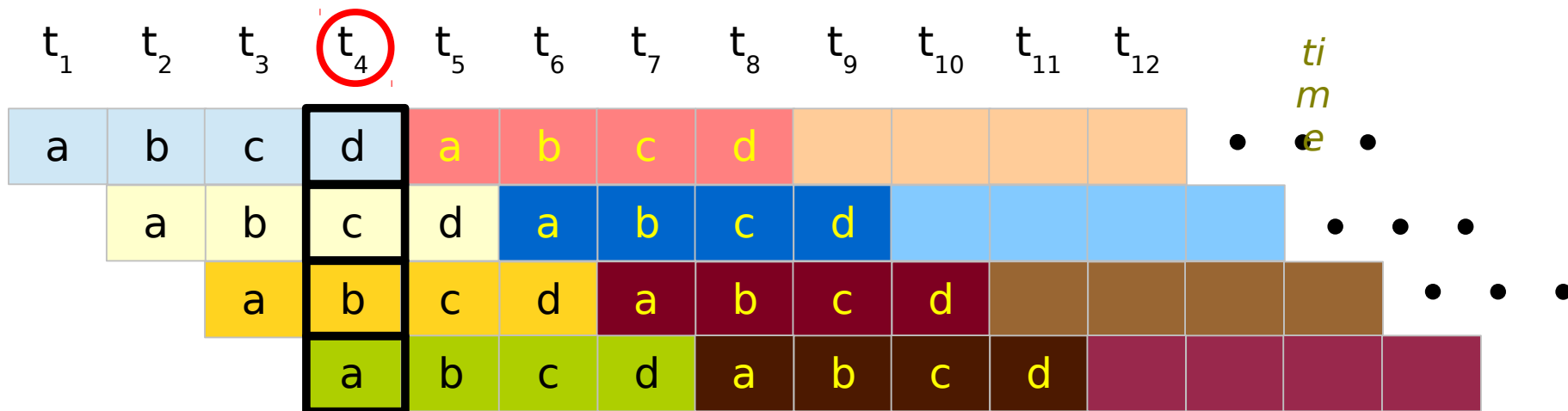
Task vs Time View (2)



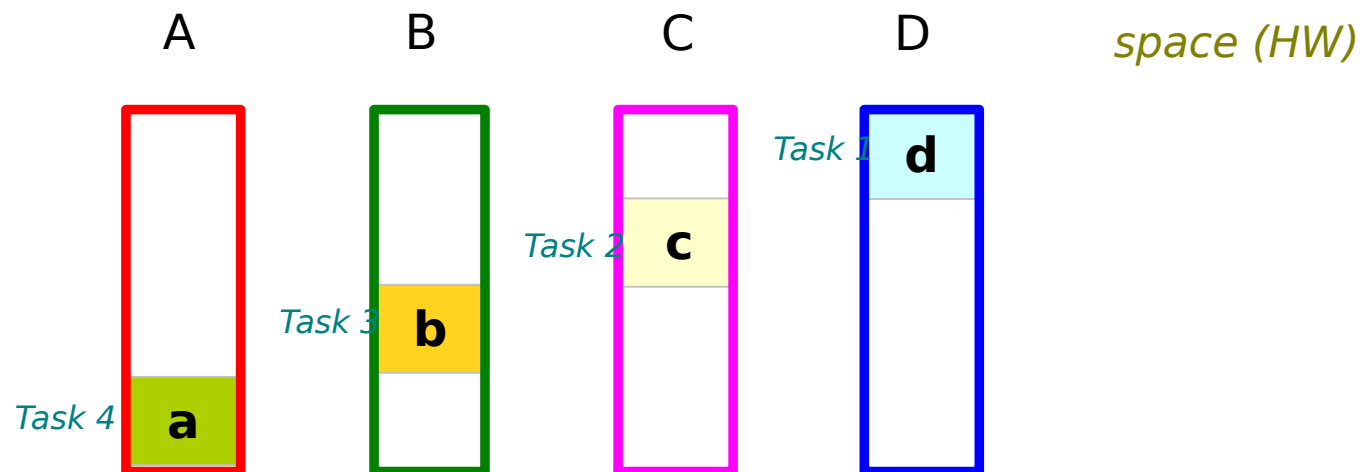
Compact Task vs Time View



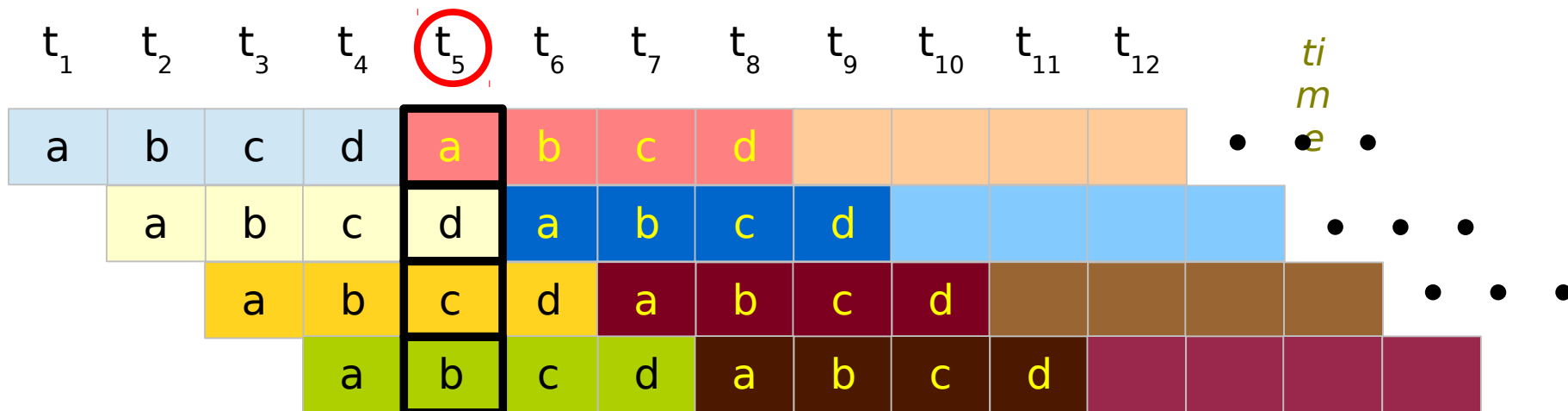
The Subtask Snapshot At time t_4



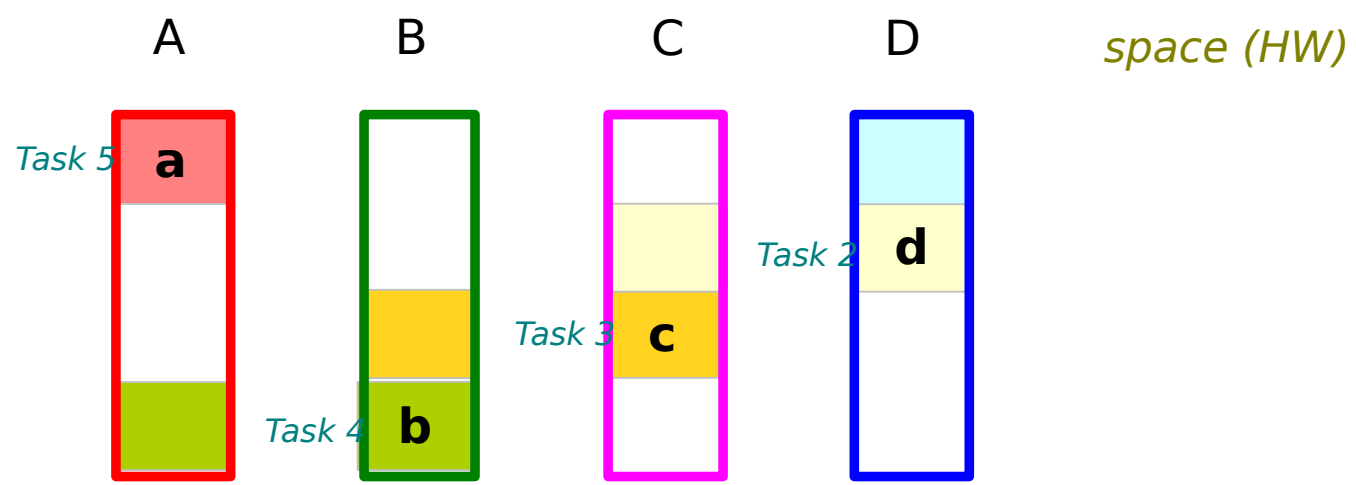
The subtask snapshot at time t_4



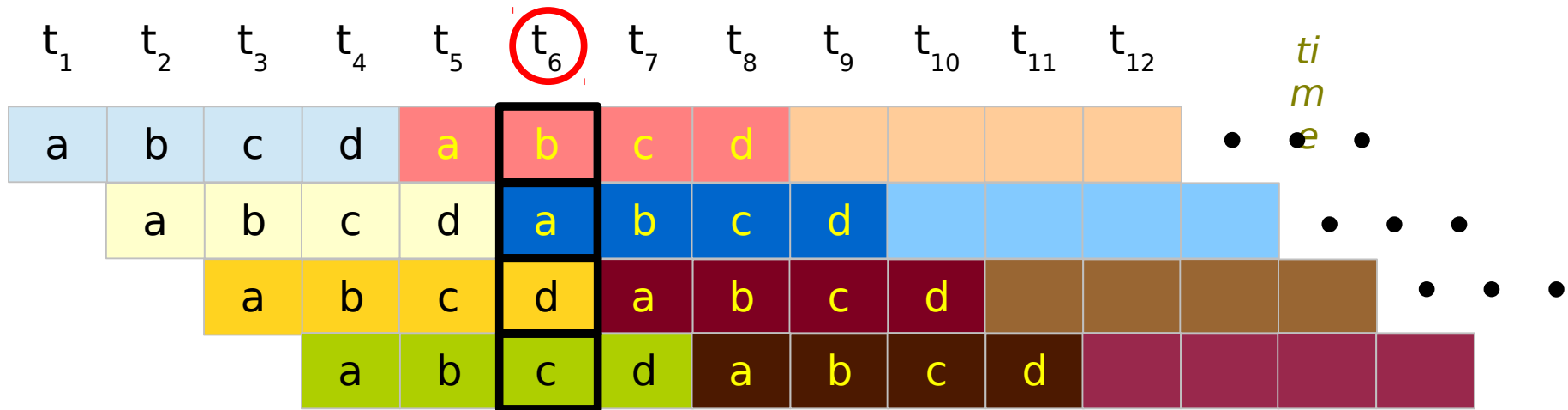
The Subtask Snapshot At time t_5



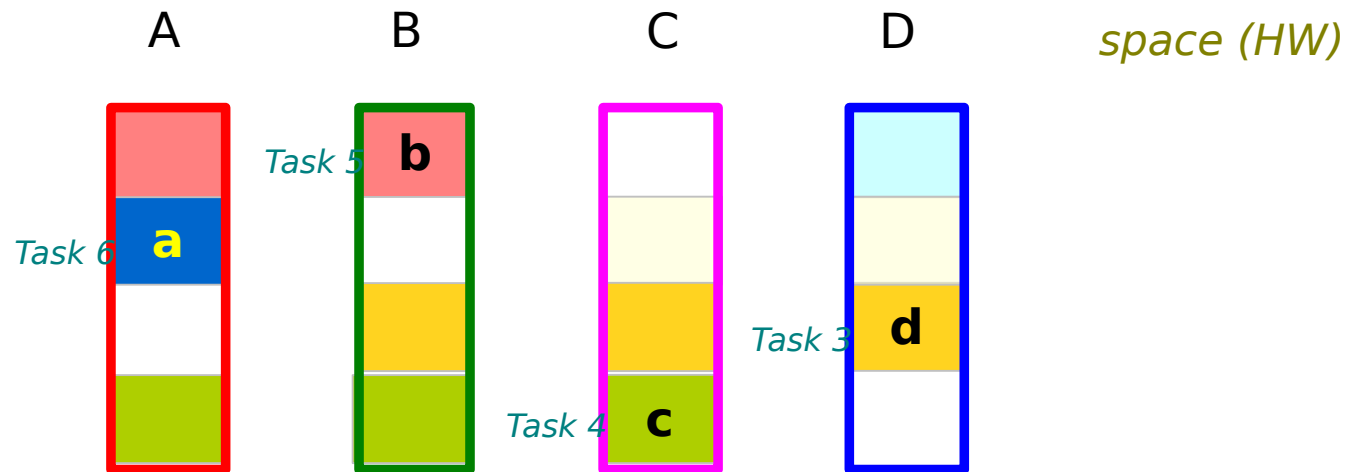
The subtask snapshot at time t_5



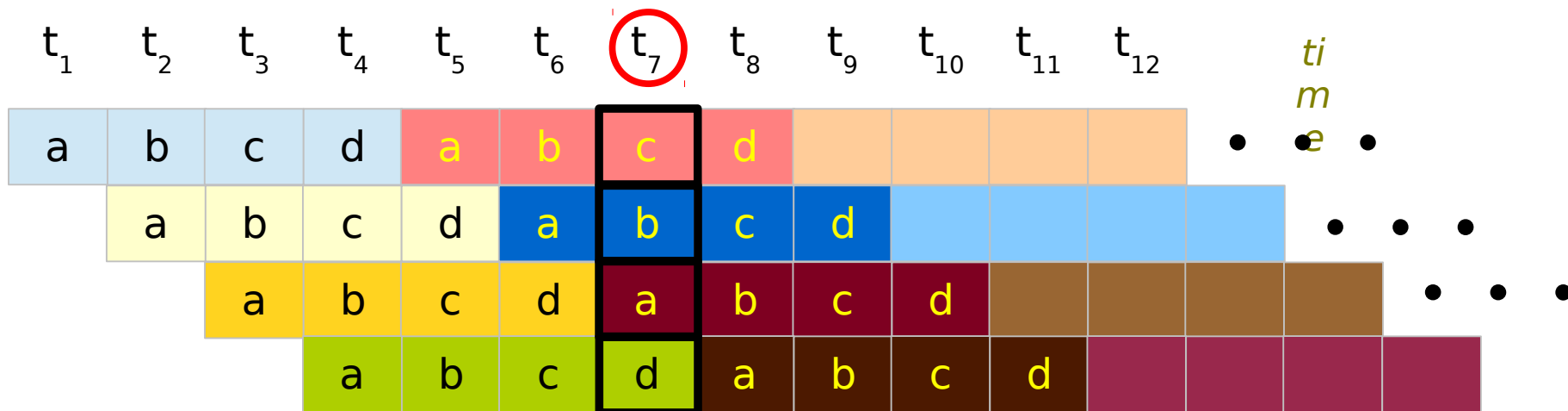
The Subtask Snapshot At time t_6



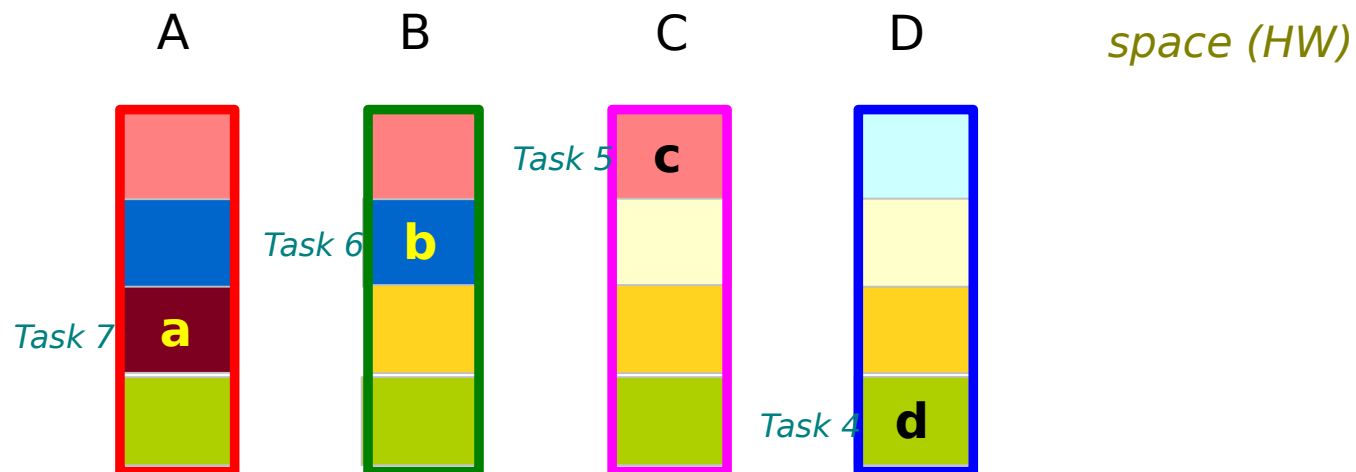
The subtask snapshot at time t_6



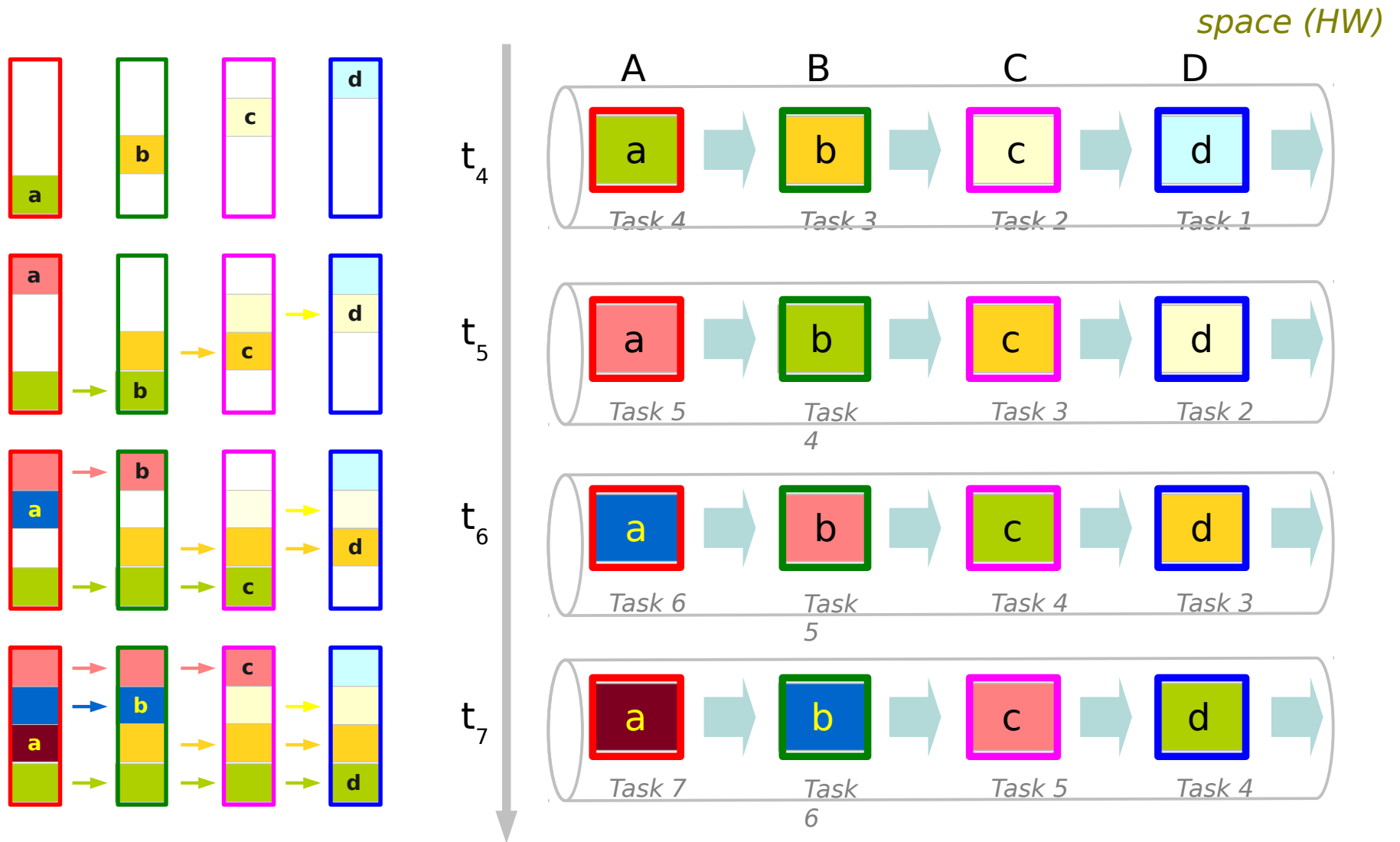
The Subtask Snapshot At time t_7



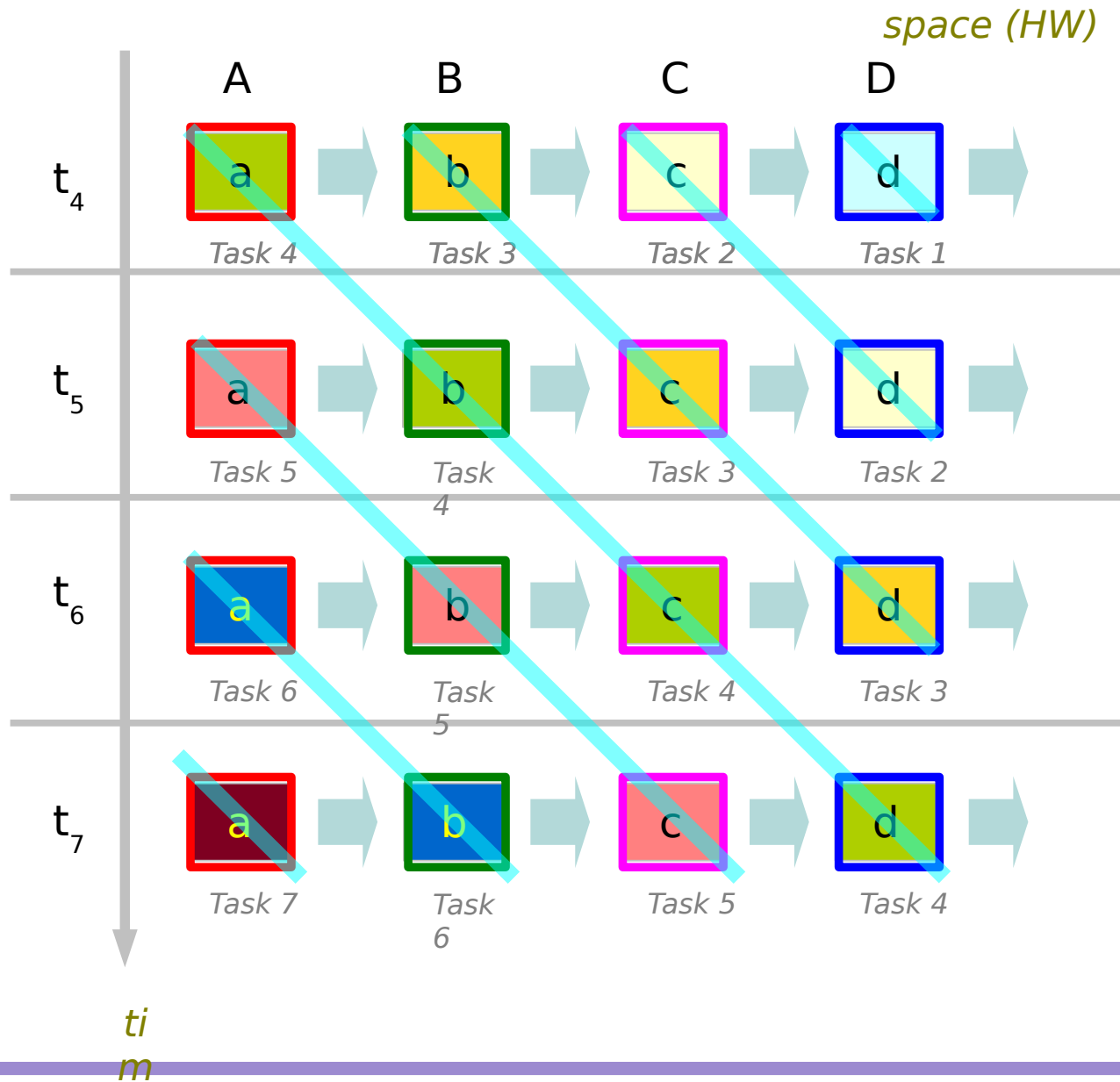
The subtask snapshot at time t_7



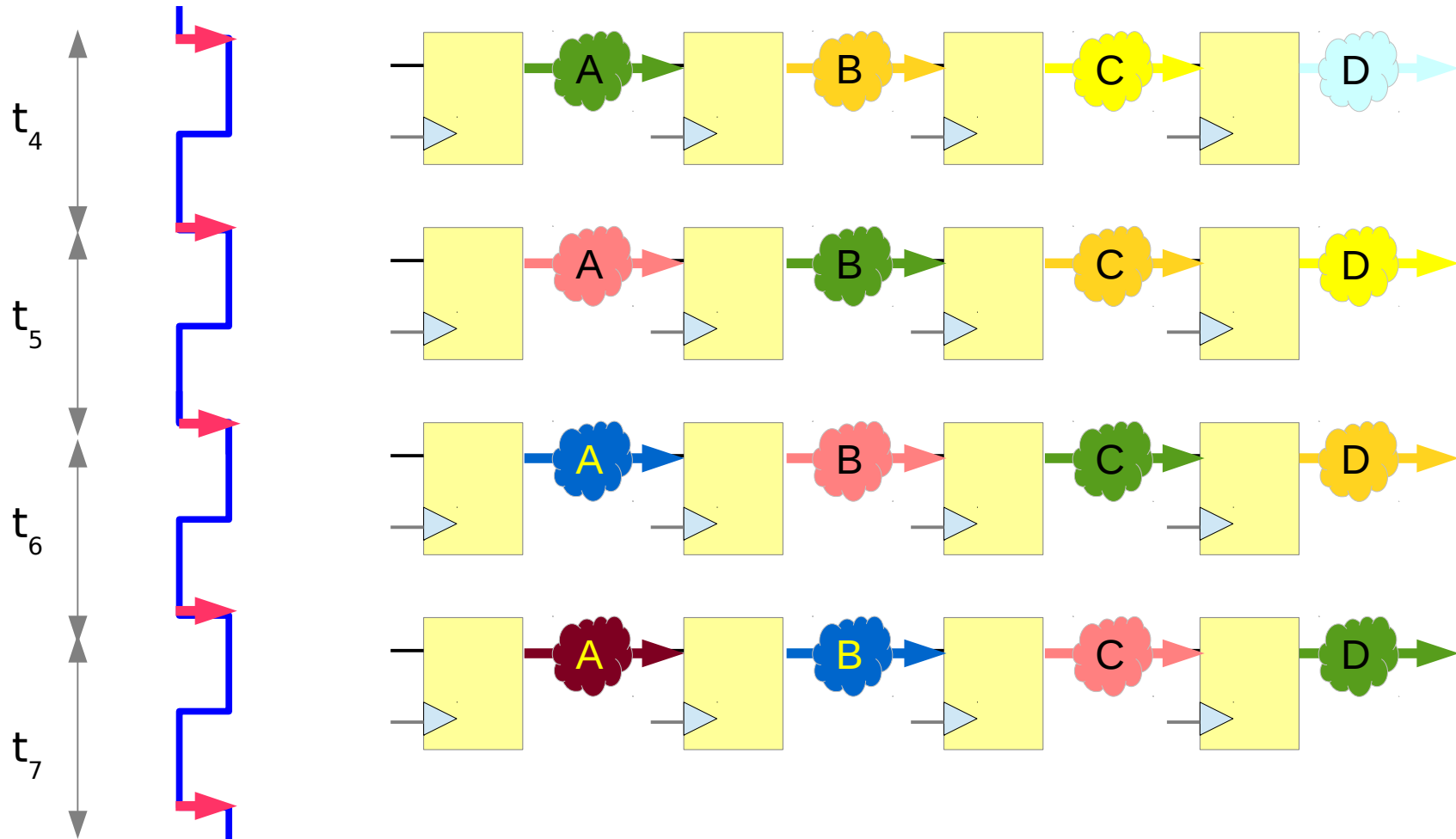
Time vs Subtask View (1)



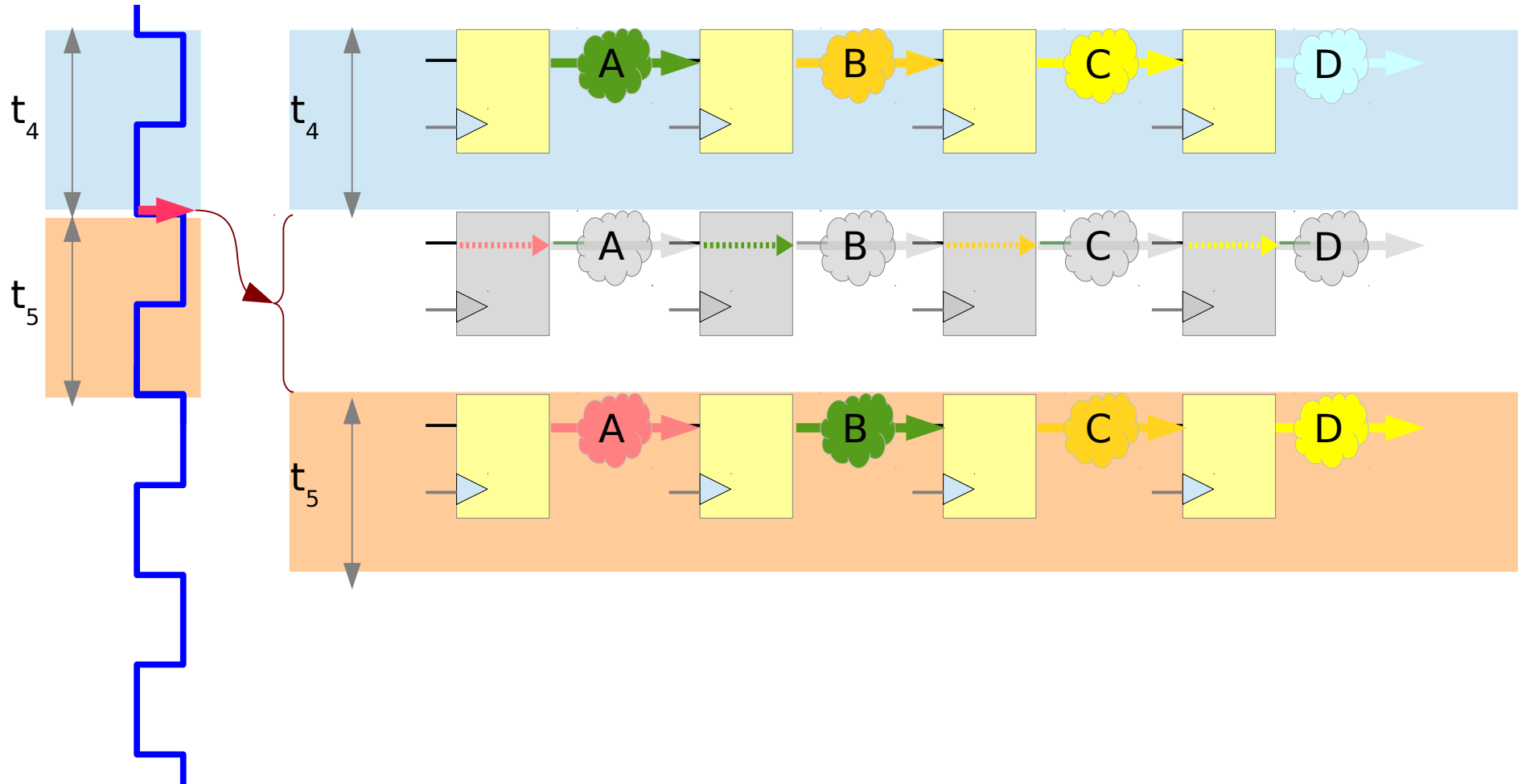
Time vs Subtask View (2)



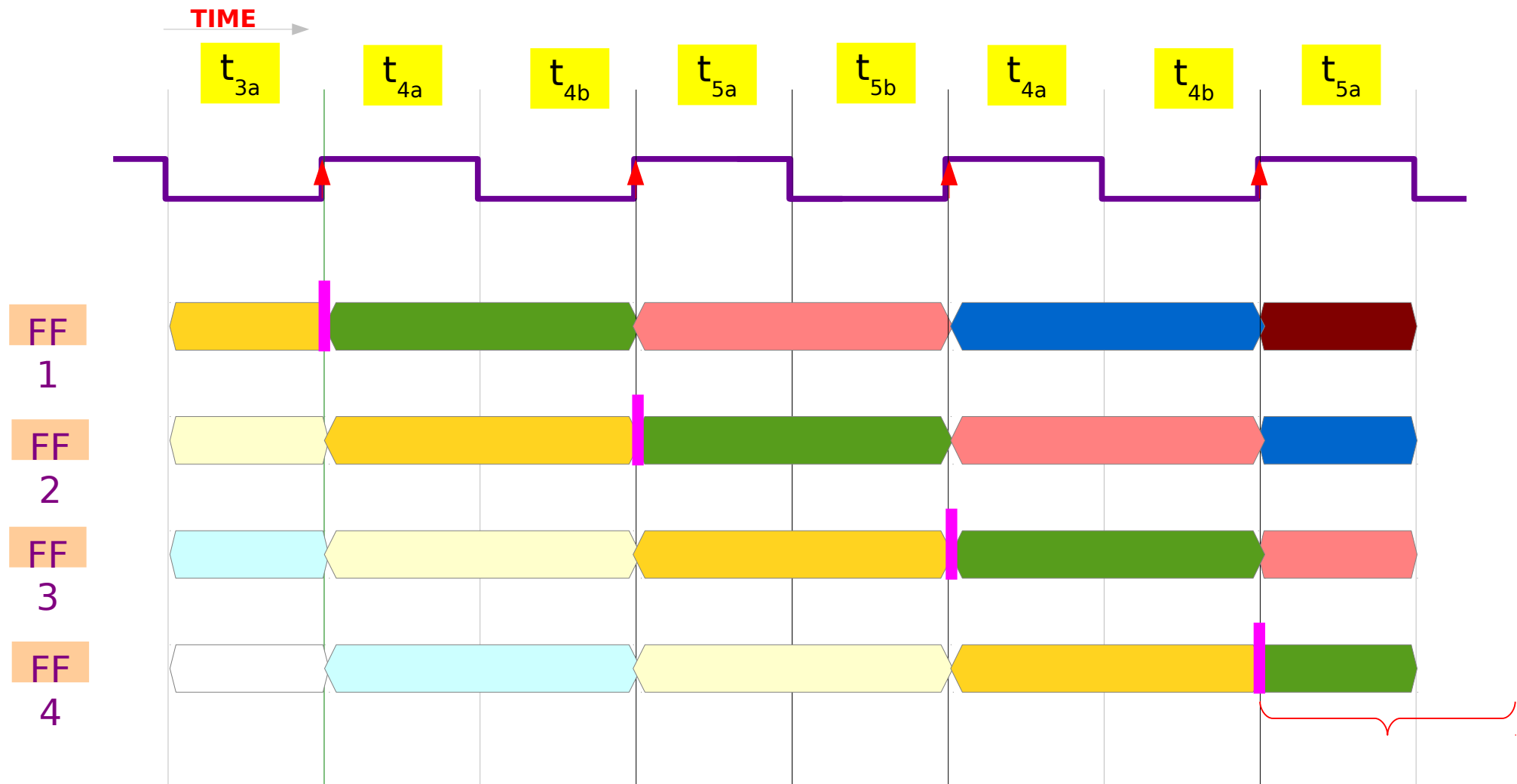
FlipFlop Based Pipeline (1)



FlipFlop Based Pipeline (2)

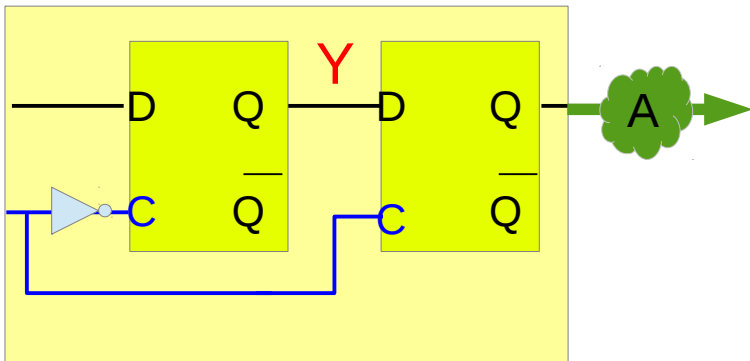
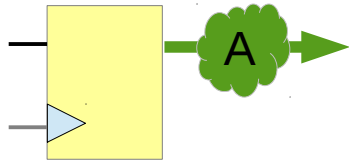


The FlipFlop Timing

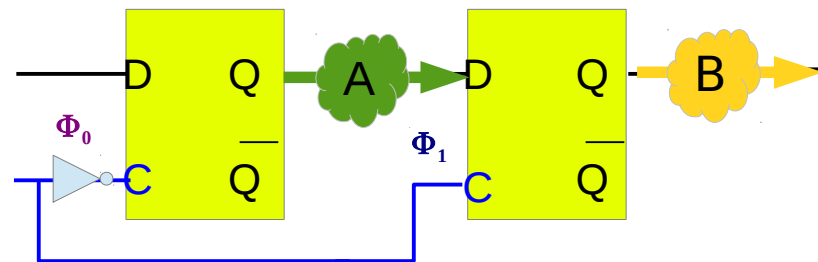
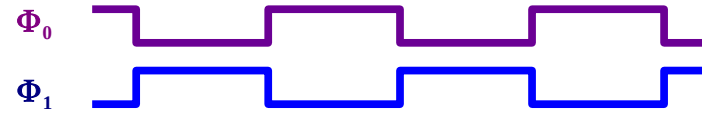
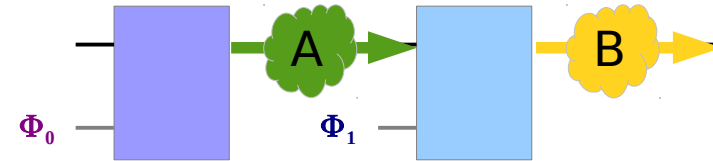


FlipFlops and Latches

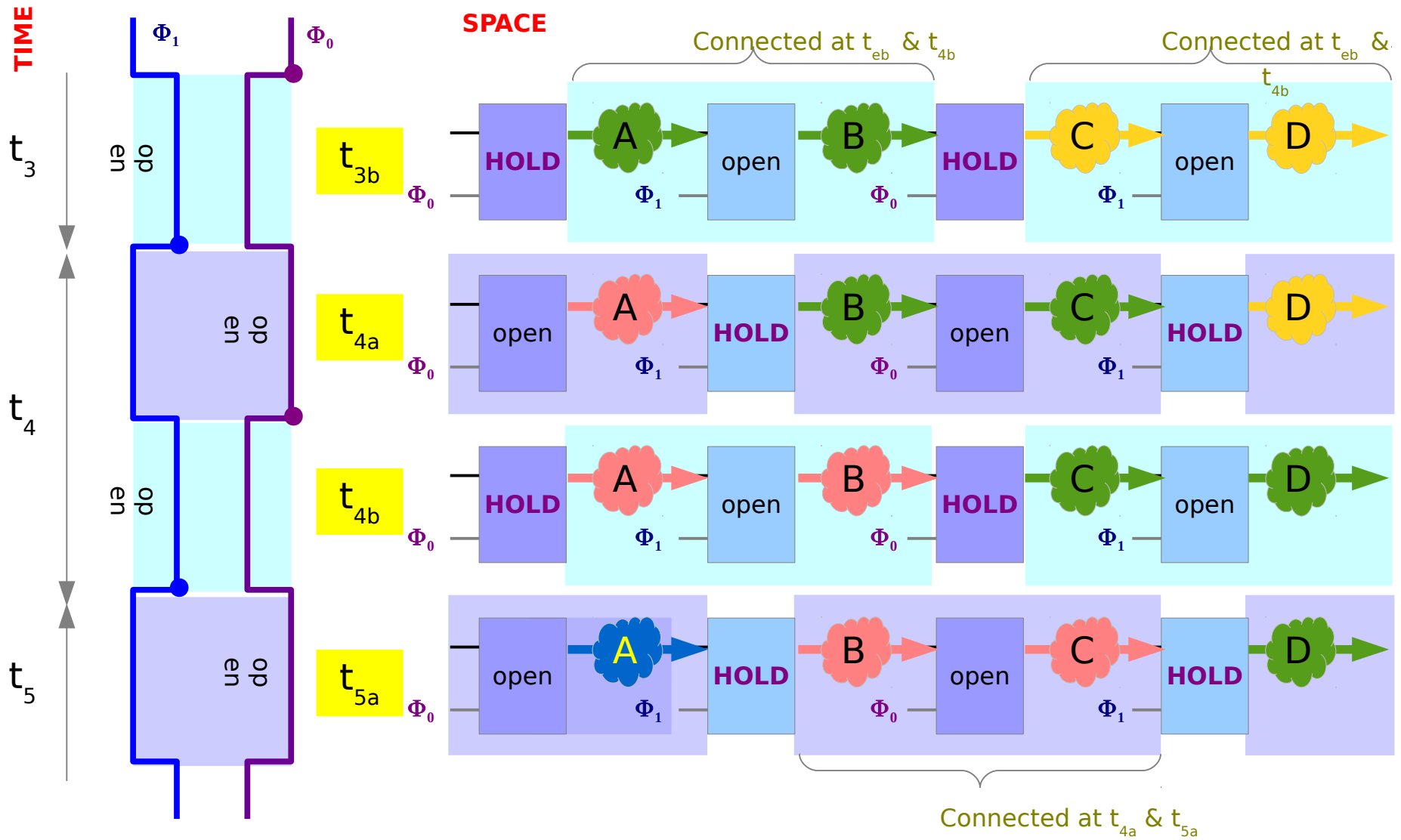
D Type Master-Slave Flipflop



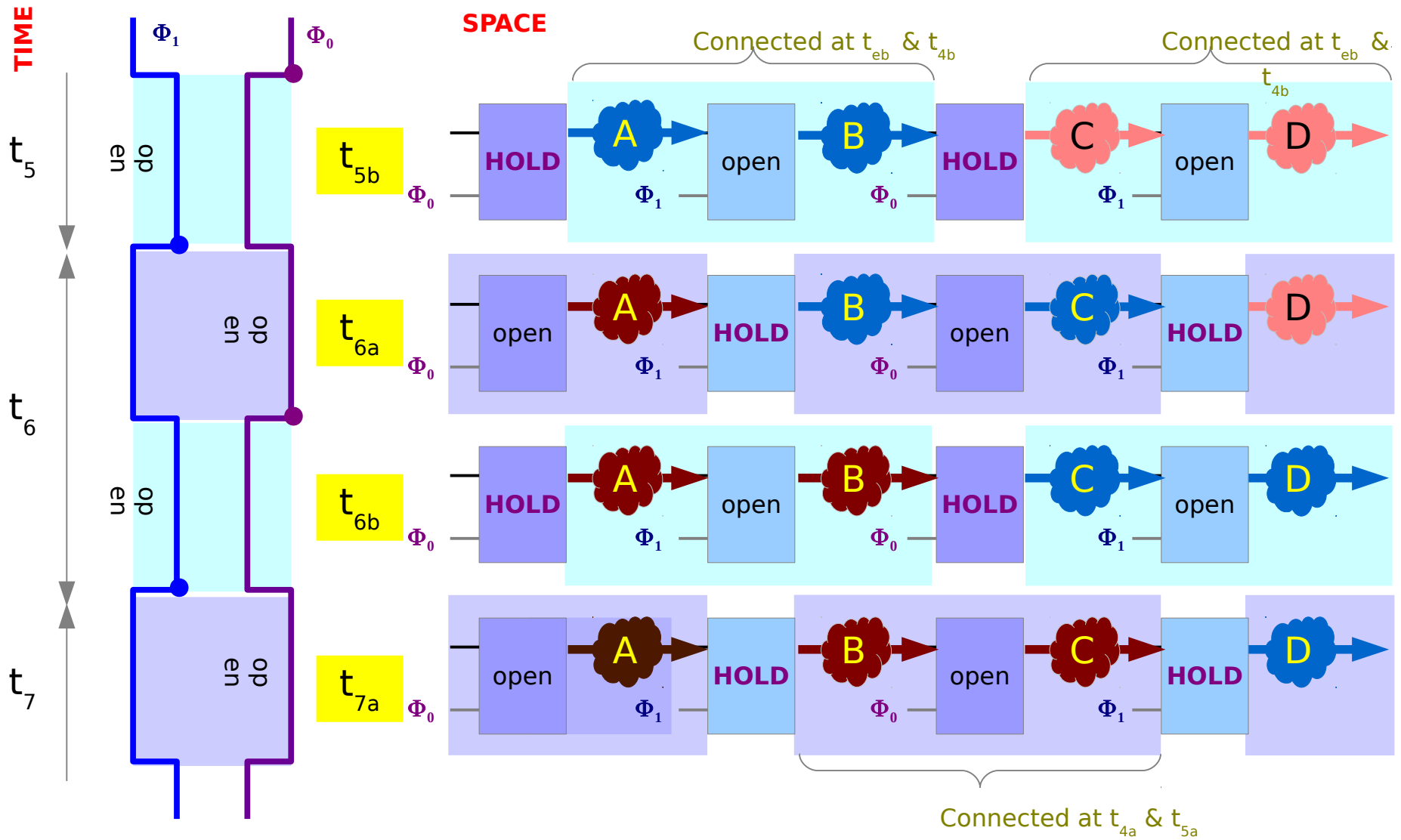
D Type Latches in series



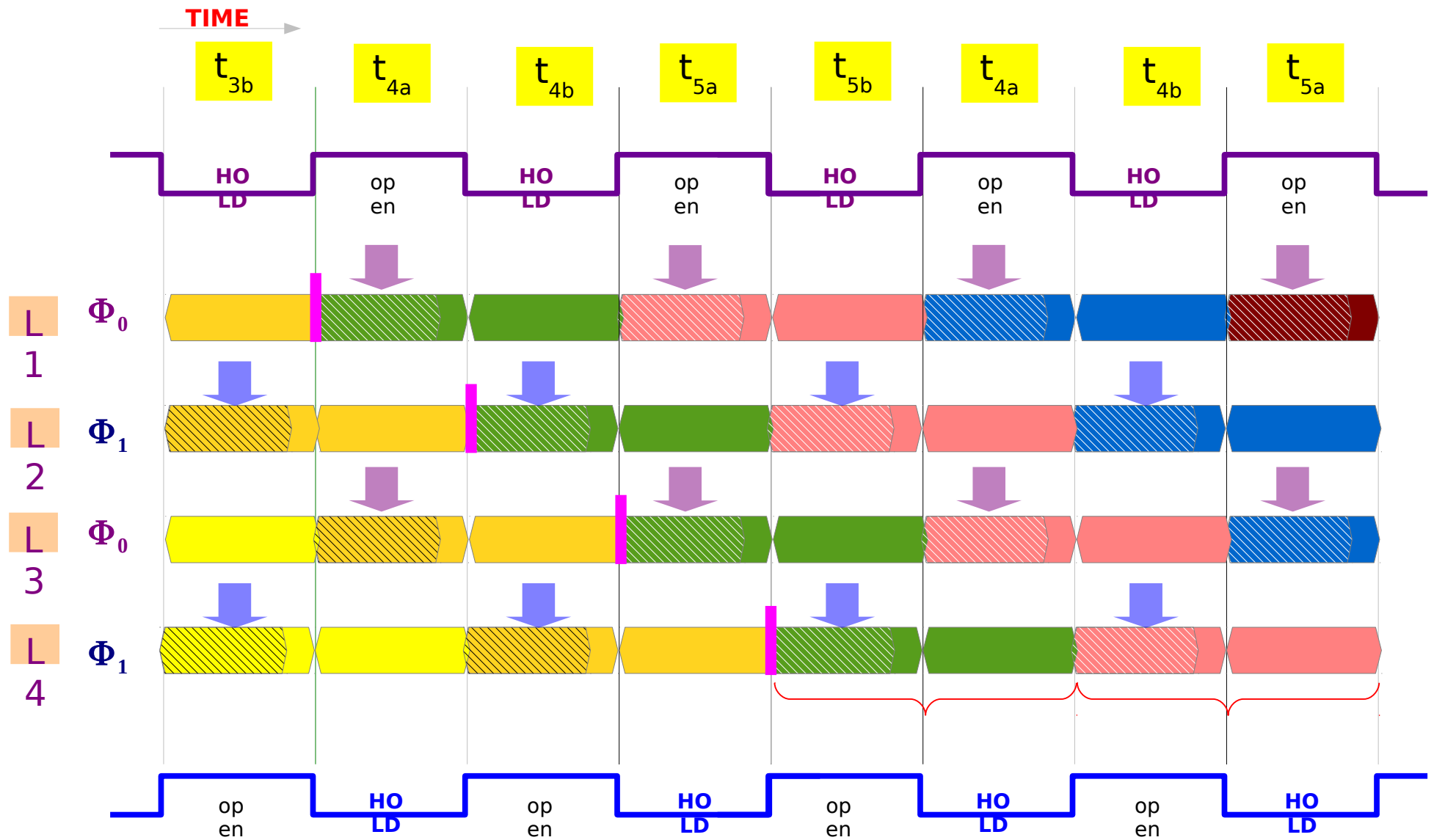
Latch Based Pipeline (1)



Latch Based Pipeline (2)



The Latch Timing



Register Timing

References

- [1] <http://en.wikipedia.org/>
- [2] <http://www.allaboutcircuits.com/>
- [3] W. Wolf, "Modern VLSI Design : Systems on Silicon"
- [4] N. Weste, D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective"
- [5] J. P. Uyemura, "Introduction to VLSI Circuits and Systems"
- [6] https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design
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