Combinational Gates (3A)

Transistor Level Design

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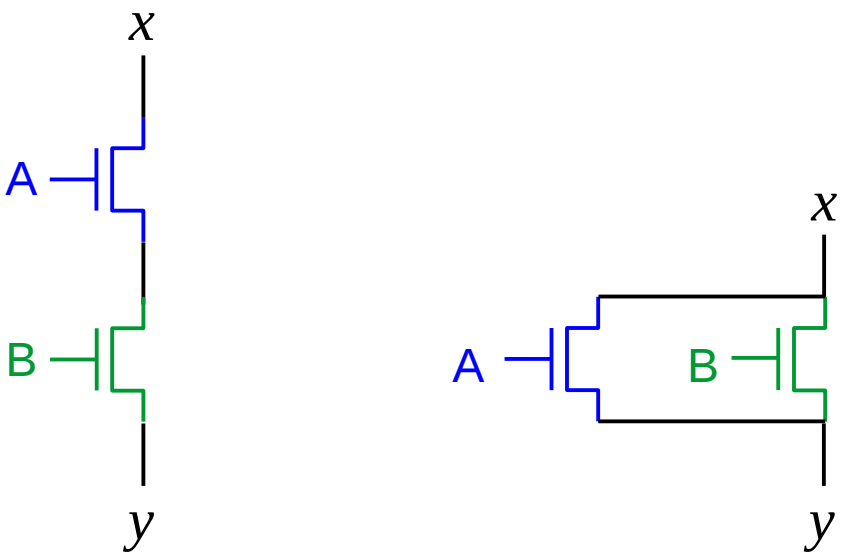
Please send corrections (or suggestions) to youngwlim@hotmail.com.

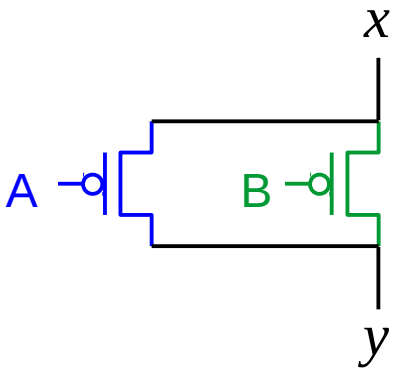
This document was produced by using OpenOffice and Octave.

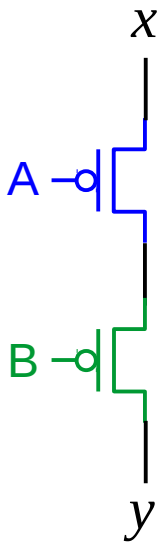
nMOS : series and parallel connections



$x = y \quad if \quad A \cdot B$ $\qquad$ $x = y \quad if \quad A + B$

pMOS : series and parallel connections





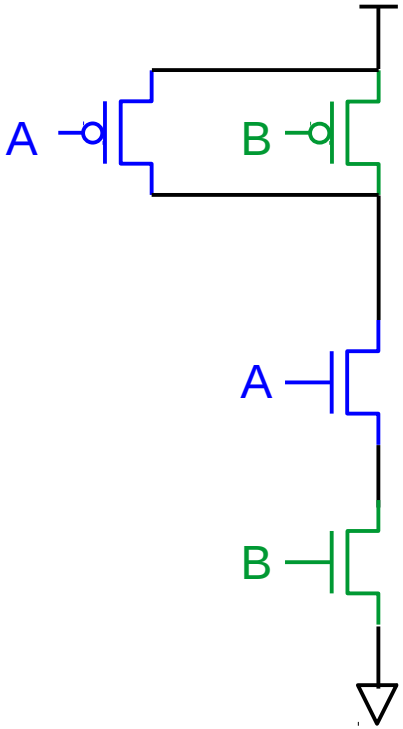
$$x = y \quad if \quad \overline{A} + \overline{B}$$

$$\overline{A \cdot B}$$

$$x = y \quad if \quad \overline{A} \cdot \overline{B}$$

$$\overline{A + B}$$

NAND Gate

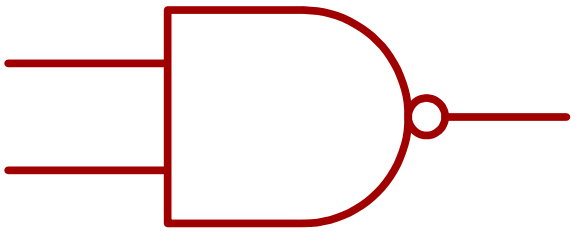


$G(\overline{A}, \overline{B}) = \overline{A} + \overline{B}$

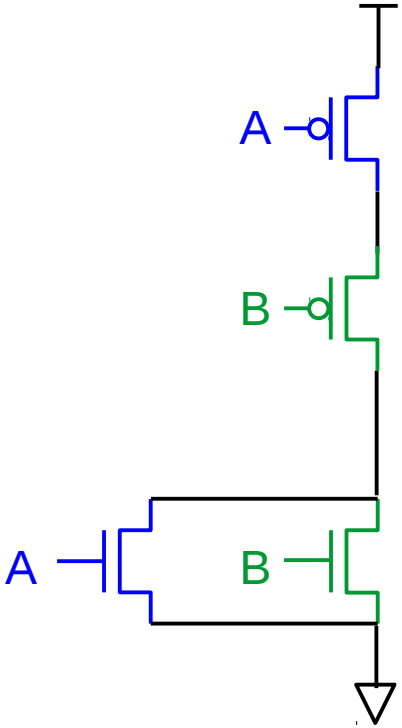
$F(A, B) = A \cdot B$

$$\overline{F(A, B)} = G(\overline{A}, \overline{B})$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$



NOR Gate

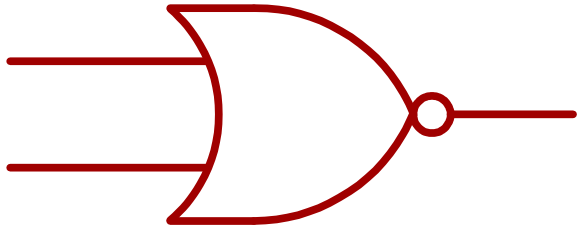


$$G(\overline{A}, \overline{B}) = \overline{A} \cdot \overline{B}$$

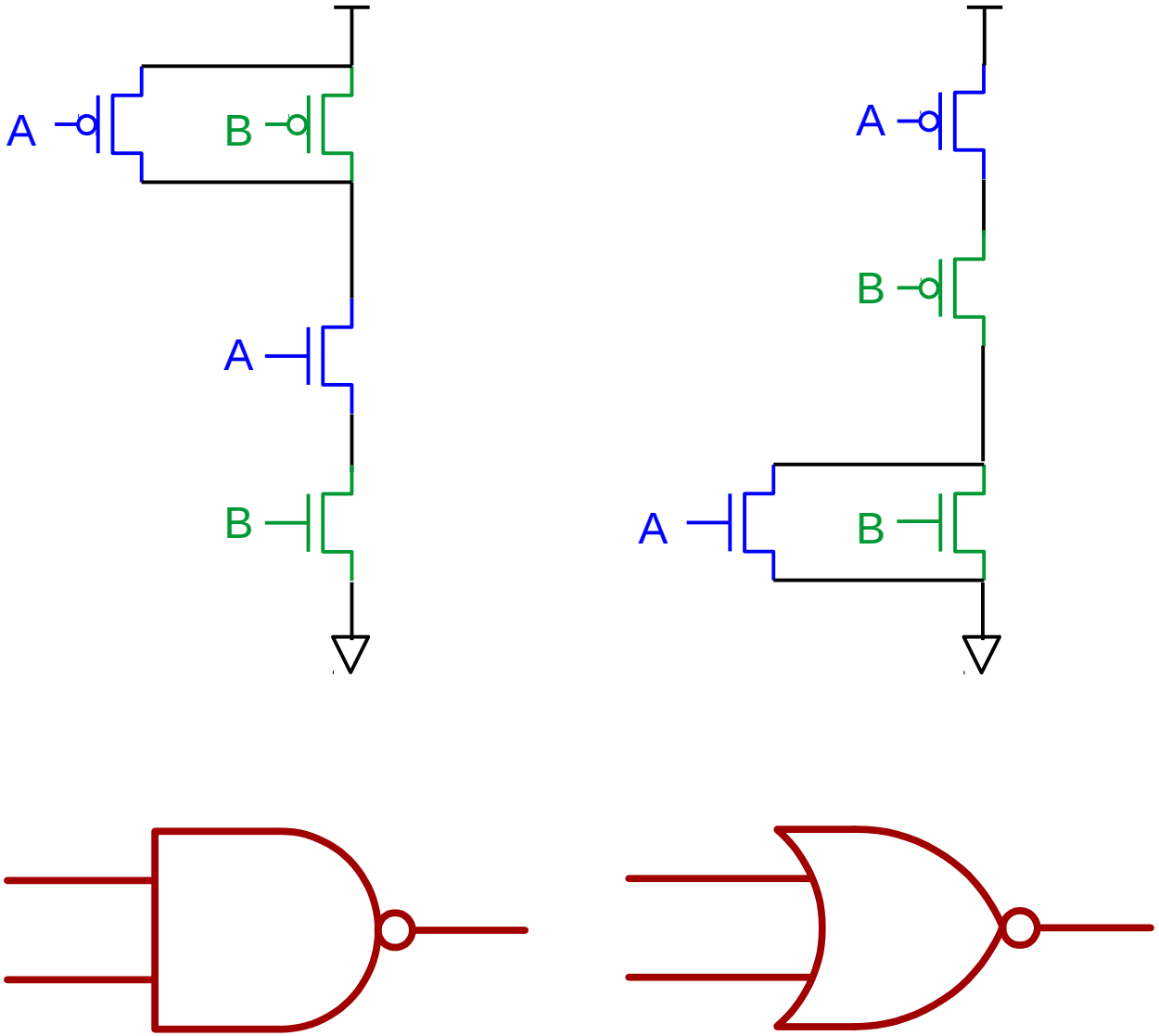
$$F(A, B) = A + B$$

$$\overline{F(A, B)} = G(\overline{A}, \overline{B})$$

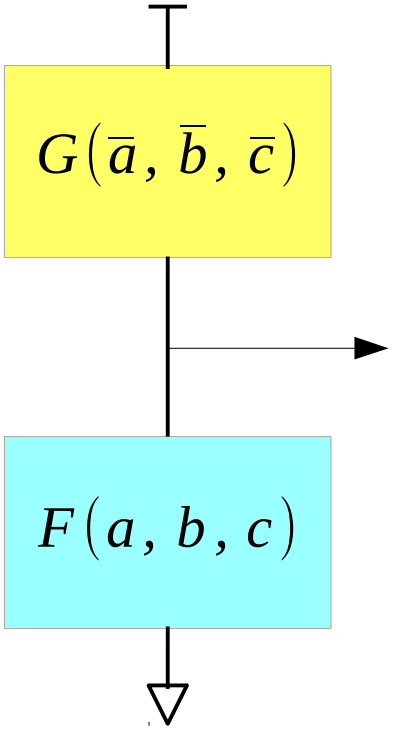
$$\overline{A + B} = \overline{A} \cdot \overline{B}$$



Circuit Families



Circuit Families



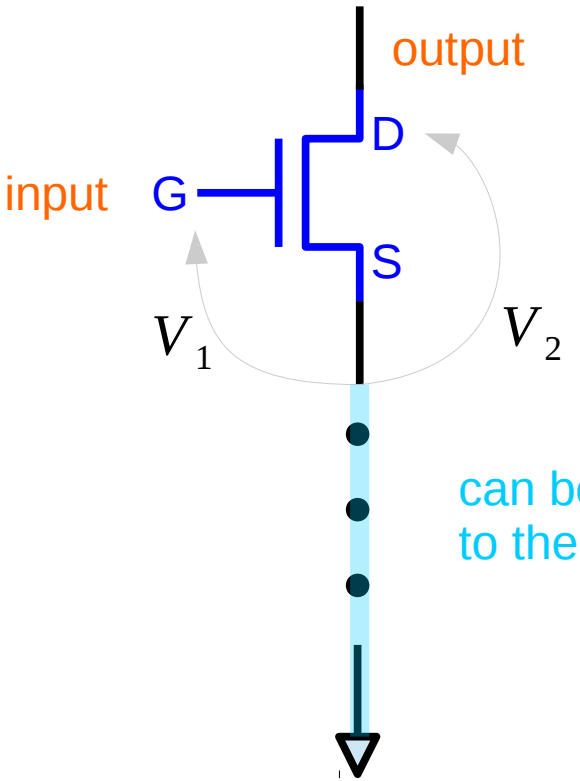
Pull – Up Network

Pull – Down Network

$$\overline{F(a, b, c)} = G(\bar{a}, \bar{b}, \bar{c})$$

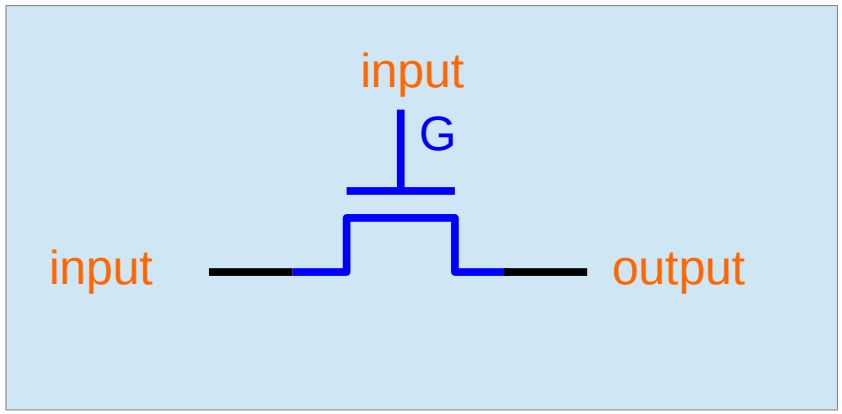
De Morgan's Law

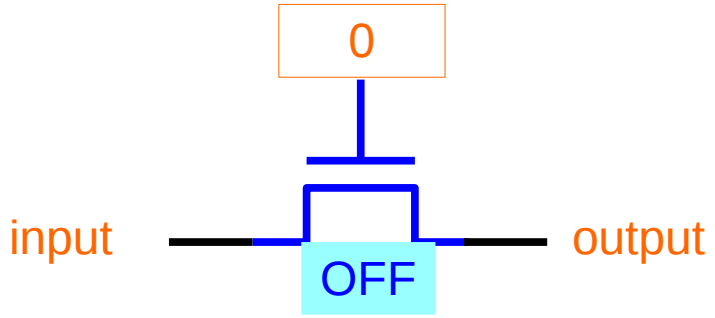
nMOS Operating Modes

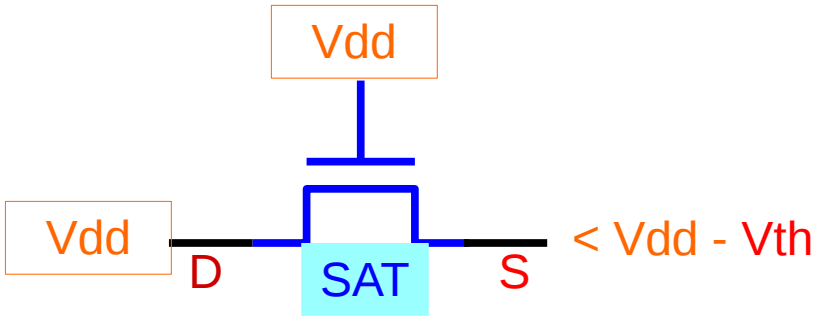


$V_1 < V_{th}$	$V_1 - V_{th} > 0$ $V_1 - V_{th} > V_2$	$V_1 - V_{th} > 0$ $V_1 - V_{th} < V_2$
OFF	LIN	SAT
	$I_{DS} \propto v_{GS}$	$I_{DS} = I_{SAT}$

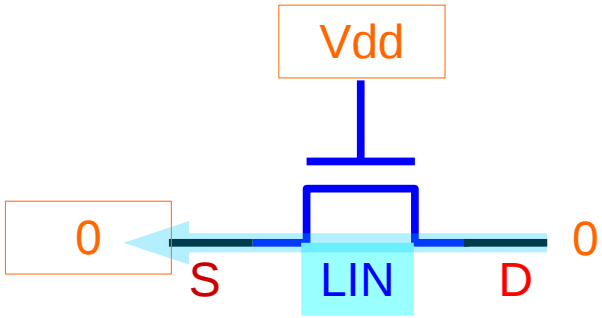
Pass Transistor





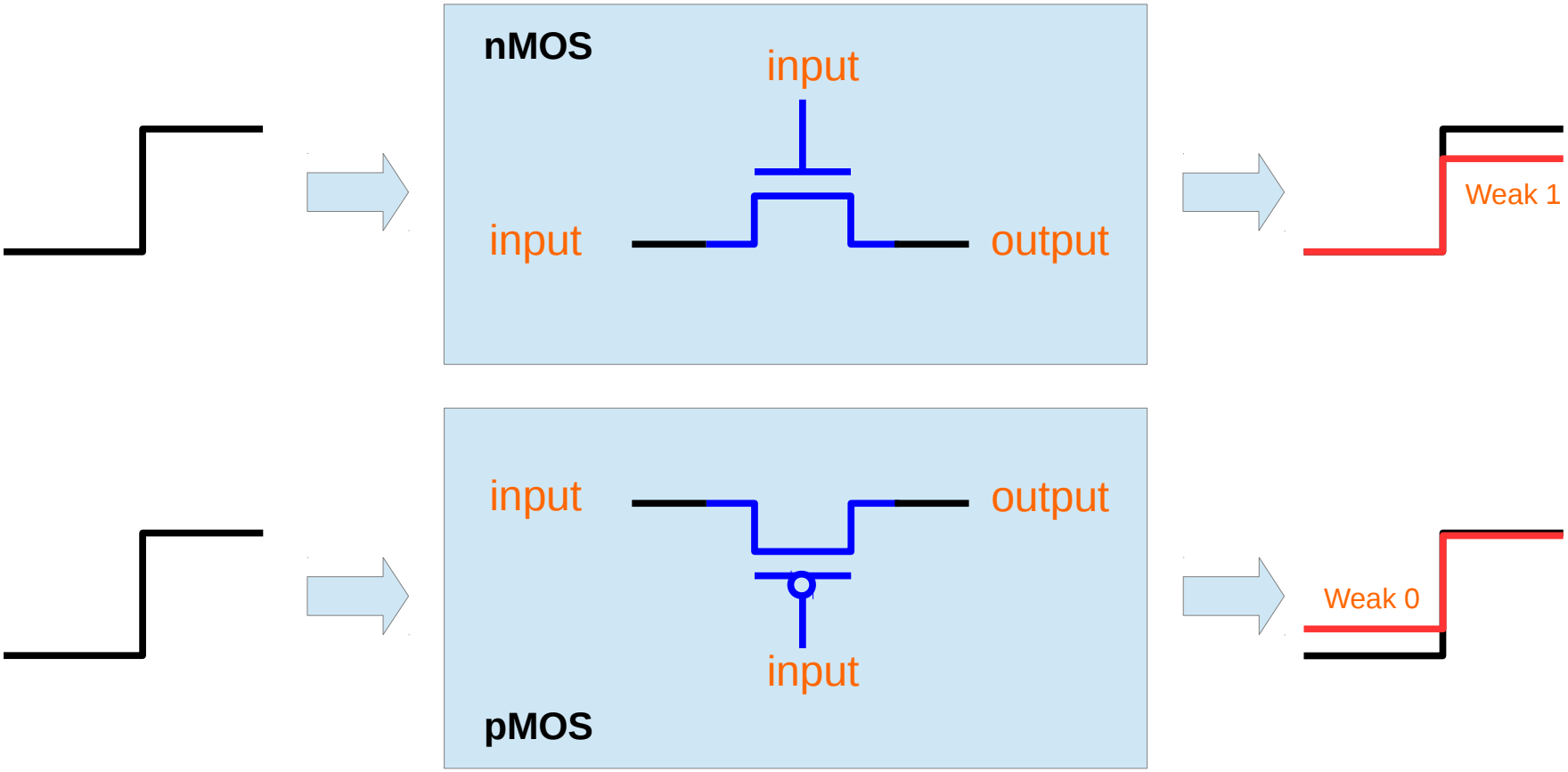


Threshold drop

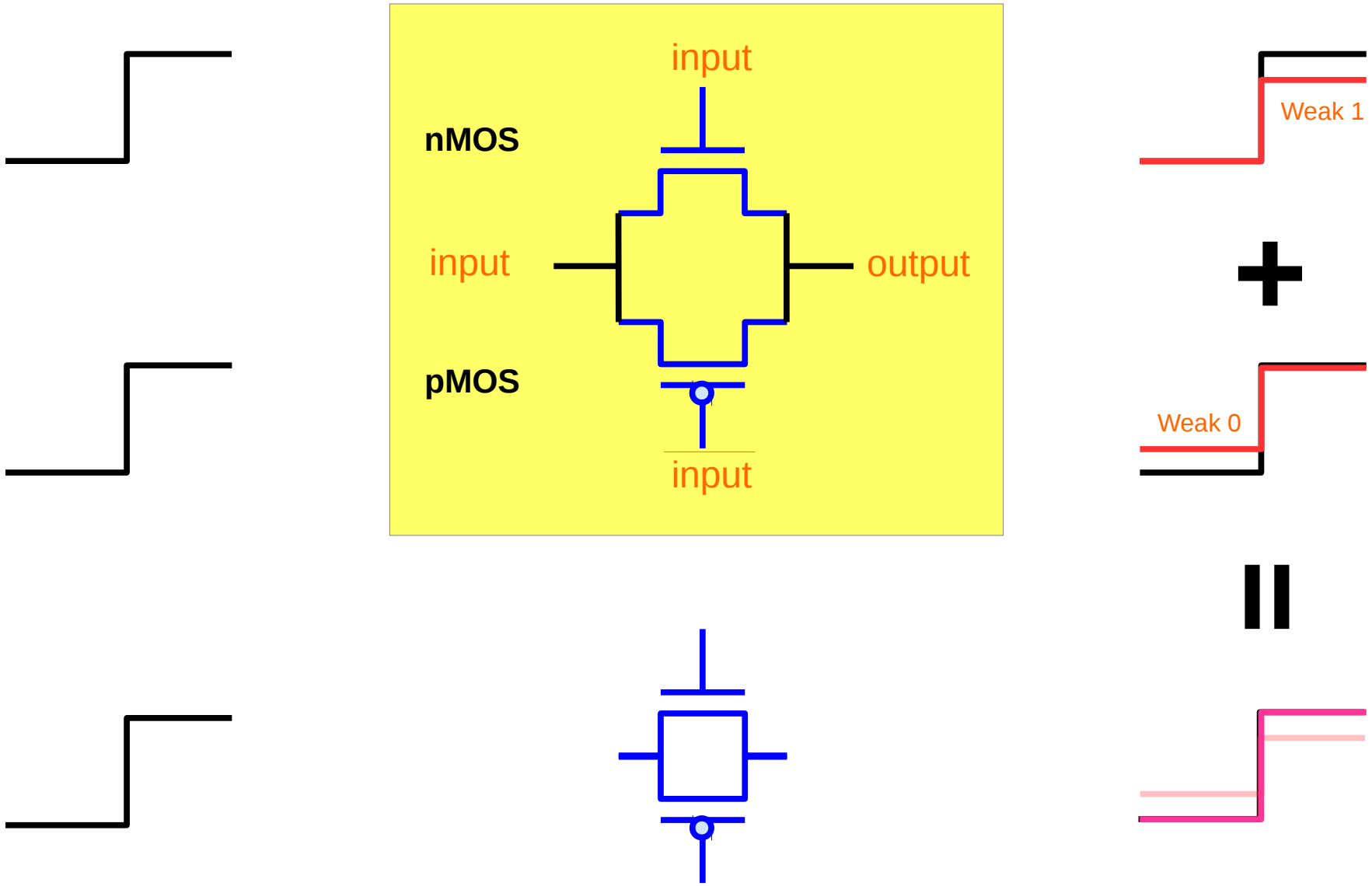


can be pull down
to the GND

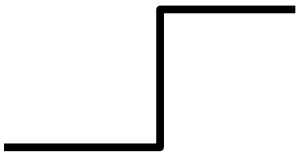
Strong 0 and Weak 1

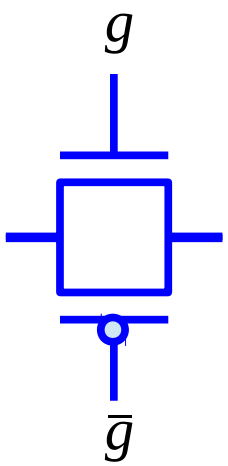


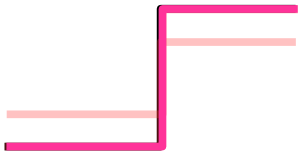
Pass Transistor



Pass Transistor







Pass strong 1 and strong 0

When $g = V_{dd}$ that is
$\bar{g} = 0$

Circuit Families

Circuit Families

Static CMOS
Ratioed Circuits
Cascade Voltage Switch Logic
Dynamic Circuits
Pass Transistor Circuits

References

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[10] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Organization