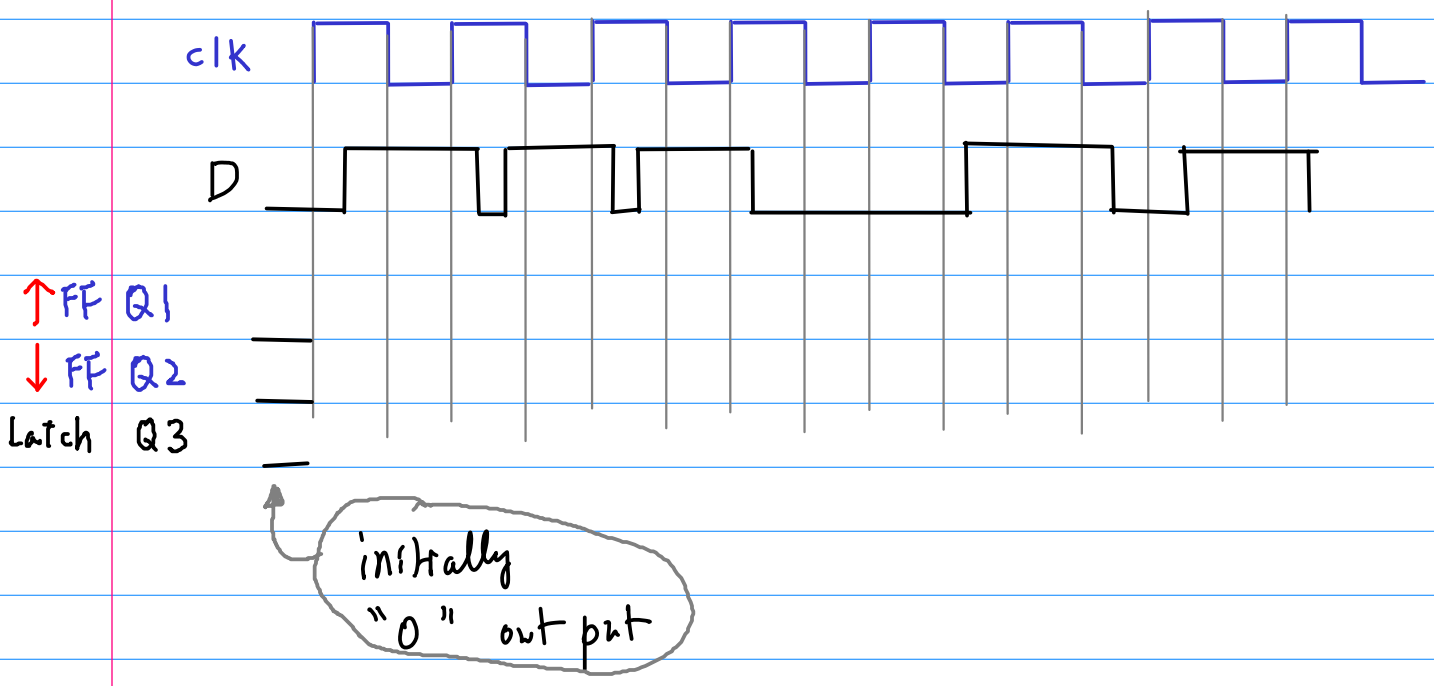
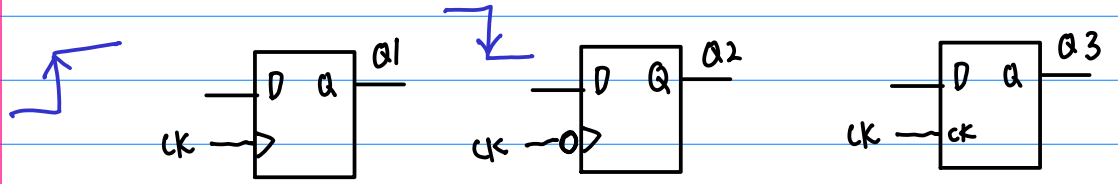
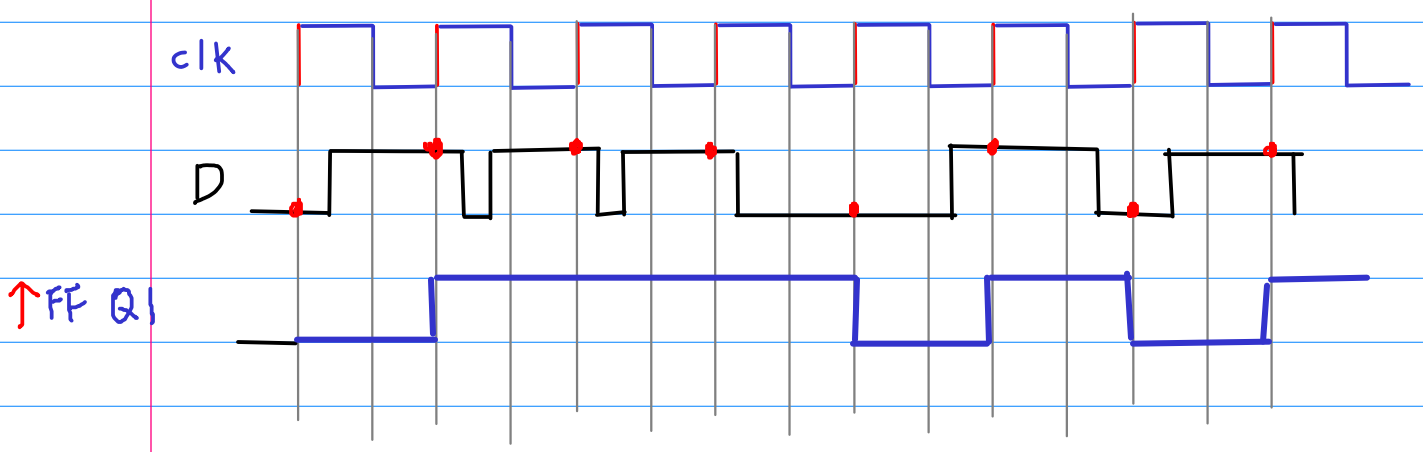
HW #2

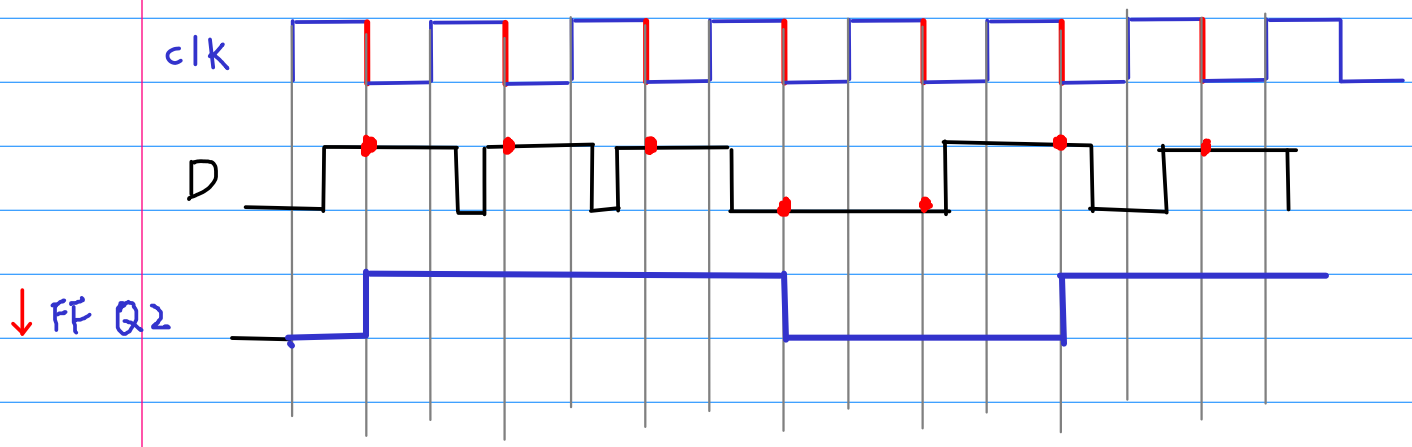
① FF / Latch Timing

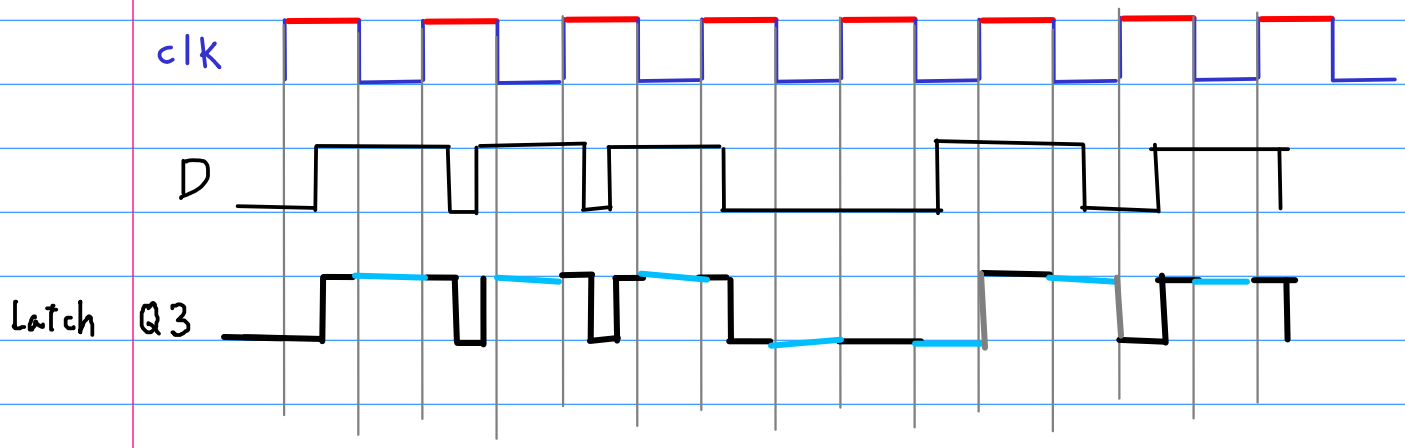




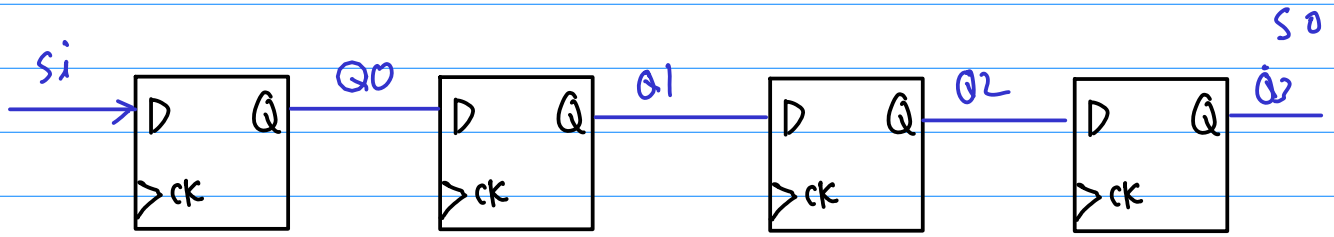
rising edge FF falling edge FF Level sensitive Latch


clk
D
↑FF Q1


clk
D
↓FF Q2


clk
D
Latch Q3

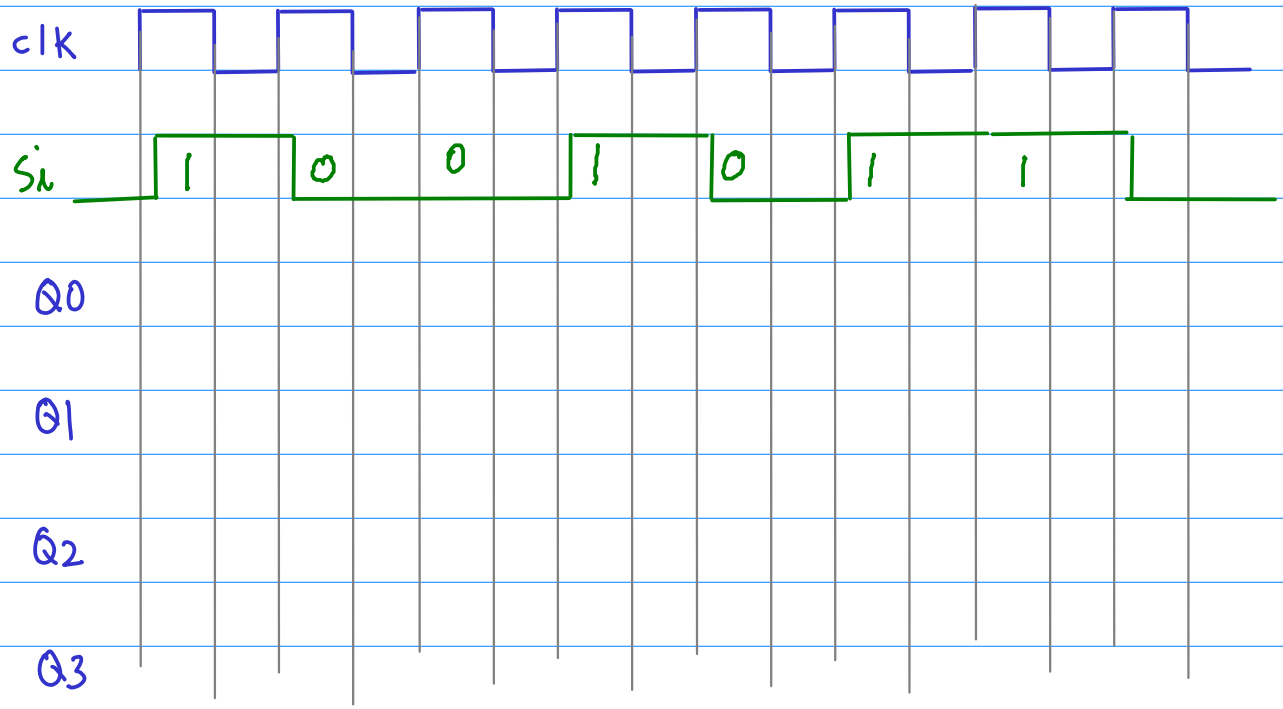
(2) Shift reg.



∴ (Si) sequence

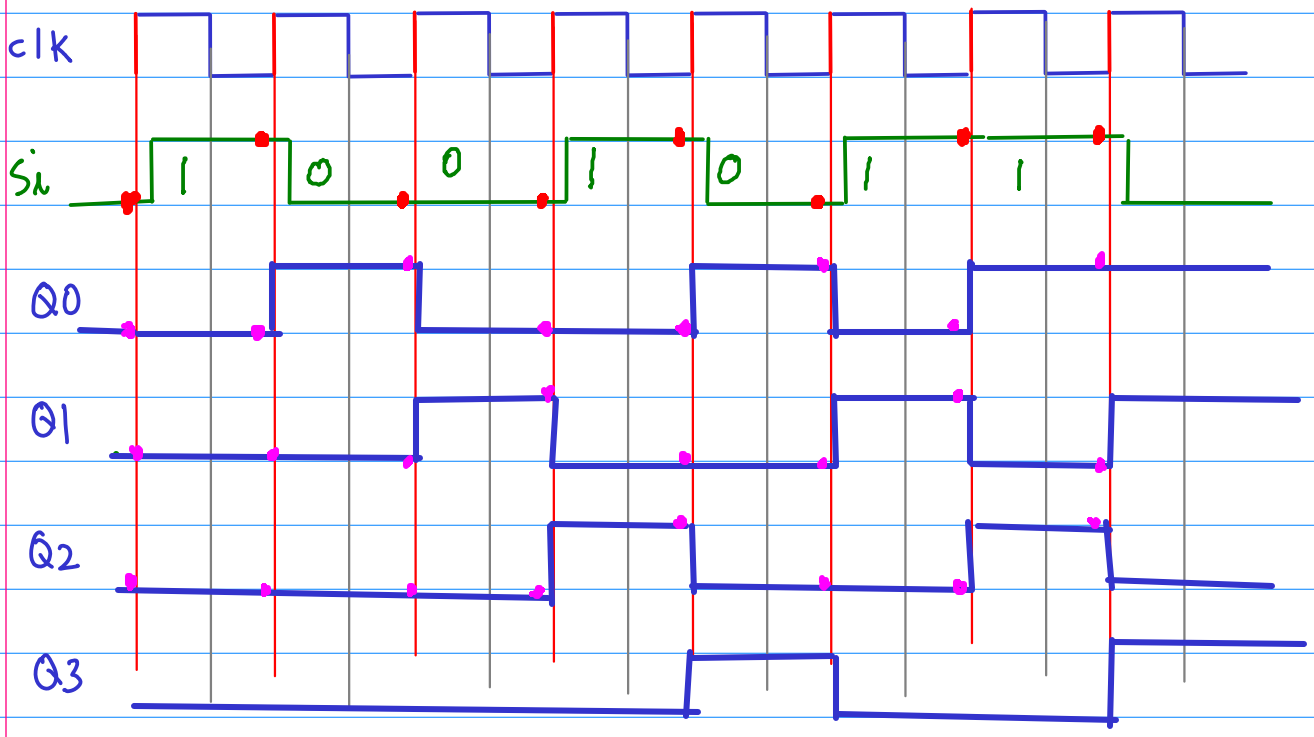
1 0 0 1 0 1 1

Wave form ?



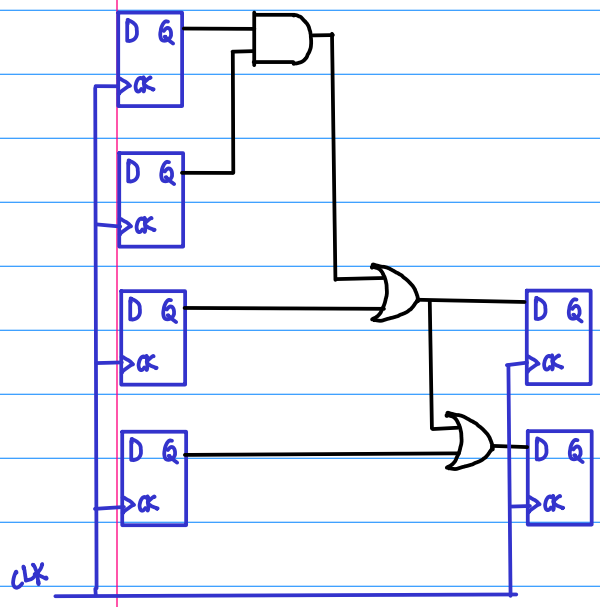
1 0 0 1 0 1 1

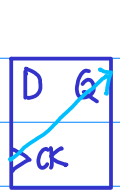
Wave form ?



③ Setup & hold Timing check.

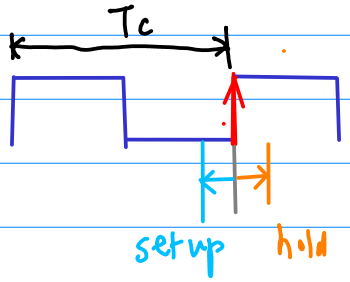
chap 3





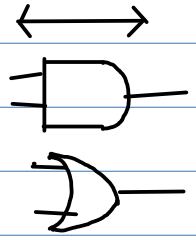
min $t_{ccq} = 30ps$

max $t_{pcq} = 50ps$



$t_{setup} = 60ps$

$t_{hold} = 70ps$



$t_{cd} = 25ps$

$t_{pd} = 35ps$

$t_{pd} = ?$

$t_{cd} = ?$

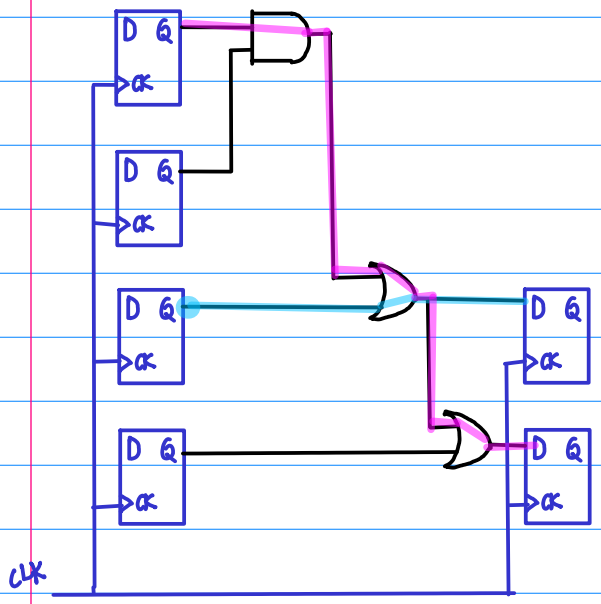
Setup time constraint

$T_c \geq$

$f_c =$

Hold time constraint

$t_{ccq} + t_{cd} \overset{?}{\geq} t_{hold}$



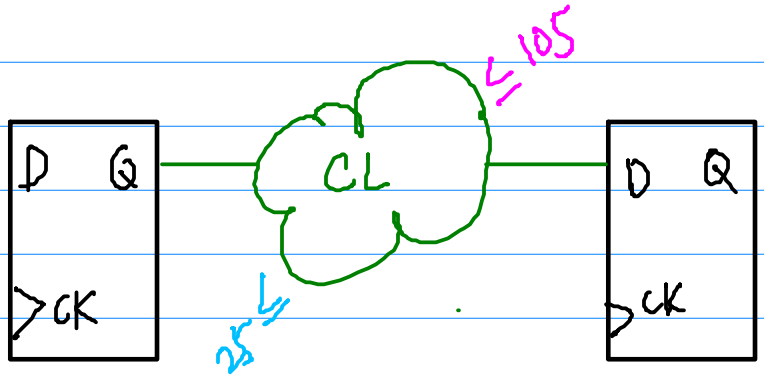
min path : 1 gate delay

$1 \times t_{cd} = 25$

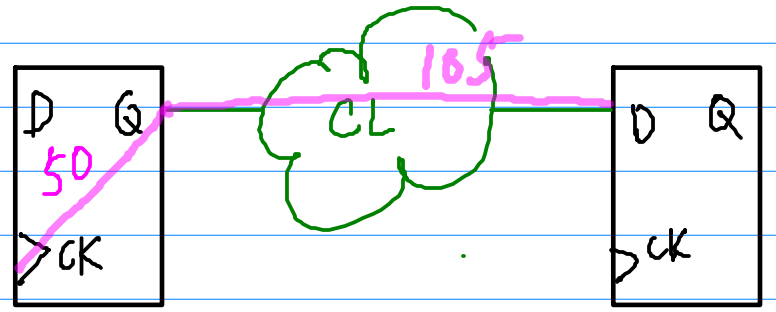
max path : 3 gate delay

$3 \times t_{pd} = 3 \times 35 = 105$

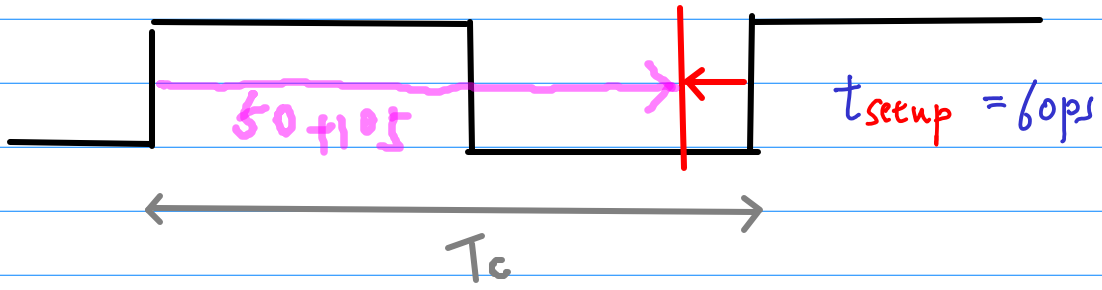
simplify



max path

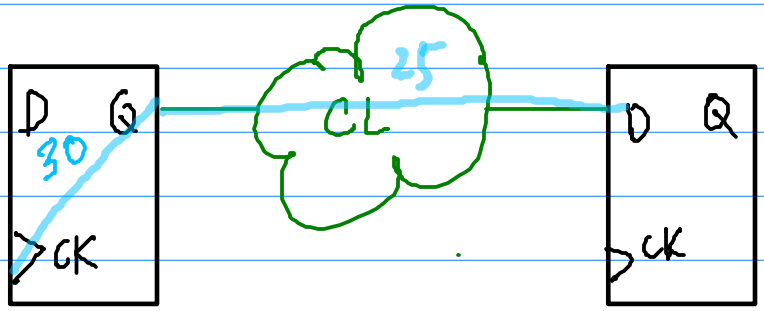


$t_{pcq} = 50ps$



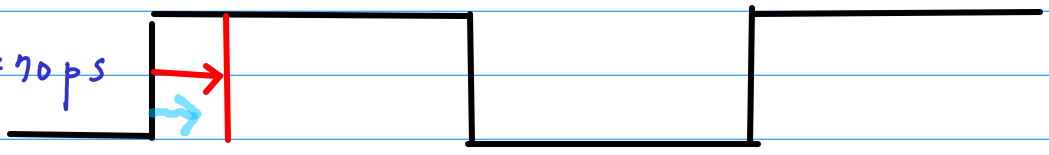
$T_c \geq 50+105+60 = 215$

min path



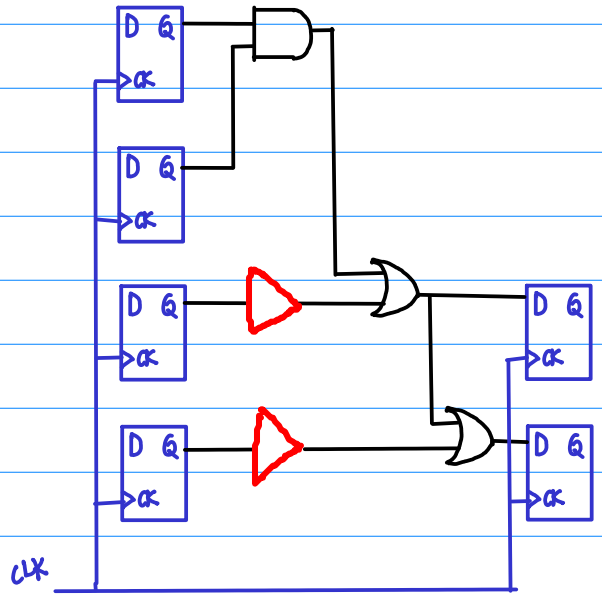
$t_{ccq} = 30ps$

30+25 must be greater than 70



30+25 ✗ 70 hold violation!

add buffers



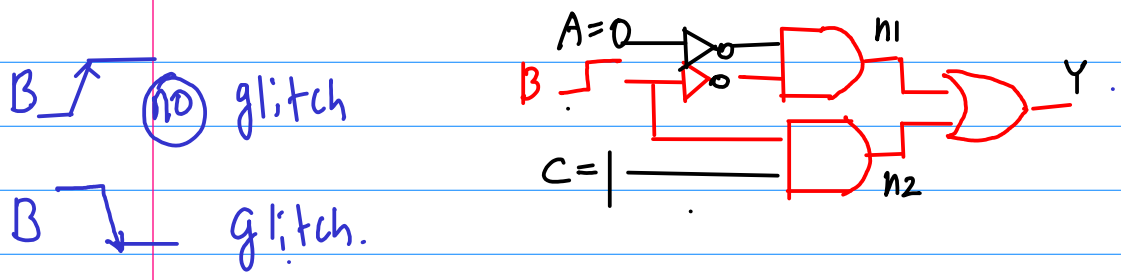
min path 2 gates delay

max path 3 gates delay

now $2 \times 25 + 30 > 70$

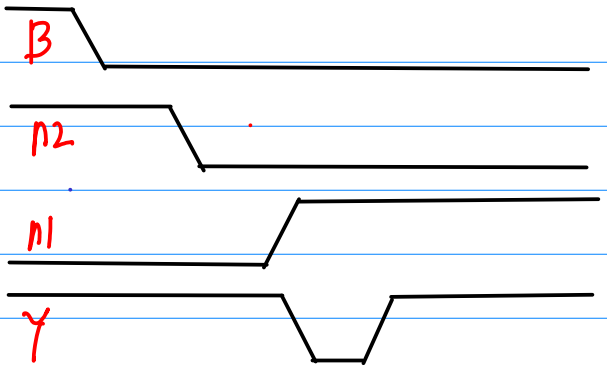
hold constraints met

④ explain the timing diagram in the below



B ↑ no glitch

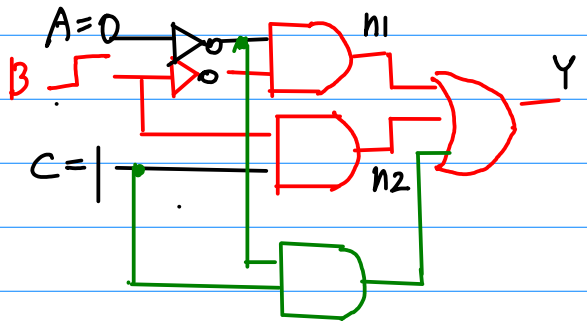
B ↓ glitch.



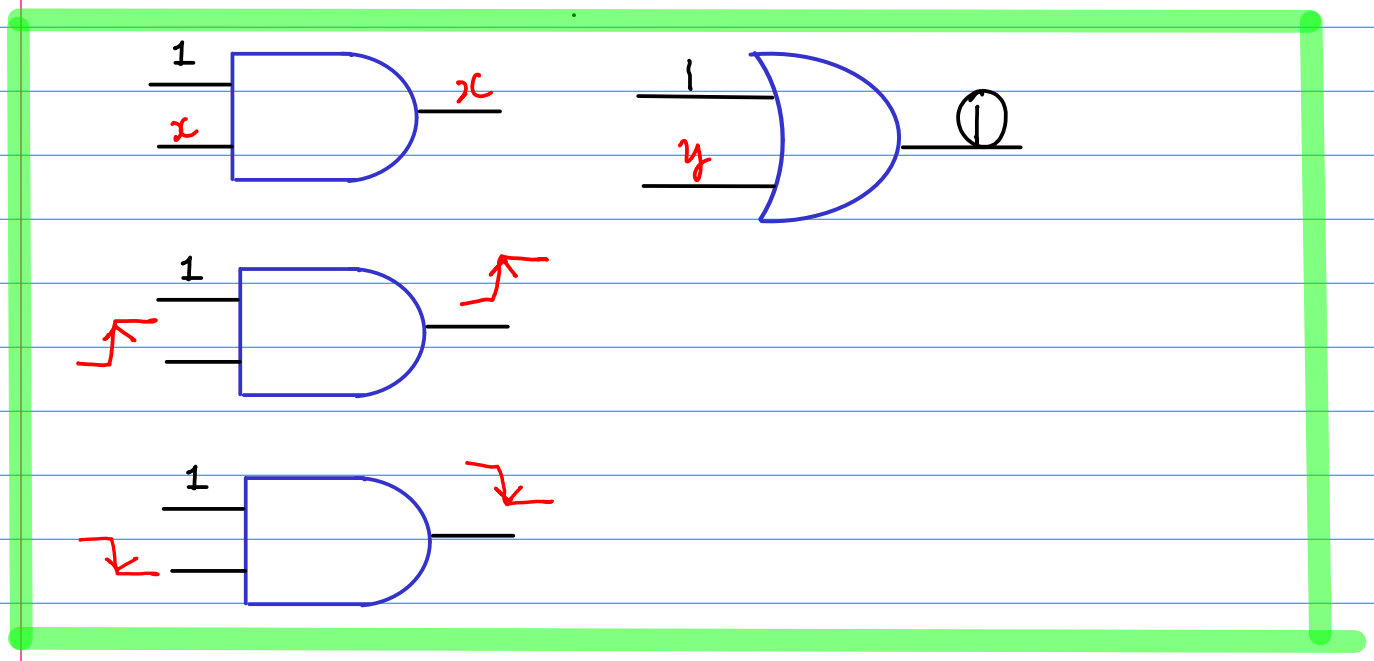
Glitches

Harris "Digital design & Computer Architecture" Elsevier

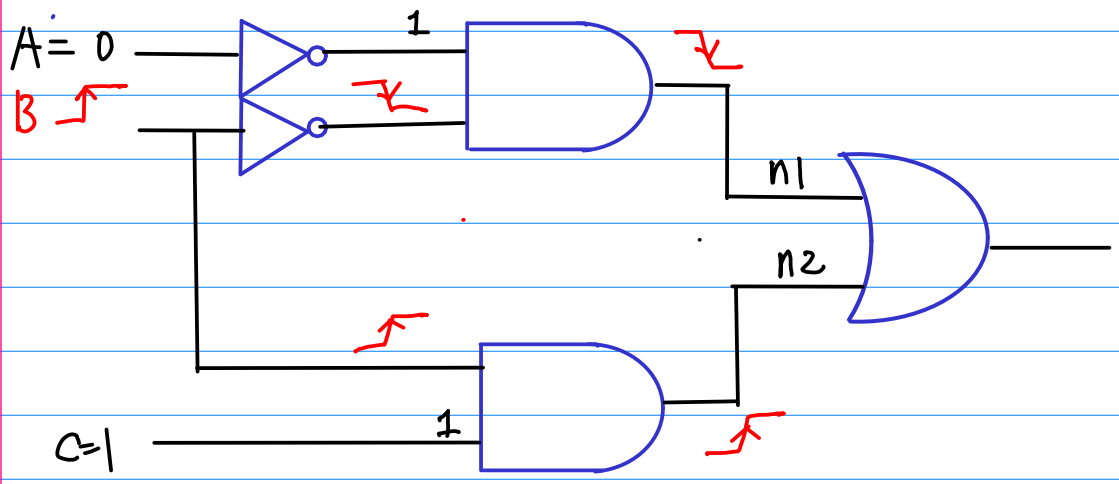
Chap 2.



timing diagram?

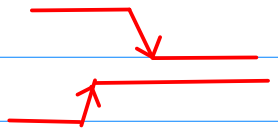

1
x
xc
1
y
1
1

I B L → H transition no glitch !



different arrival times of S1 & S2
can cause glitch
at the output of the OR gate

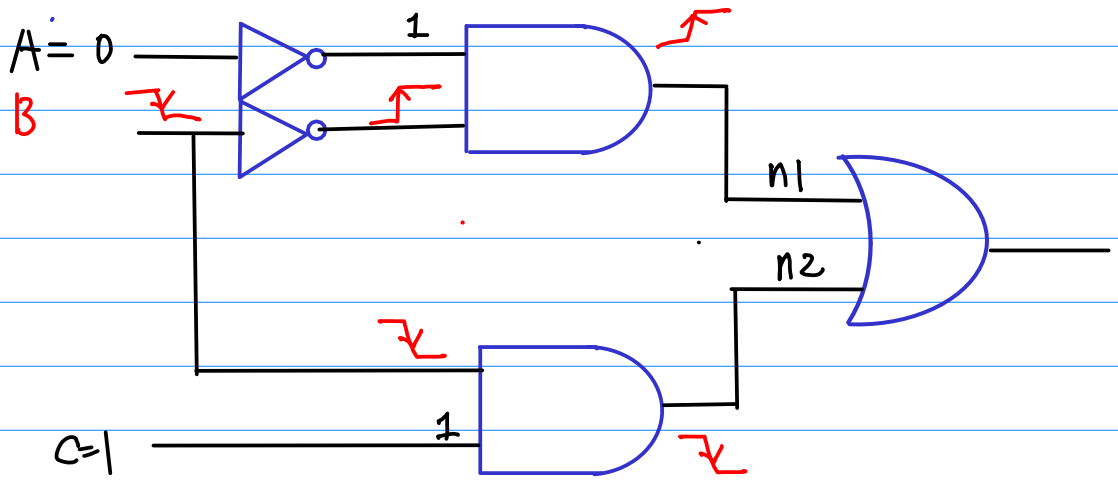
n1 : 2-gate delay
n2 : 1- gate delay



— slower

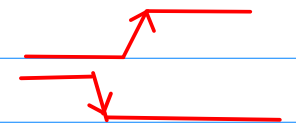
n1+n2 high

II B H → L transition glitch !



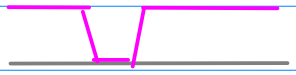
different arrival times of S_1 & S_2 can cause glitch at the output of the OR gate

n_1 : 2-gate delay
n_2 : 1-gate delay

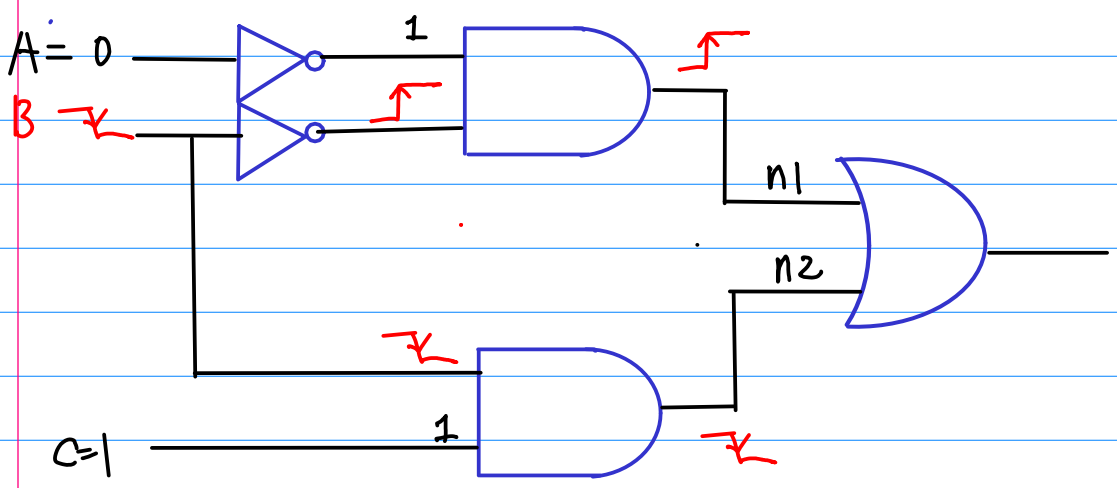


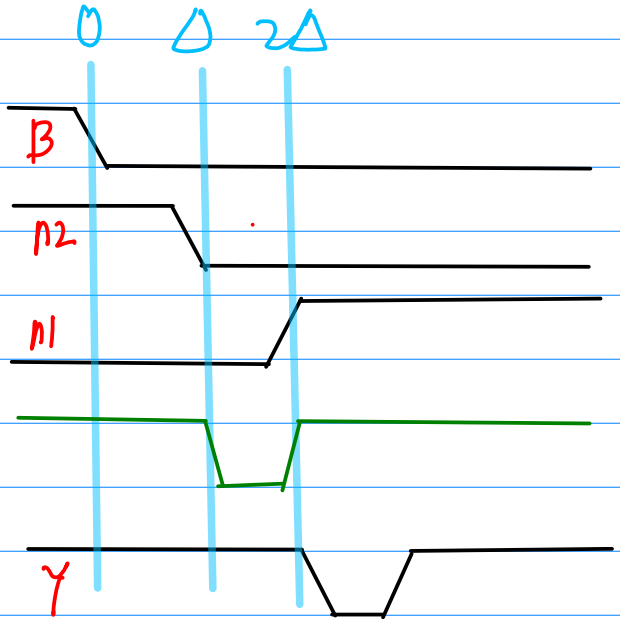
— slower

$n_1 + n_2$



glitch.

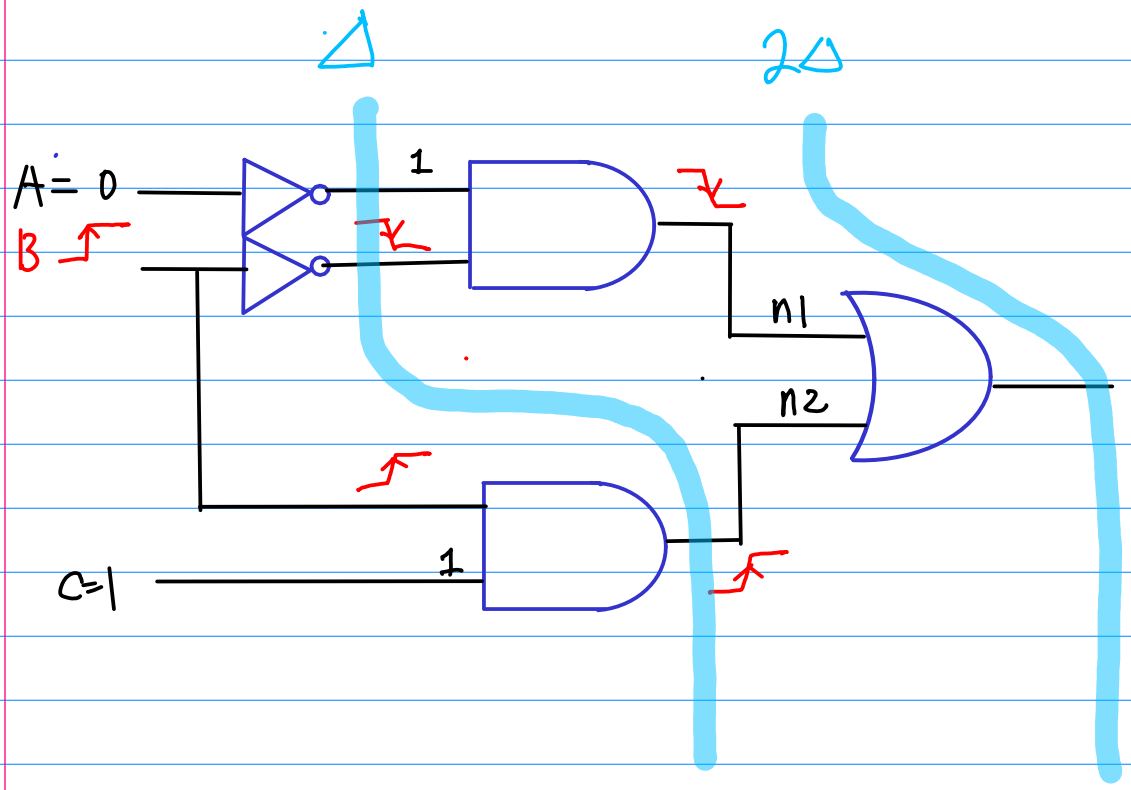


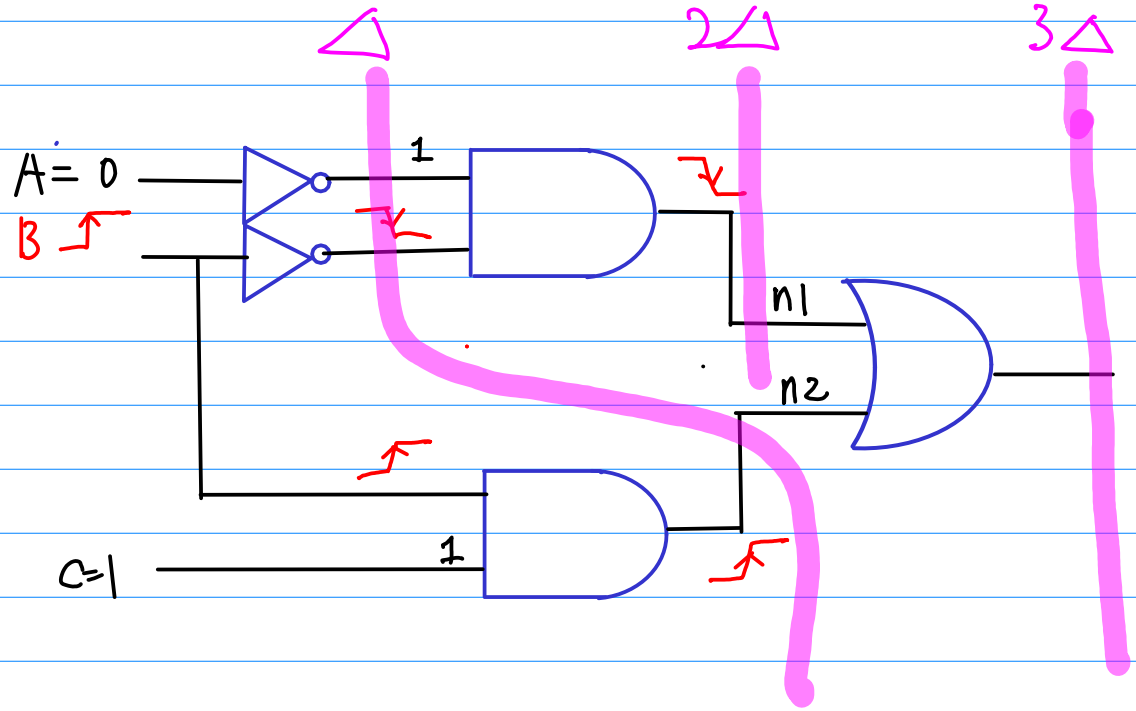


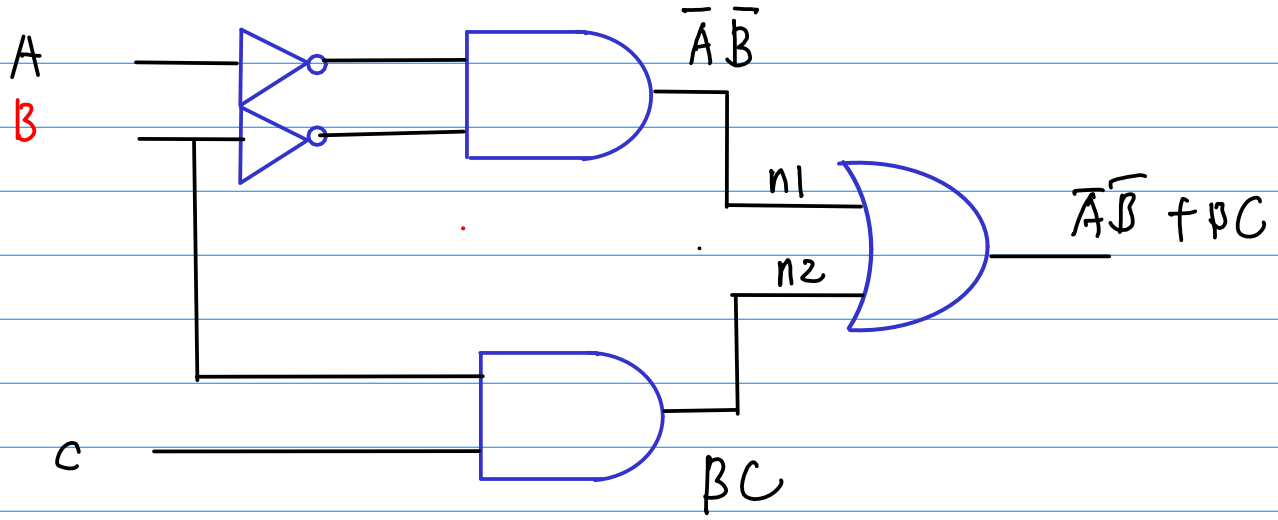
n1 + n2 w/o delay

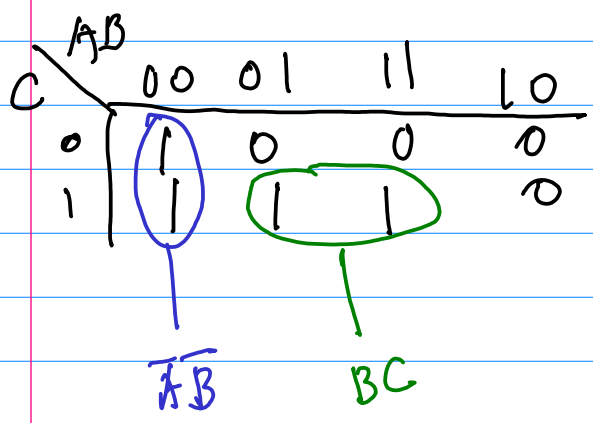
Glitches

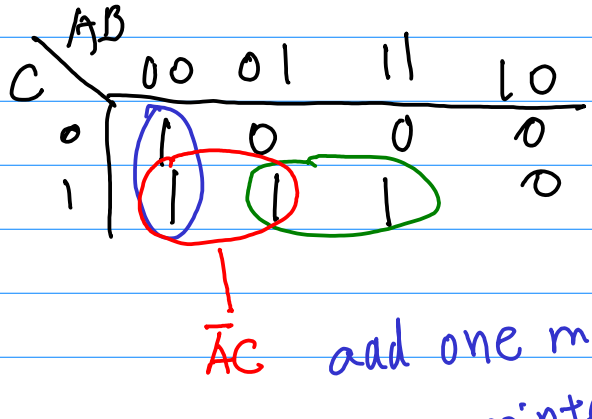
Δ : 1 gate delay.

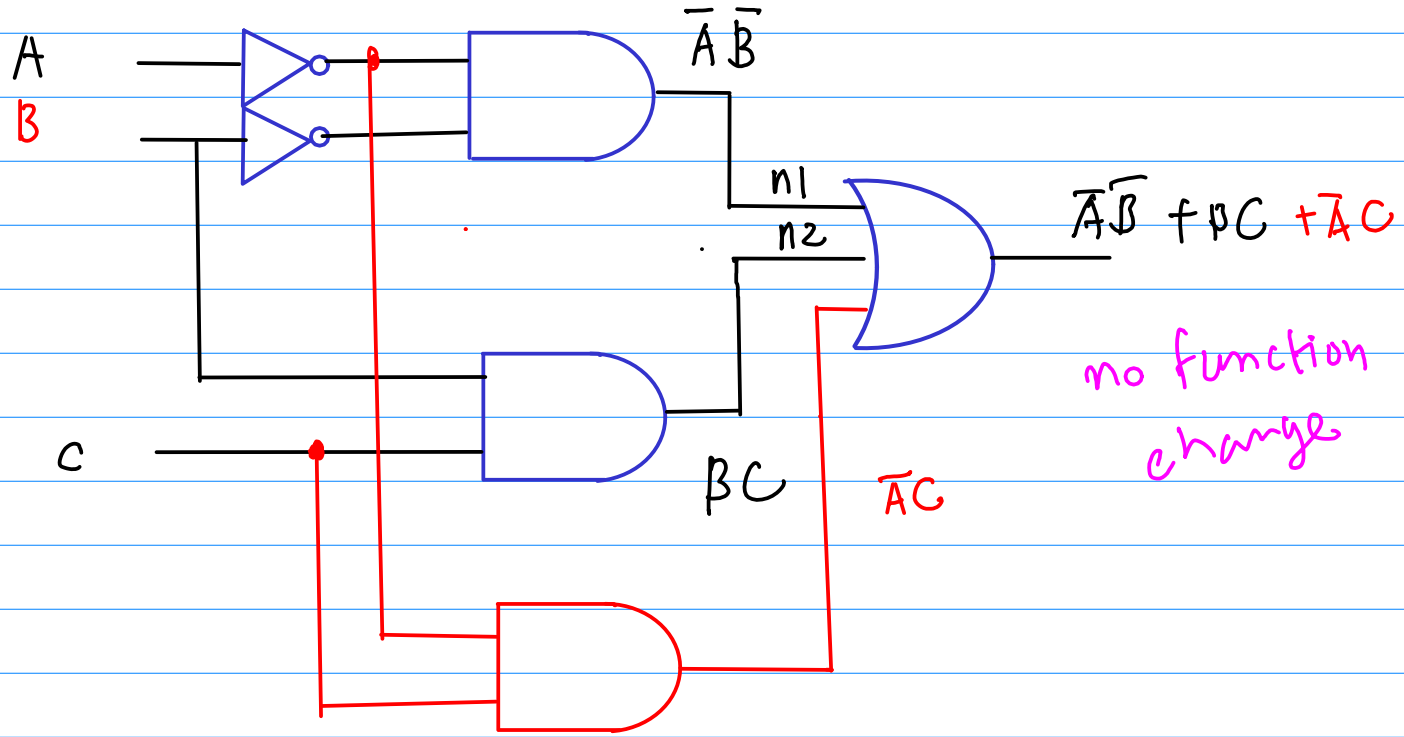


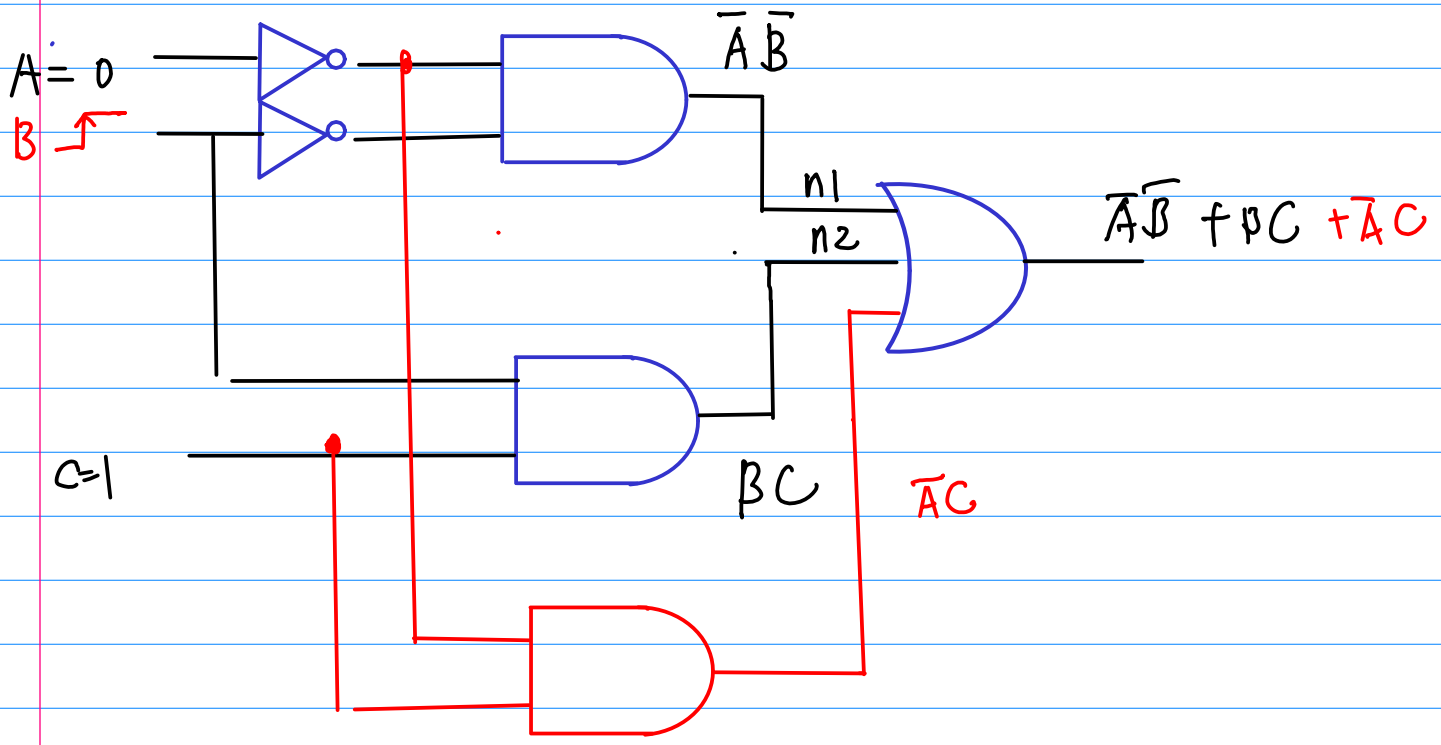


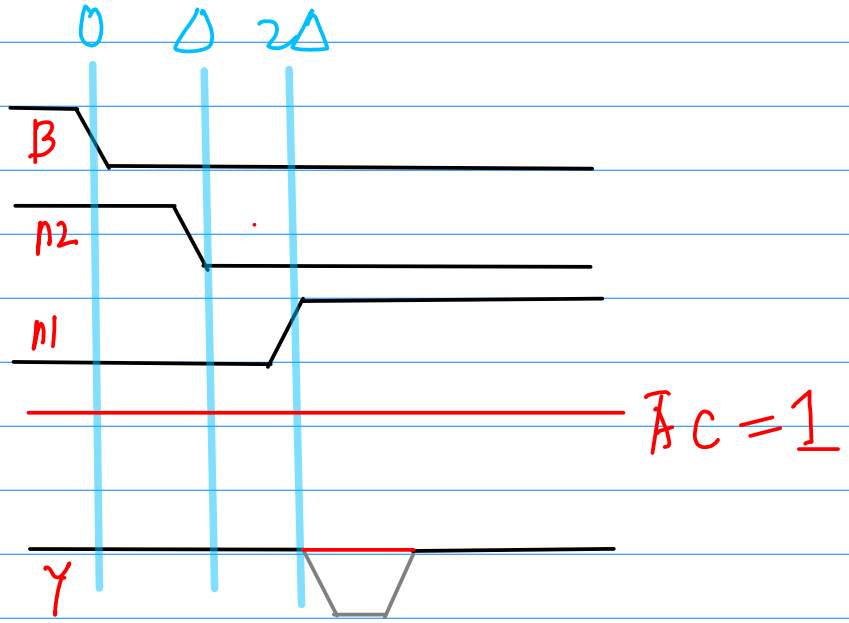

A
B
C
$\bar{A}\bar{B}$
n1
n2
$\bar{A}\bar{B} + BC$
BC


AB
C
00 01 11 10
0 1 0 0
1 1 1 0
$\bar{A}\bar{B}$
BC


AB
C
00 01 11 10
0 1 0 0
1 1 1 0
$\bar{A}C$
add one more minterm


A
B
C
$\bar{A}\bar{B}$
n1
n2
$\bar{A}\bar{B} + BC + \bar{A}C$
BC
$\bar{A}C$
no function change


A = 0
B
C = 1
$\bar{A}\bar{B}$
n1
n2
$\bar{A}\bar{B} + BC + \bar{A}C$
BC
$\bar{A}C$


0
Δ
2Δ
B
n2
n1
$\bar{A}C = 1$
Y

Glitches