Gate Power

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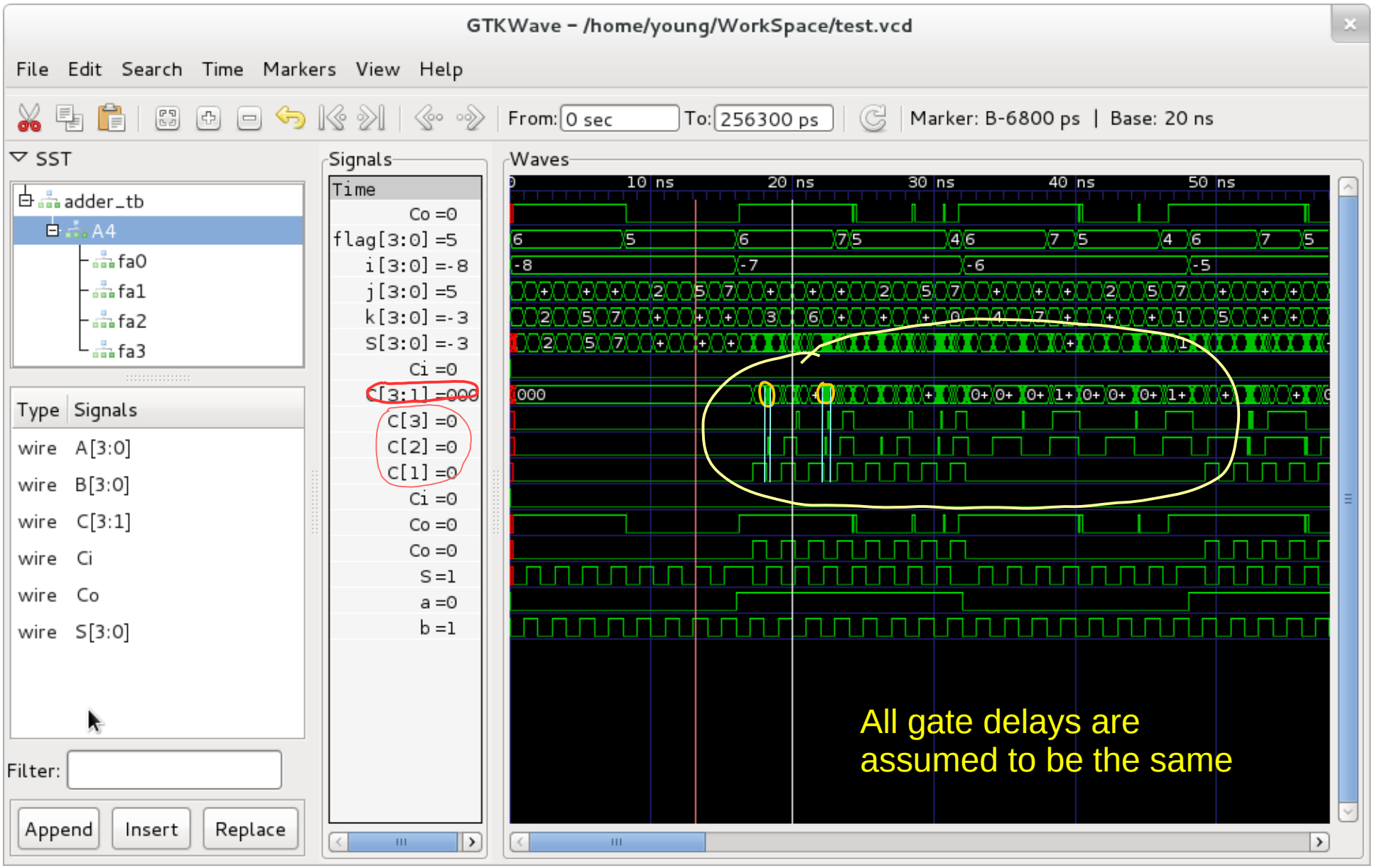
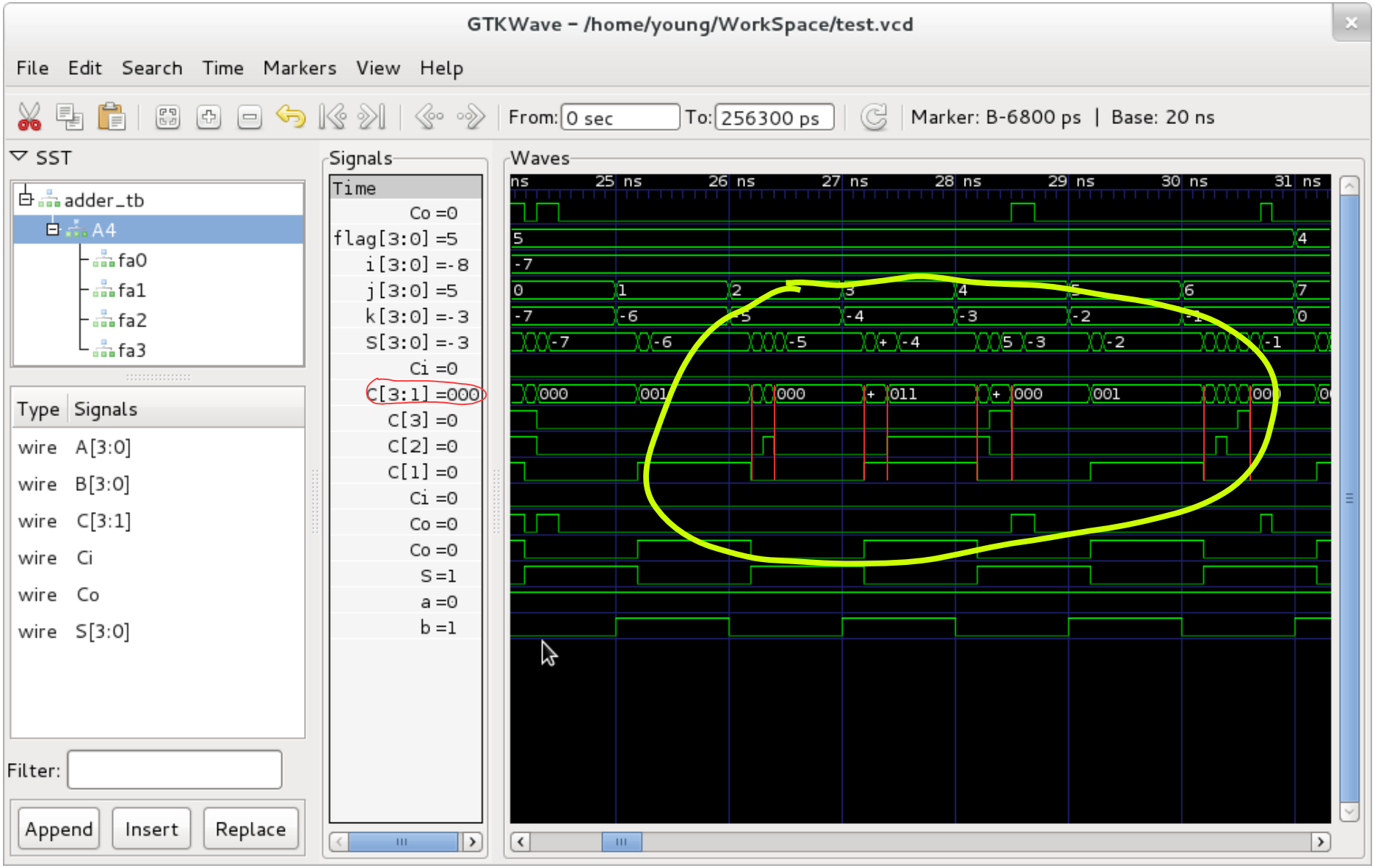
This document was produced by using OpenOffice and Octave.

Adder Simulation Waveform



Glitches


GTKWave – /home/young/WorkSpace/test.vcd
File Edit Search Time Markers View Help
From: 0 sec
To: 256300 ps
Marker: B-6800 ps | Base: 20 ns
SST
adder_tb
A4
fa0
fa1
fa2
fa3
Type Signals
wire A[3:0]
wire B[3:0]
wire C[3:1]
wire Ci
wire Co
wire S[3:0]
Filter:
Append
Insert
Replace
Signals
Time
Co =0
flag[3:0] =5
i[3:0] =-8
j[3:0] =5
k[3:0] =-3
S[3:0] =-3
Ci =0
C[3:1] =000
C[3] =0
C[2] =0
C[1] =0
Ci =0
Co =0
Co =0
S =1
a =0
b =1
Waves
ns 25 ns 26 ns 27 ns 28 ns 29 ns 30 ns 31 ns

Dynamic Power

Activity Factor
- Clock Gating

- Switching Probability
- Glitches

Static Power

Power Gating

Low Power Architecture

Micro Architecture

Parallelism and Pipelining

Power Management Mode

Segmented Bus

Multi Core

Pass Transistor Circuits

References

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[6] https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design
[7] https://en.wikiversity.org/wiki/The_necessities_in_Digital_Design
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[9] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Architecture
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[11] https://en.wikiversity.org/wiki/Verilog_programming_in_plain_view