

# CMOS Sequential Circuits

## Seq-4 (H.4)

20151215

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# References

Some Figures from the following sites

[1] <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>  
Weste & Harris Book Site

[2] [en.wikipedia.org](http://en.wikipedia.org)

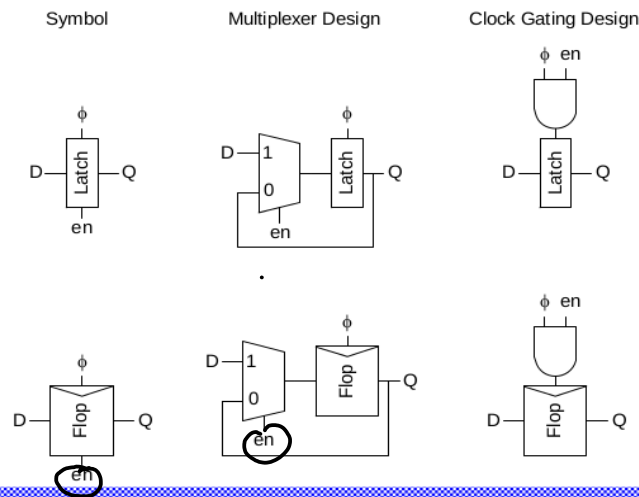
[3] Digital Integrated Circuits : A Design Perspective,  
Jan M. Rabaey,  
(<http://bwracs.eecs.berkeley.edu/Classes/lcBook/>)

[4] Digital Electronics and Design with VHDL  
Pedroni

# Latch and FF with Enable

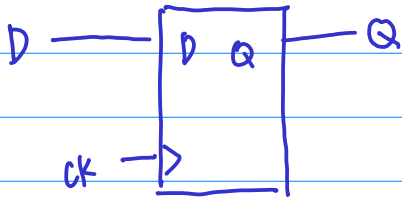
## Enable

- Enable: ignore clock when  $en = 0$ 
  - Mux: increase latch D-Q delay
  - Clock Gating: increase en setup time, skew

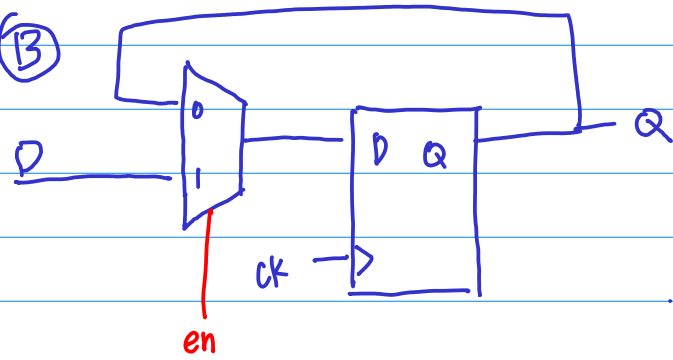


# Flipflop with Enable

(A)

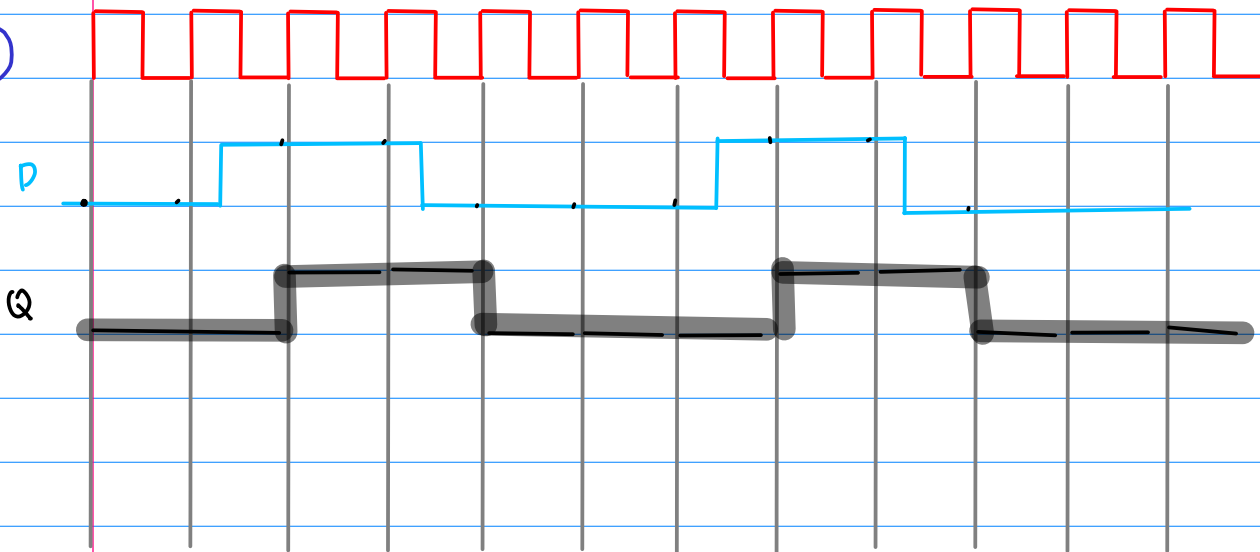


(B)

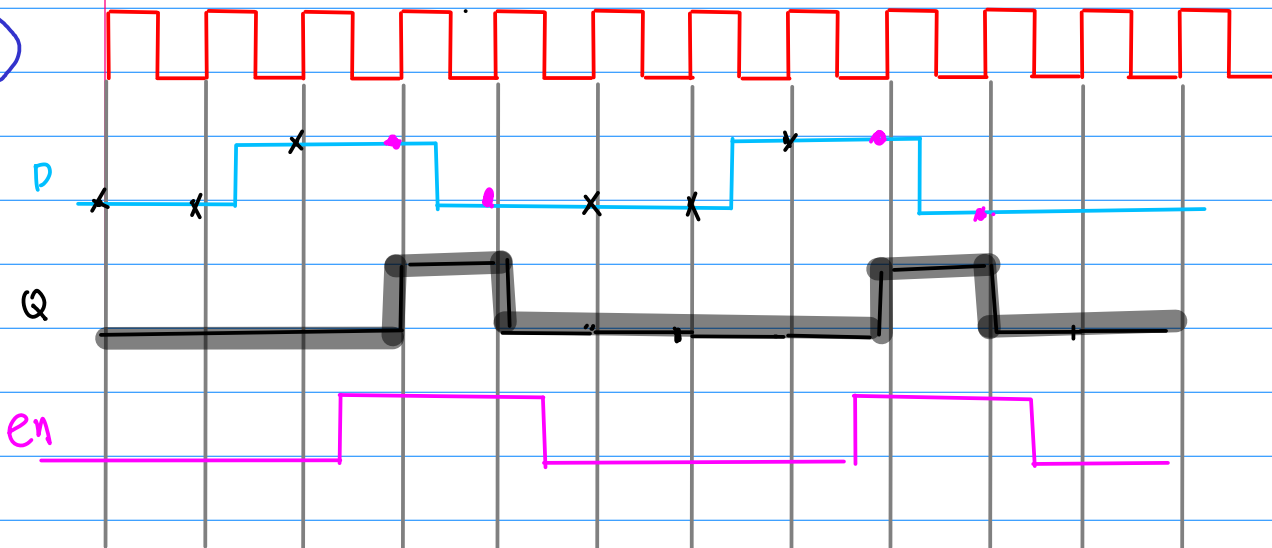


enable  
load

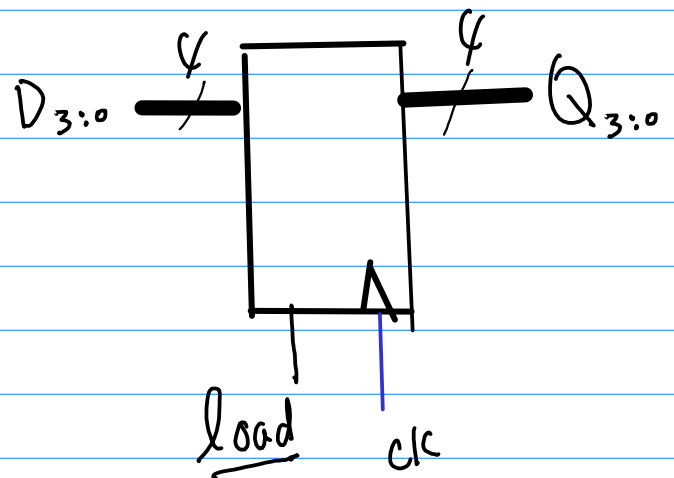
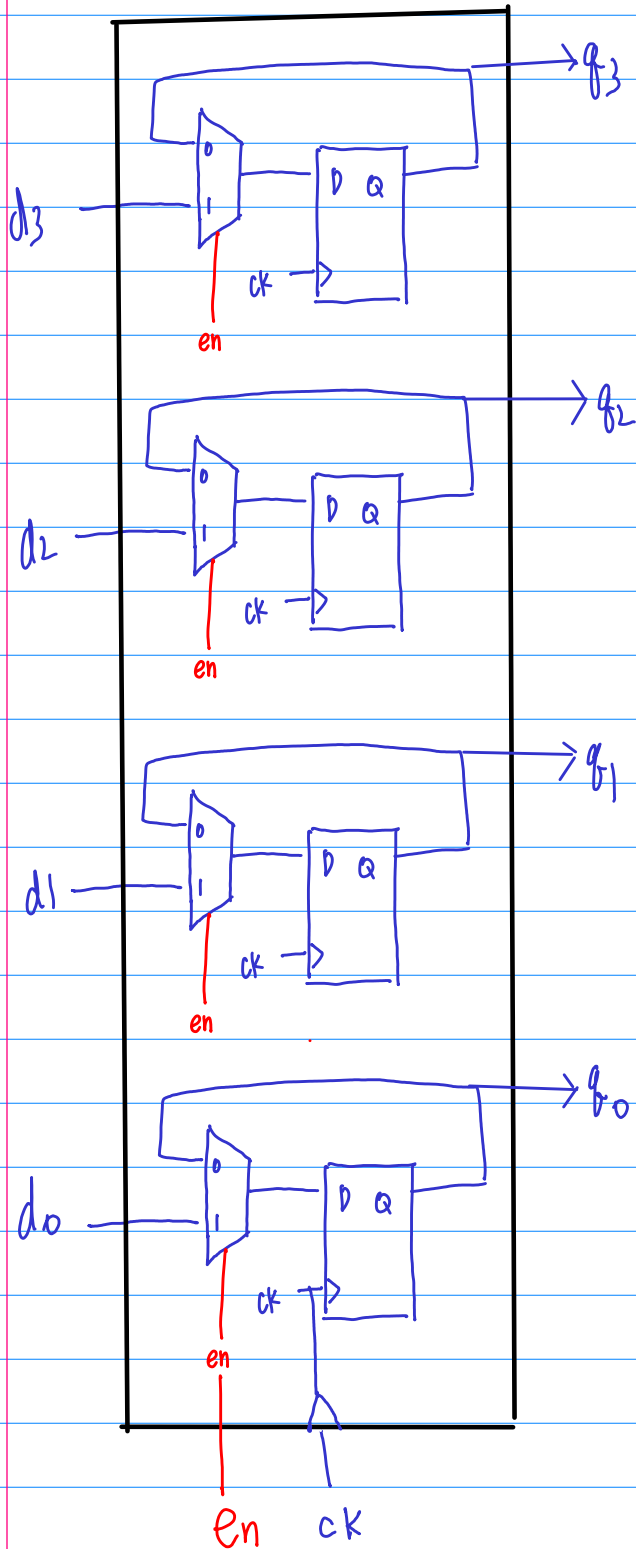
(A)



(B)



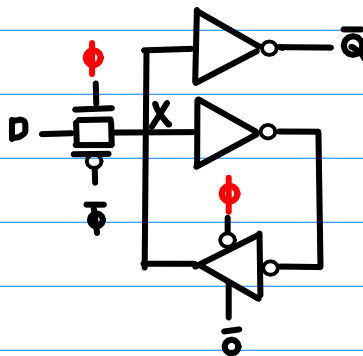
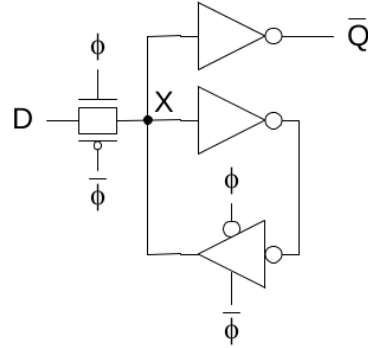
# Register with Enable



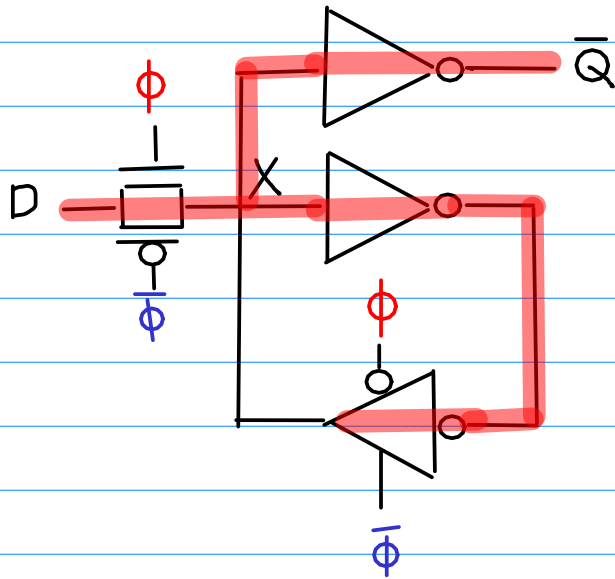
# Latch Design

## □ Datapath latch

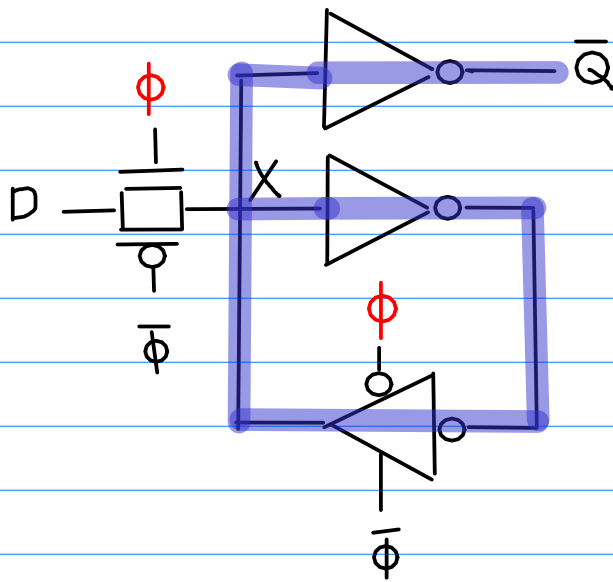
- +
- +
- 



# transparent and opaque mode



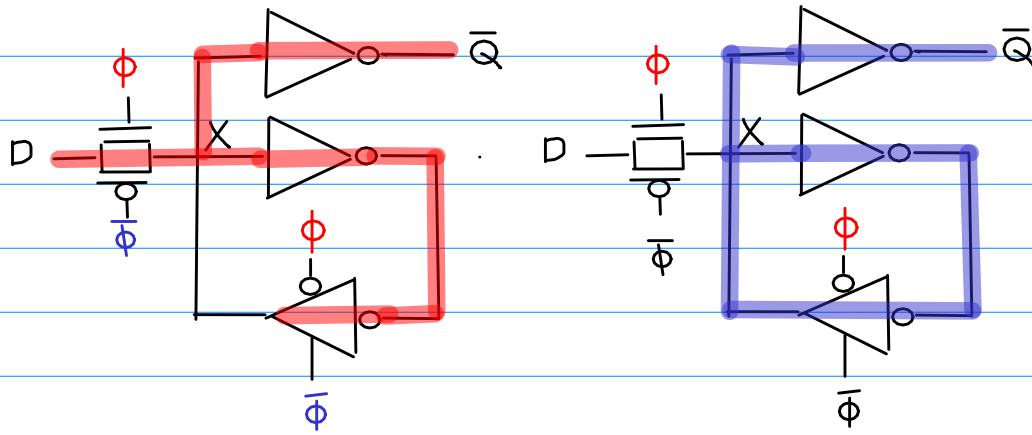
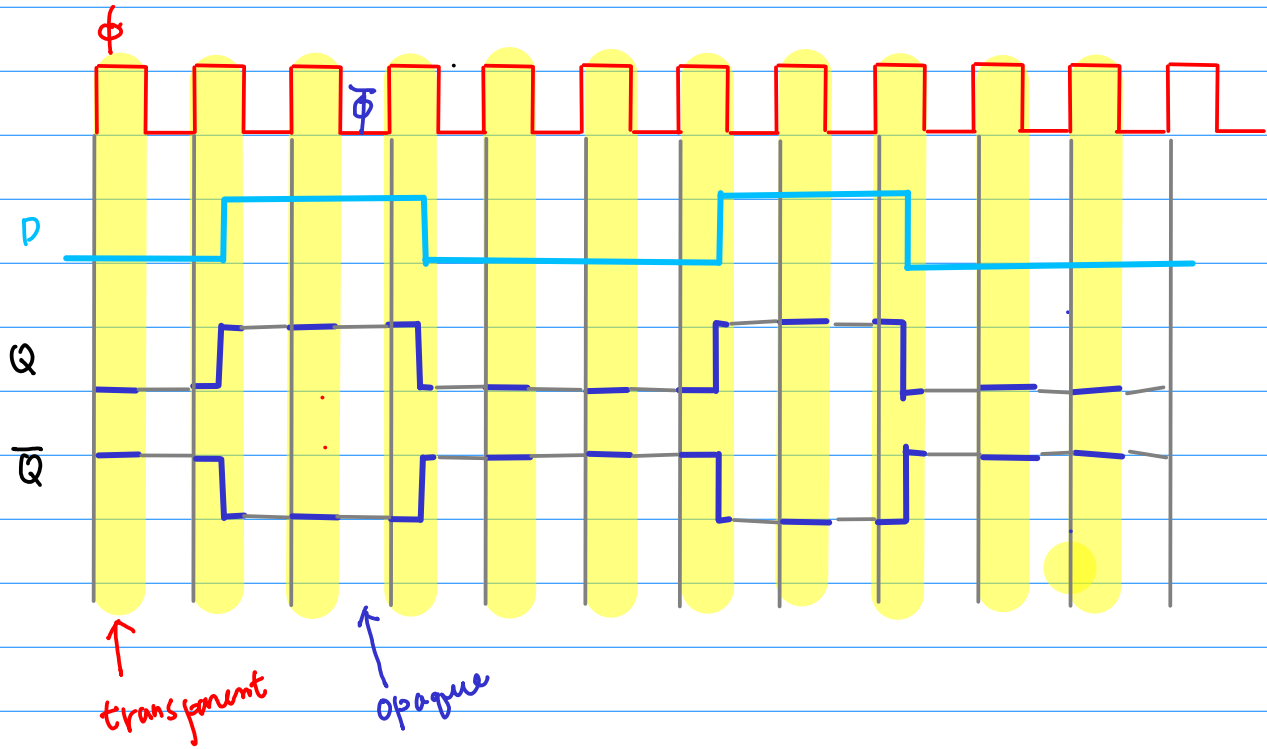
$\phi = H$  : transparent



$\bar{\phi} = H$  : opaque

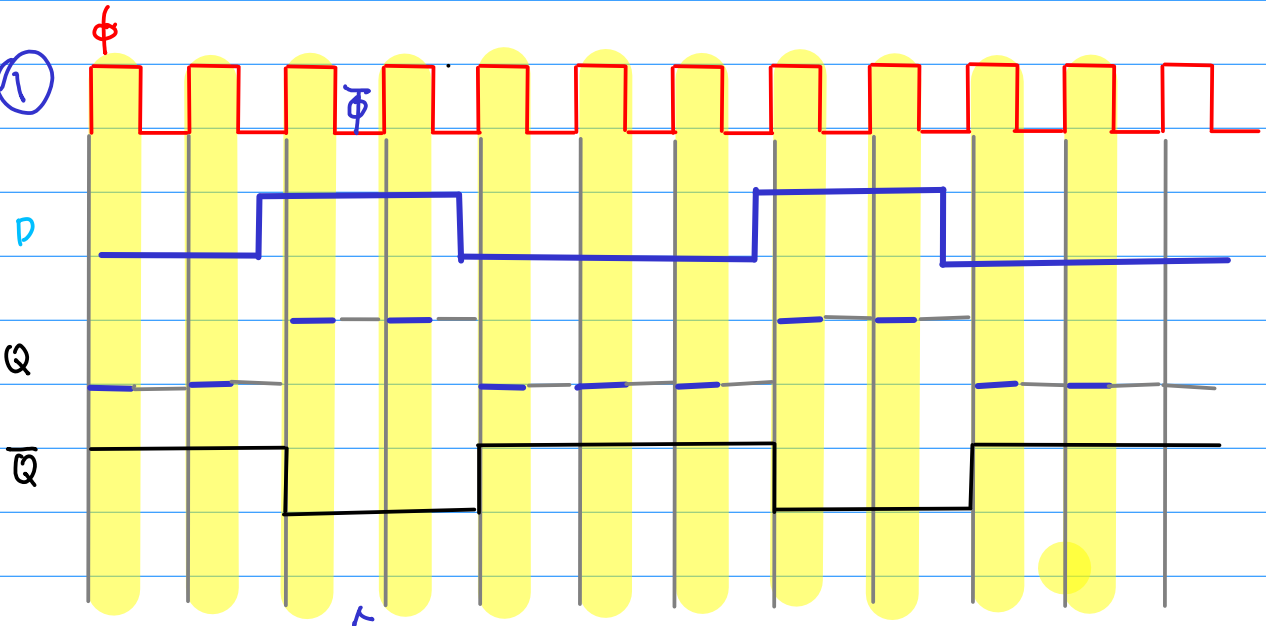
# Latch outputs for two different inputs

①



delayed ①

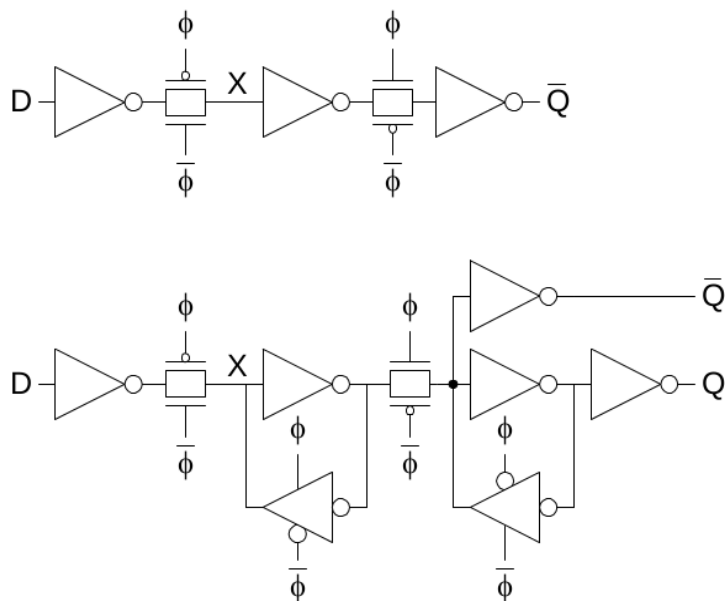
②  $\Rightarrow$





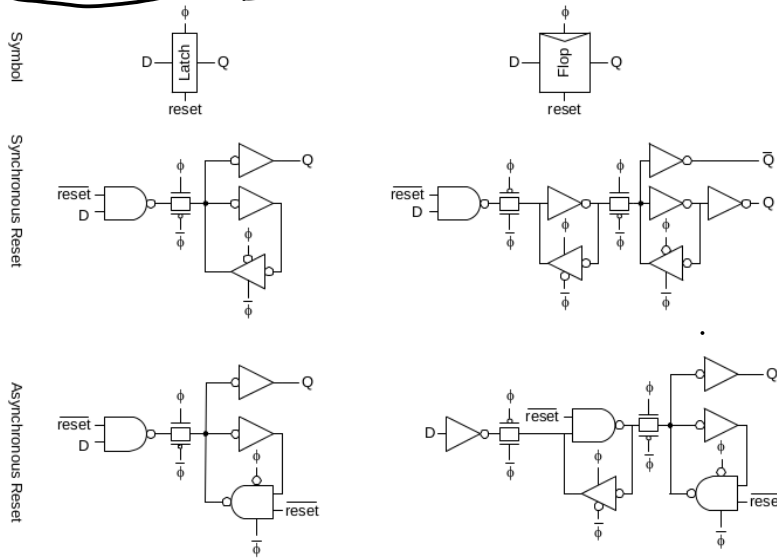
# Flip-Flop Design

- ❑ Flip-flop is built as pair of back-to-back latches

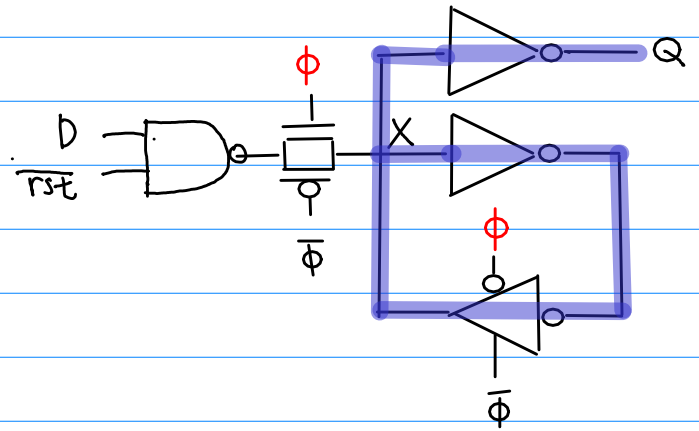
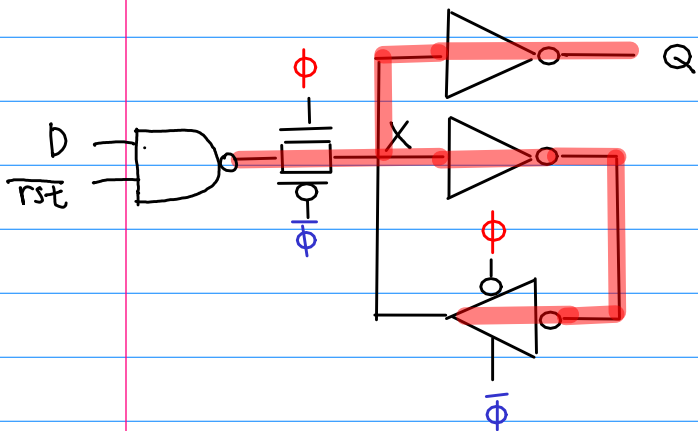


# Reset

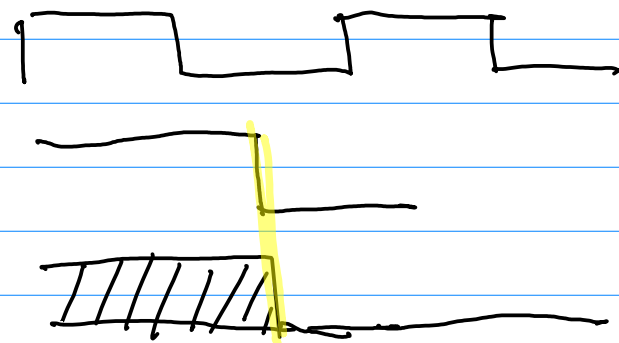
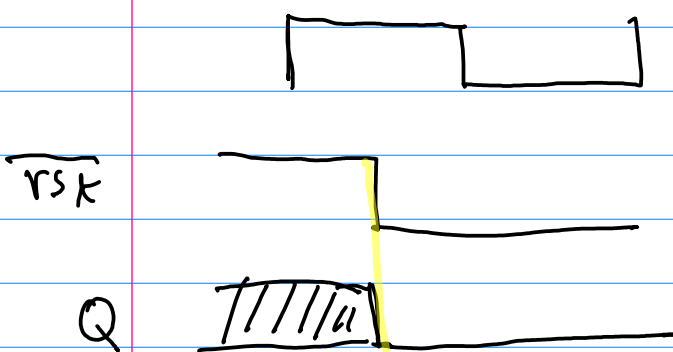
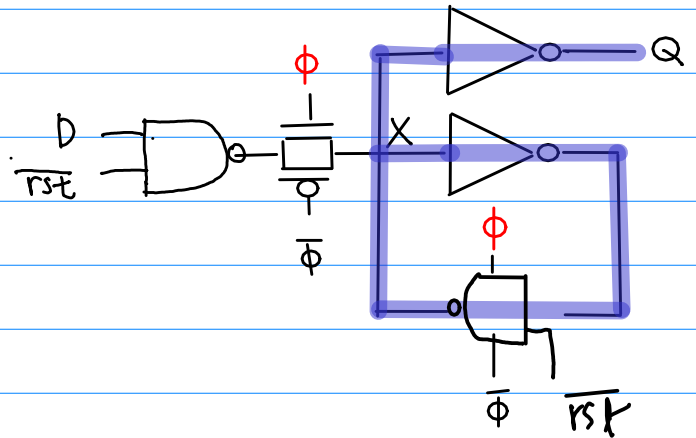
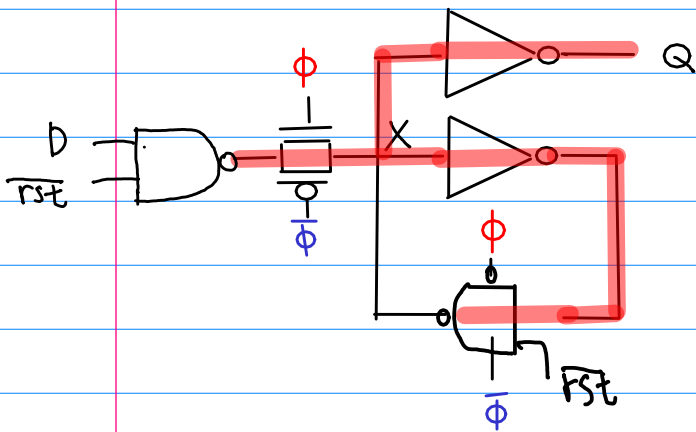
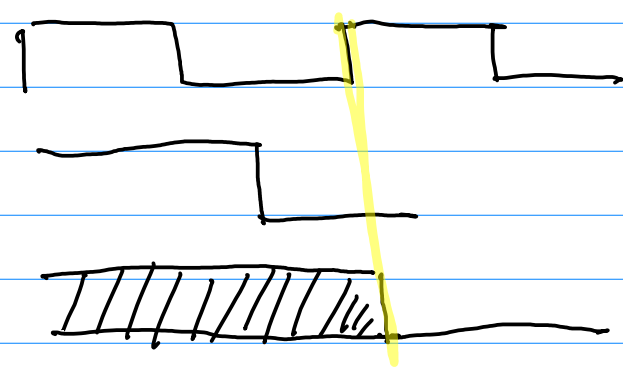
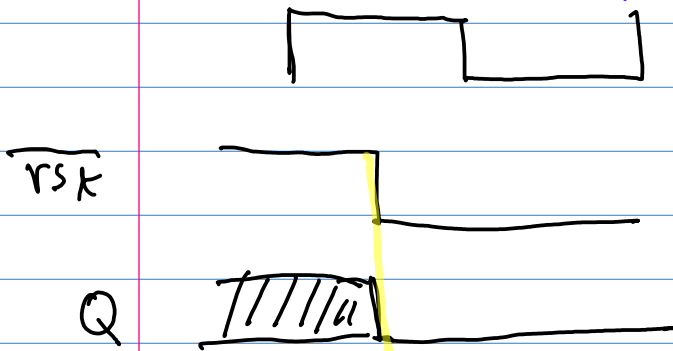
- ❑ Force output low when reset asserted
- ❑ Synchronous vs. asynchronous



# Synchronous / Asynchronous Reset

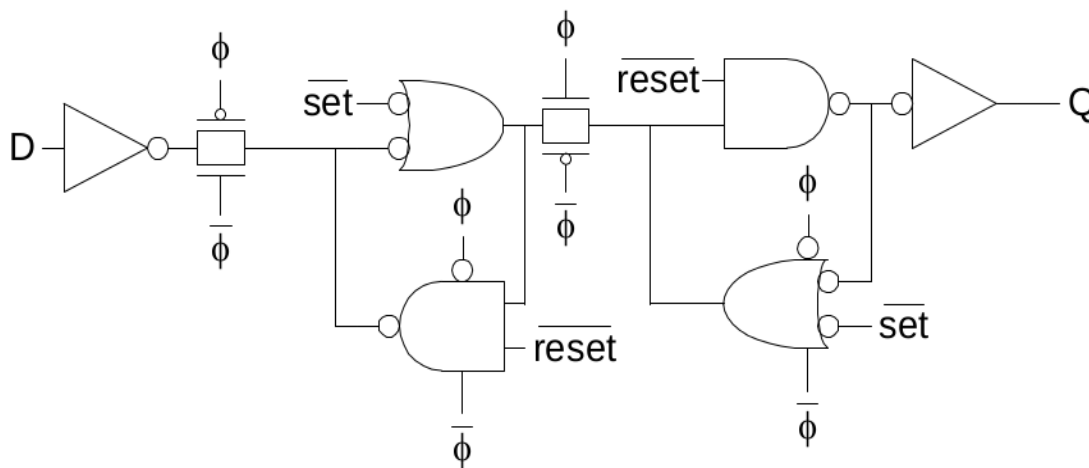


reset only for transparent

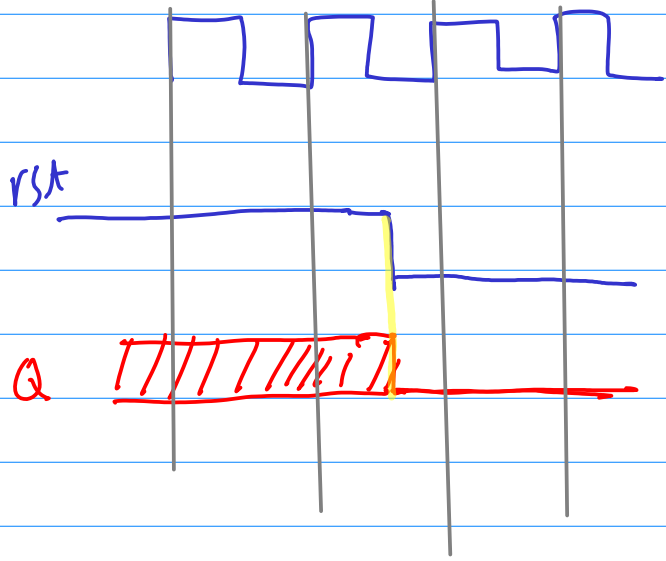
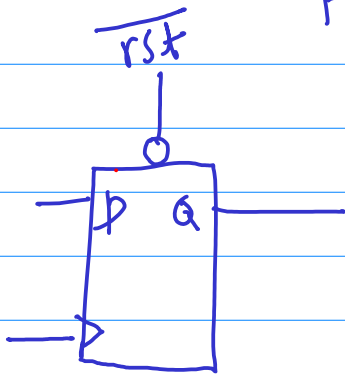


# Set / Reset

- ❑ Set forces output high when enabled
- ❑ Flip-flop with asynchronous set and reset



# FF w/ Asynchronous Reset



# FF w/ Synchronous Reset

