

# Microprogramming (3A)

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# Virtex FPGA RAM Memory

## LUT RAM

```
module ram16x1(q, a, d, we, clk);  
output q;  
input d;  
input [3:0] a;  
input clk, we;
```

```
reg mem [15:0];
```

```
always @(posedge clk) begin  
    if(we)  
        mem[a] <= d;  
end
```

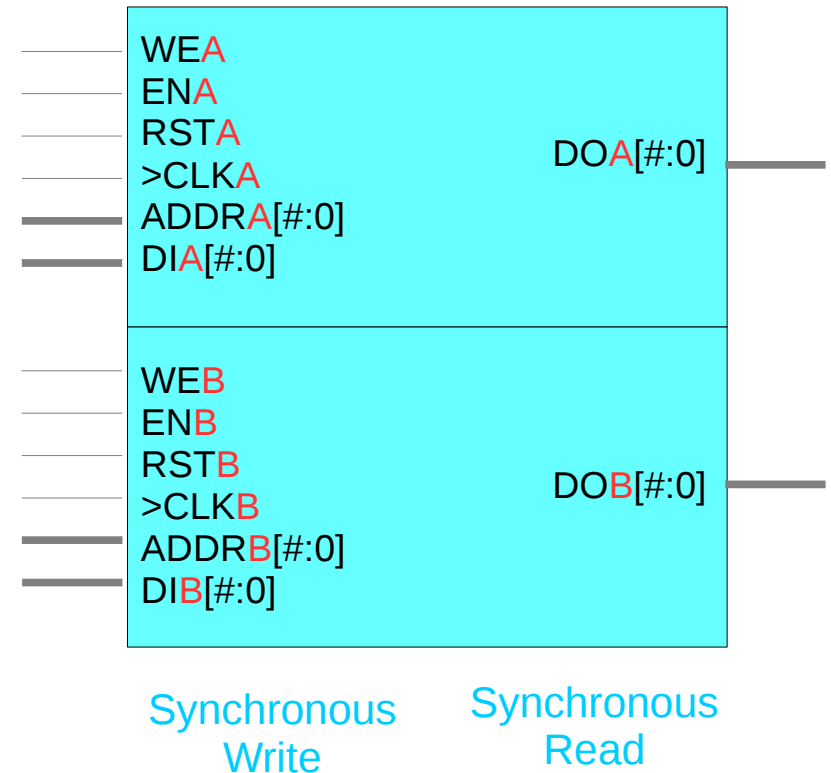
Synchronous  
Write

```
assign q = mem[a];
```

Asynchronous  
Read

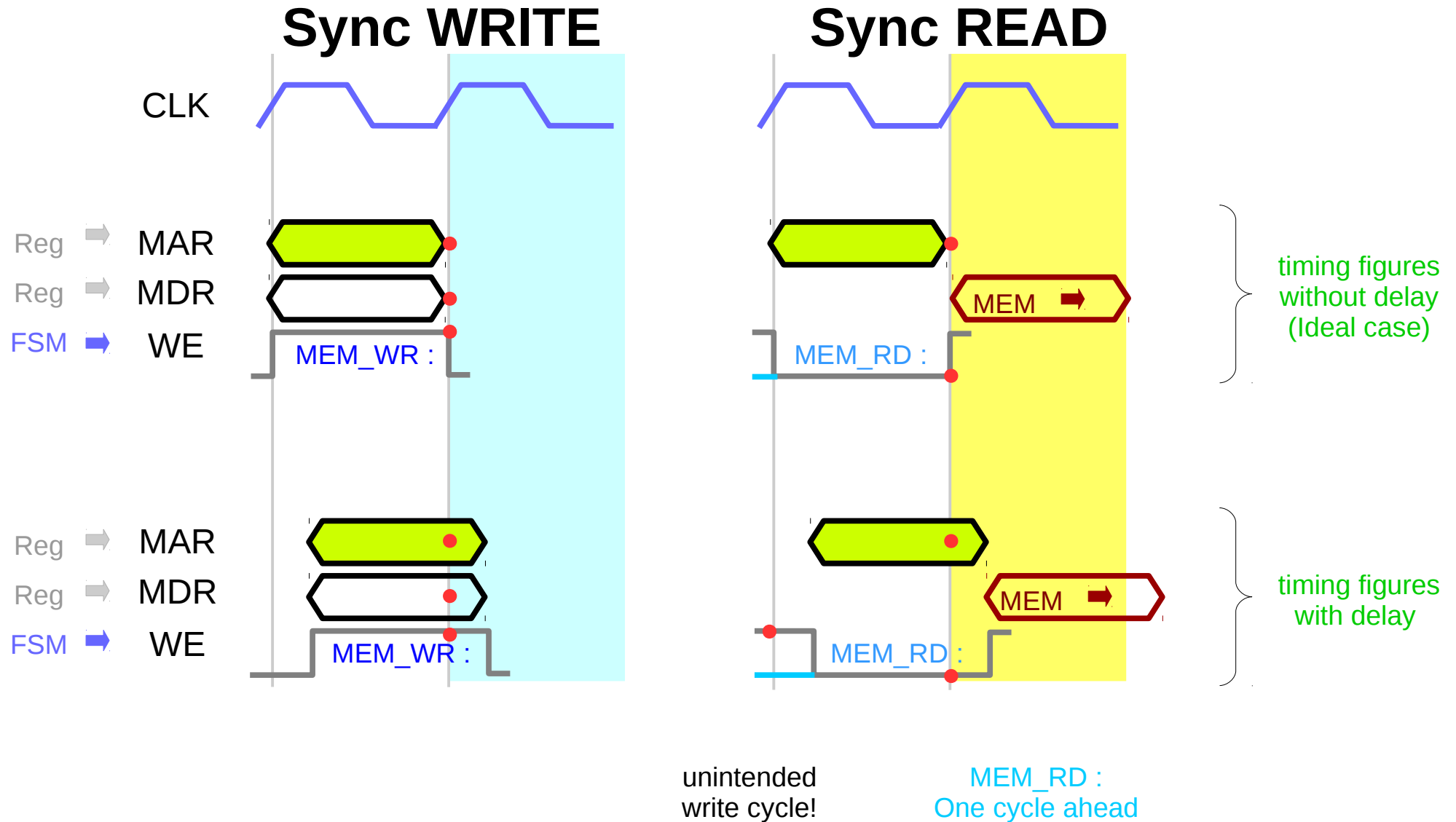
```
endmodule
```

## Block RAM



<http://www-inst.eecs.berkeley.edu/~cs150>

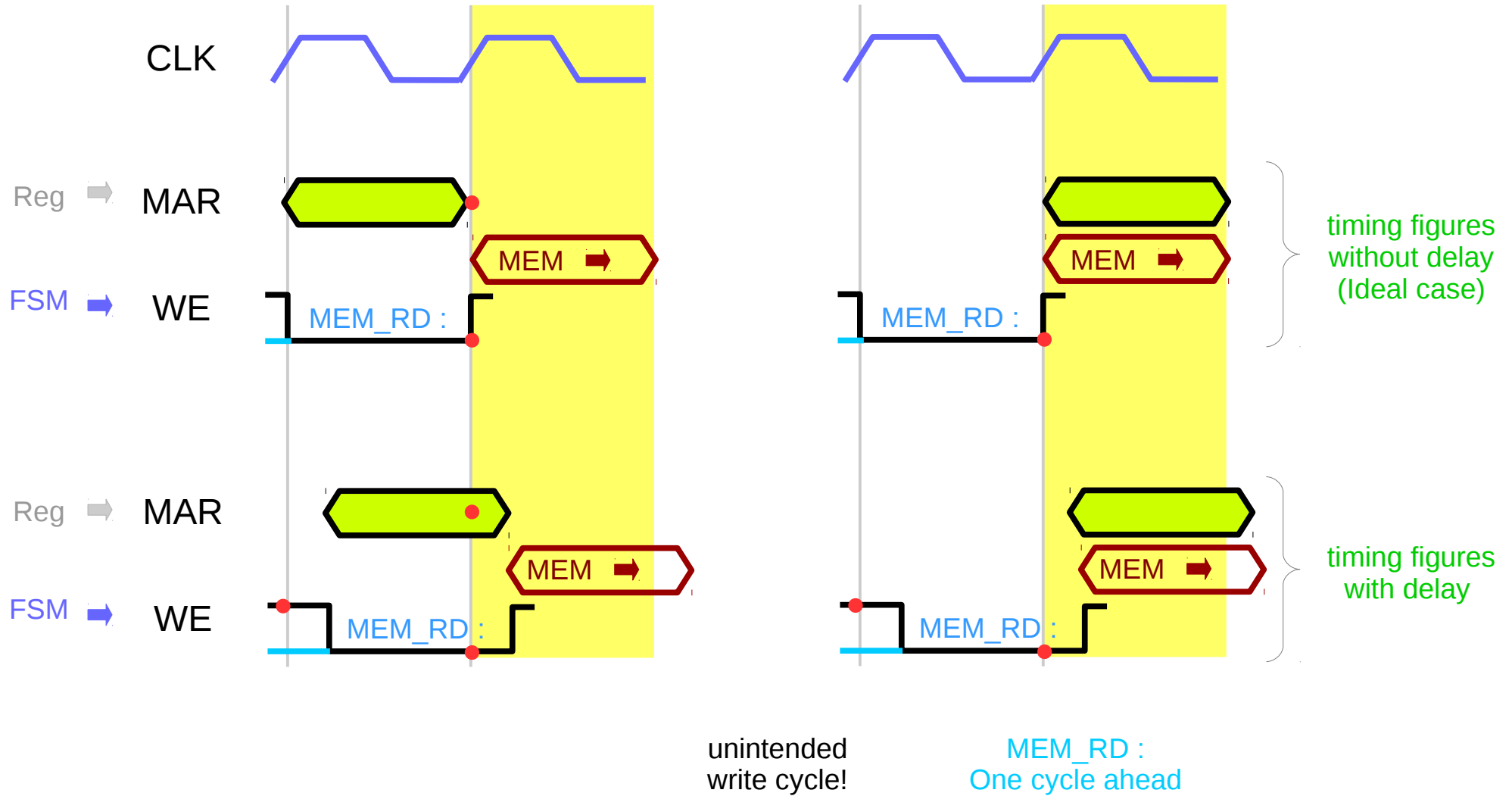
# Waveform Viewer Timing (2)



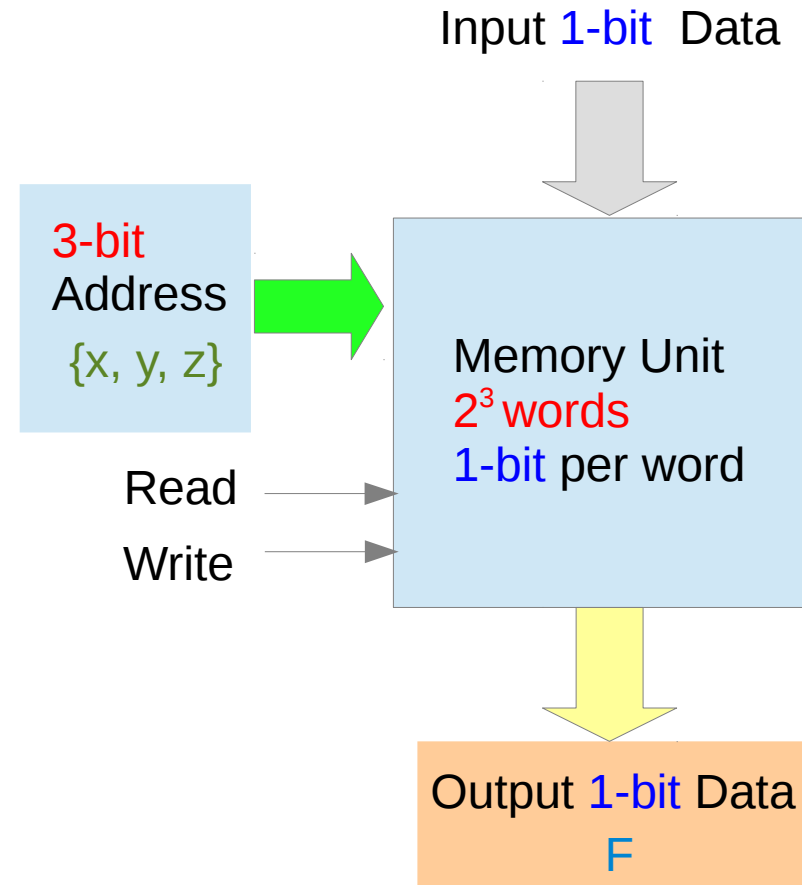
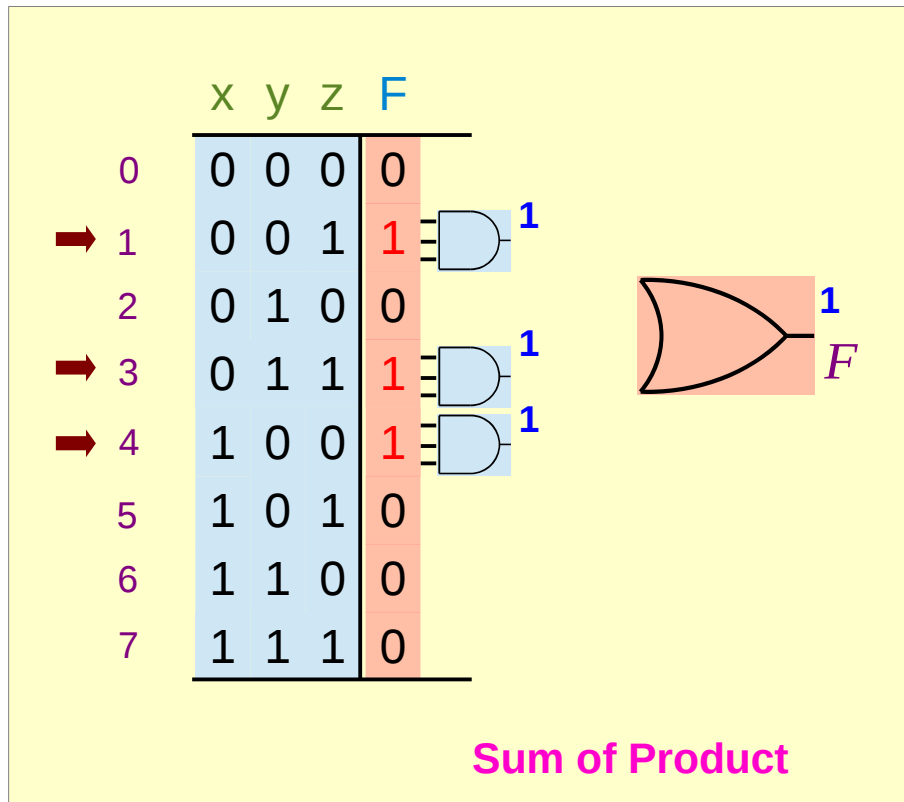
# Waveform Viewer Timing (3)

## Sync READ

## Async READ

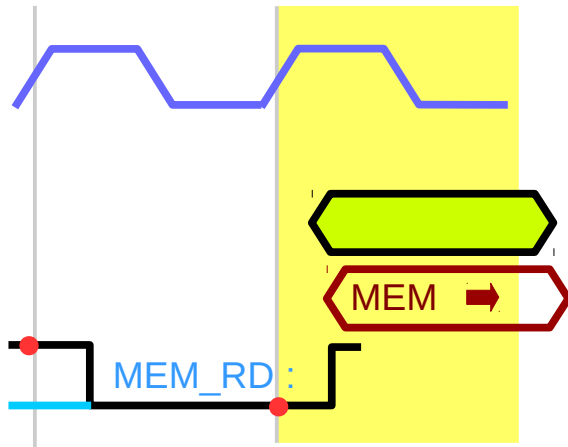


# LUT as a combination logic block



# LUT : Async Read

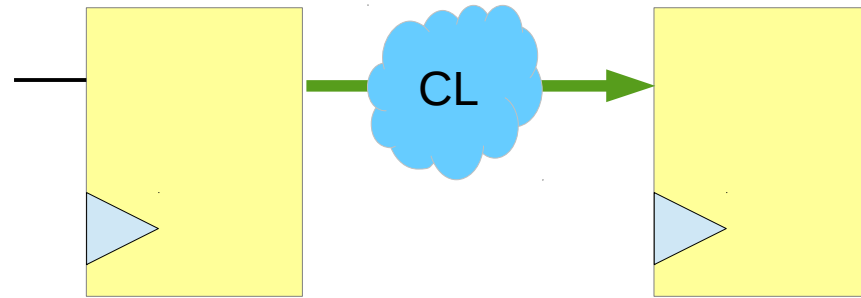
## Async READ



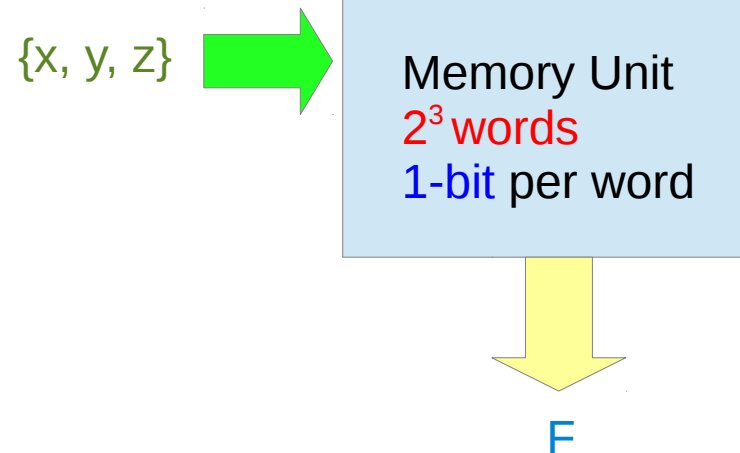
Address : Inputs  
Data : Outputs

The outputs available in the same cycle where the inputs are applied

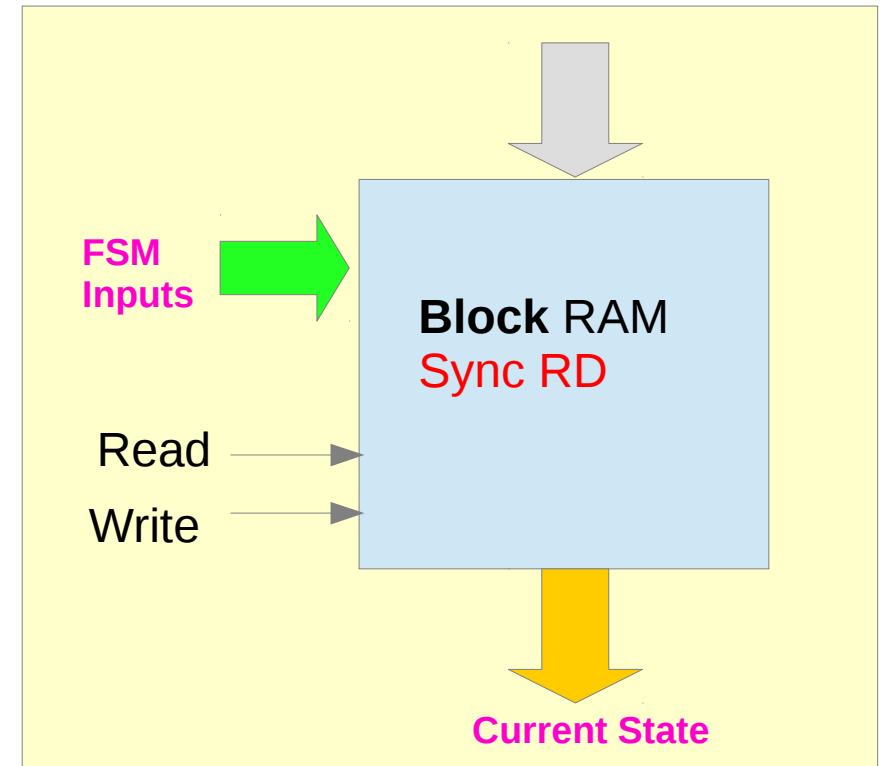
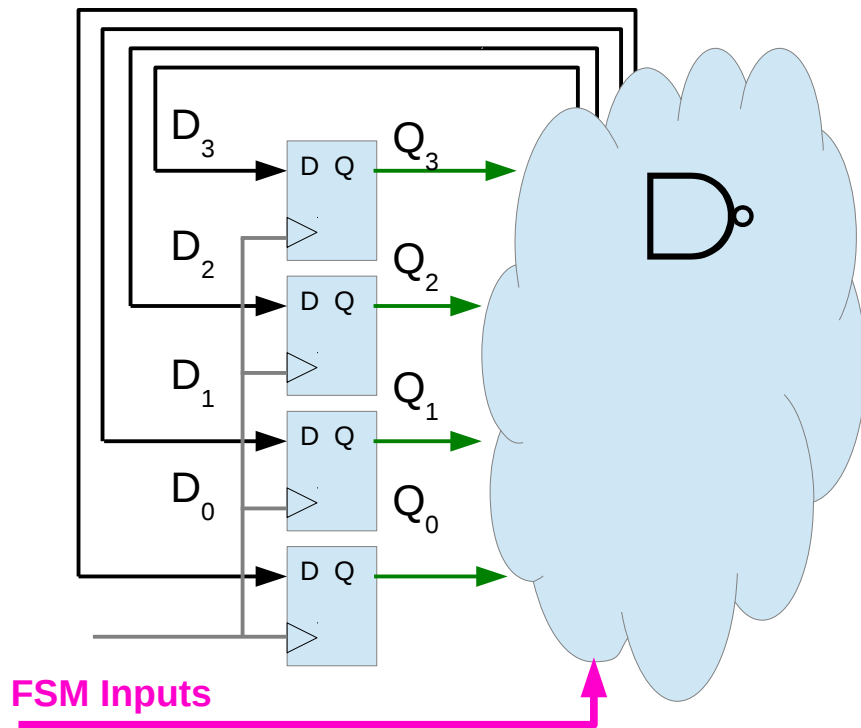
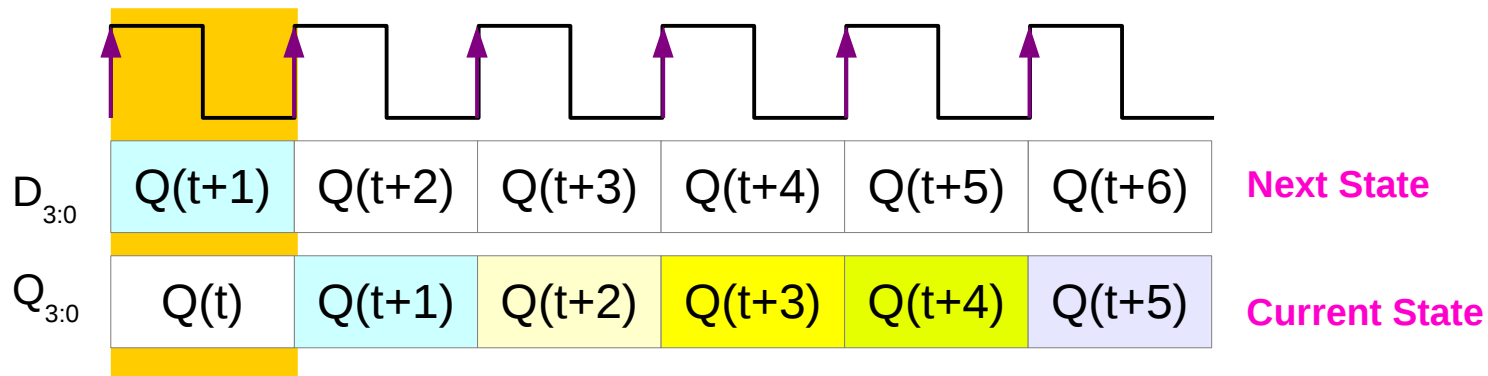
Combinational Logic Block :  
A set of Boolean Functions



LUT Data Write

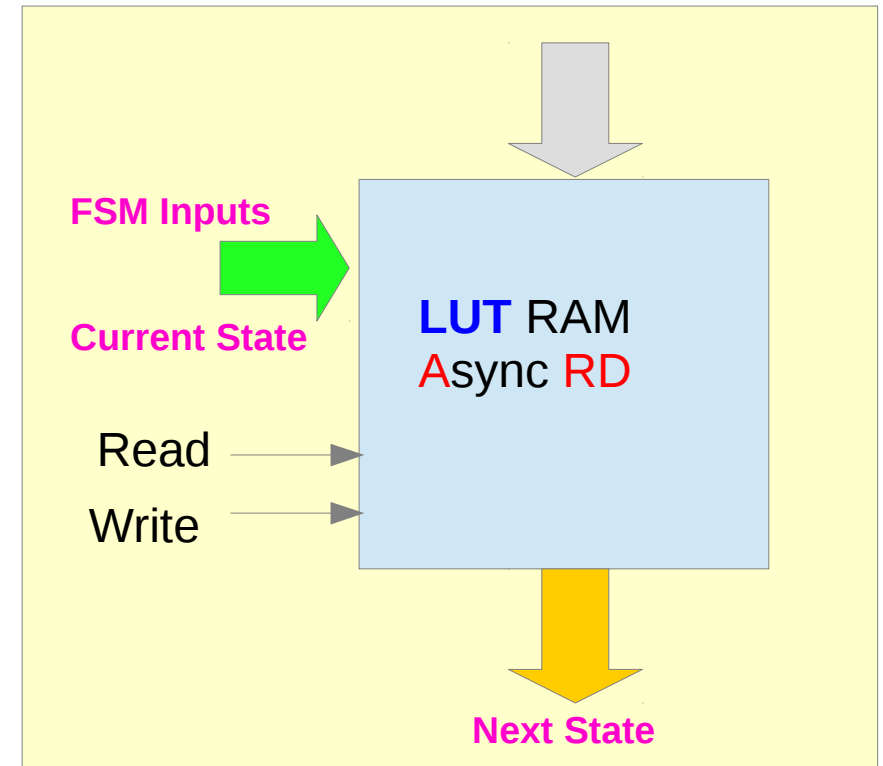
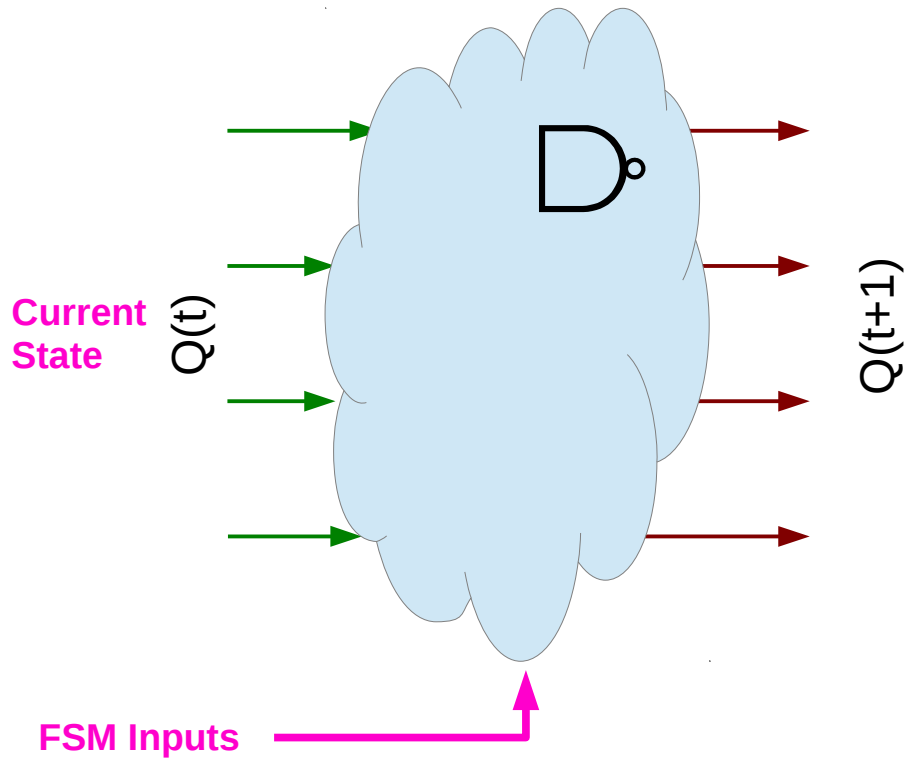
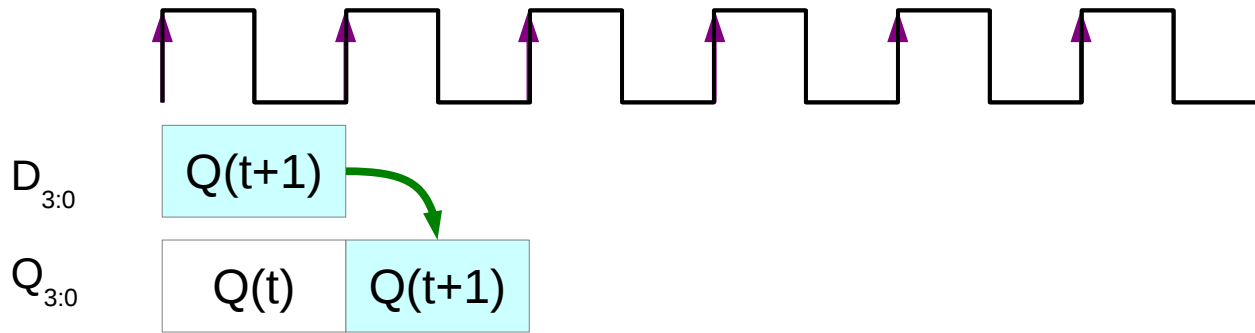


# Block RAM as a sequencer





# LUT as a next state logic



# Block RAM as a sequencer

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# Examples

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# Examples

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## References

- [1] <http://en.wikipedia.org/>
- [2] M. M. Mano, C. R. Kime, "Logic and Computer Design Fundamentals", 4<sup>th</sup> ed.
- [3] D.M. Harris, S. L. Harris, "Digital Design and Computer Architecture"
- [4] M. G. Arnold, "Verilog Digital Computer Design : Algorithms into Hardware", 1999
- [5] F.P. Prosser, D.E. Winkel, "The Art of Digital Design : An Intro to Top-Down Design", 2<sup>nd</sup> ed, 1986