

CMOS CLA (H.1)

20151118

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References

Some Figures from the following sites

[1] <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>

Weste & Harris Book Site

[2] en.wikipedia.org

[3] Digital Integrated Circuits : A Design Perspective,

Jan M. Rabaey,

(<http://bwracs.eecs.berkeley.edu/Classes/lcBook/>)

[4] Digital Electronics and Design with VHDL

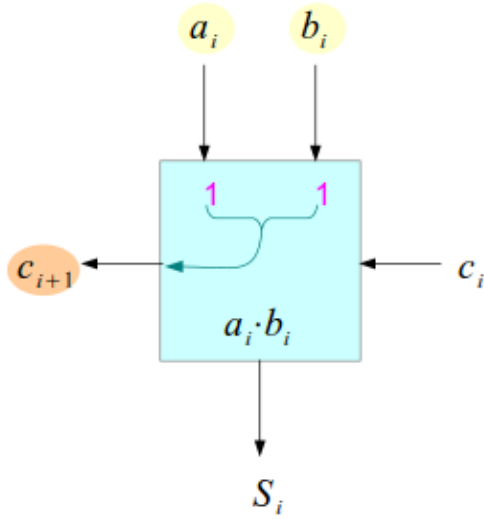
Pedroni

G and P

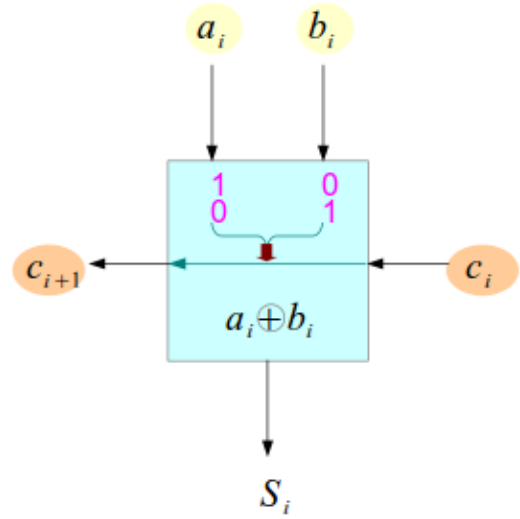
Generate $G_i = a_i \cdot b_i$

Propagate $P_i = a_i \oplus b_i$

$$c_{out} = G_i + P_i c_i$$



Generate c_{i+1}



Propagate c_i

Carry Equations

$$c_{i+1} = G_i + P_i c_i$$

$$c_1 = G_0 + P_0 c_0$$

$$c_2 = G_1 + P_1 c_1$$

$$c_3 = G_2 + P_2 c_2$$

$$c_4 = G_3 + P_3 c_3$$

$$c_1 = G_0 + P_0 c_0$$

$$c_2 = G_1 + P_1 [G_0 + P_0 c_0]$$

$$c_3 = G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_0]]$$

$$c_4 = G_3 + P_3 [G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_0]]]$$

$$G_0 + P_0 c_0 = c_1$$

$$G_1 + P_1 G_0 + P_1 P_0 c_0 = c_2$$

$$G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 c_0 = c_3$$

$$G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 c_0 = c_4$$

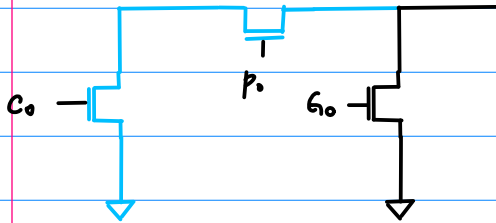
$$c_1 = G_0 + P_0 c_0$$

$$c_2 = G_1 + P_1 [G_0 + P_0 c_0]$$

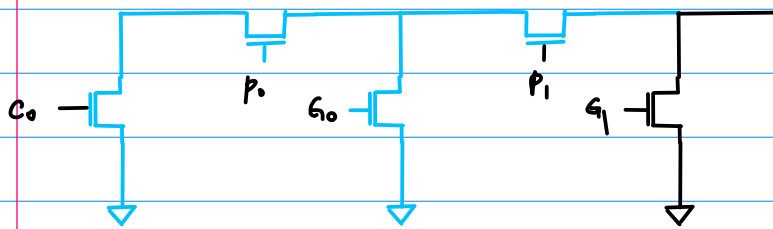
$$c_3 = G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_0]]$$

$$c_4 = G_3 + P_3 [G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_0]]]$$

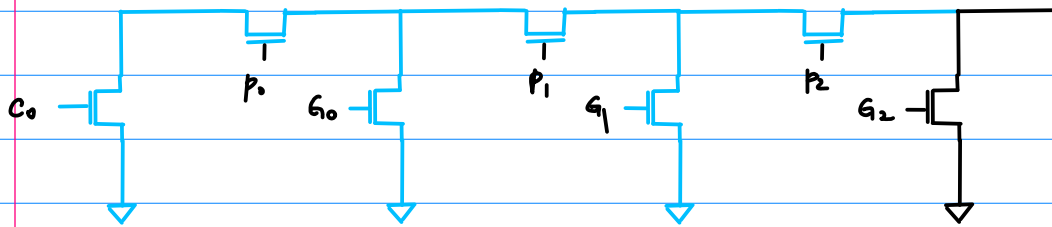
$$\overline{P_0 c_0 + G_0}$$



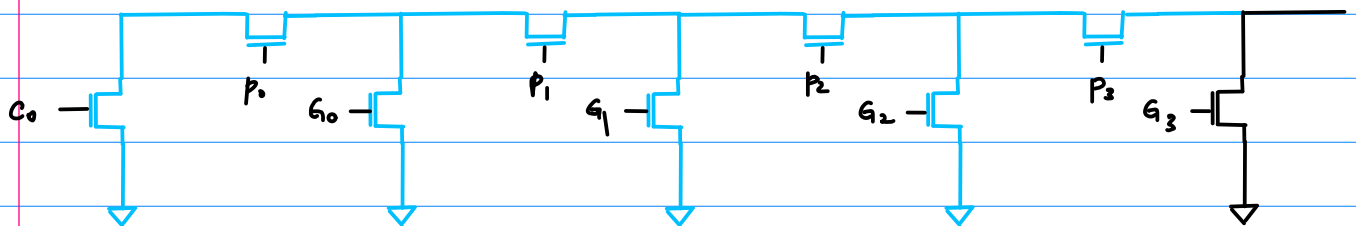
$$\overline{(G_0 + P_0 c_0) P_1 + G_1}$$



$$\overline{((G_0 + P_0 c_0) P_1 + G_0) P_2 + G_2}$$

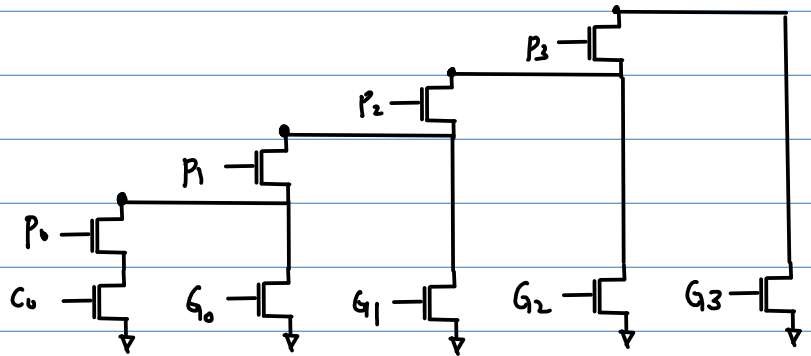


$$\overline{((G_0 + P_0 c_0) P_1 + G_0) P_2 + G_2) P_3 + G_3}$$

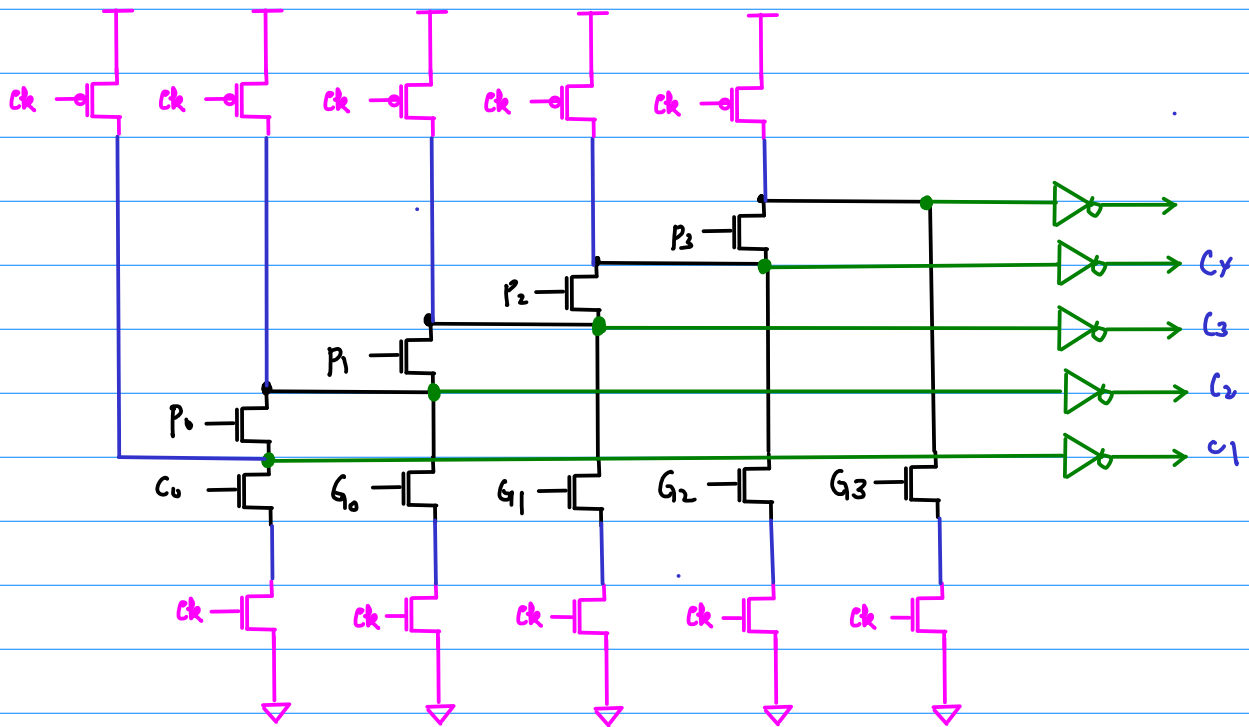
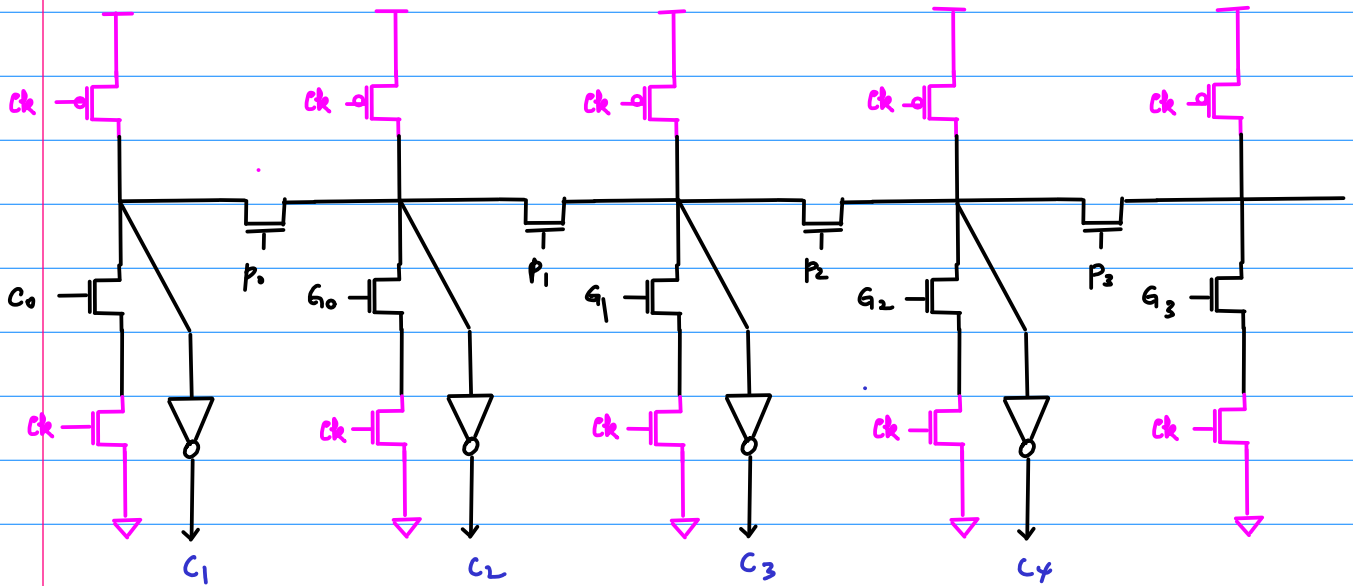


$$\frac{((G_0 + P_0 C_0) P_1 + G_0) P_2 + G_2}{((G_0 + P_0 C_0) P_1 + G_0) P_2 + G_2}$$

$$\frac{(G_0 + P_0 C_0) P_1 + G_1}{P_0 C_0 + G_0}$$



Manchester Carry-Chain Adder



4-bit CLA

