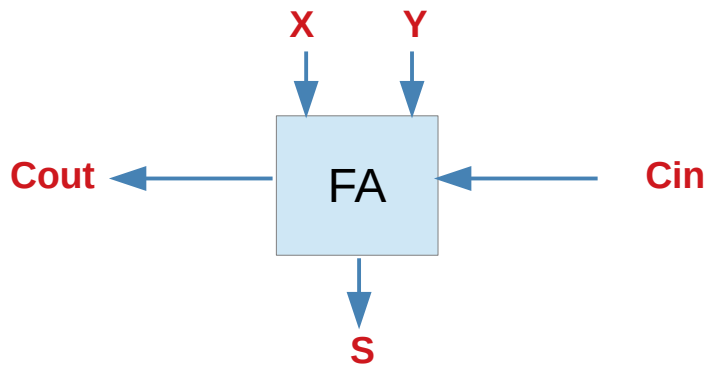# Carry Skip Adder (5A)

-
-

Young W. Lim
9/12/24

https://en.wikipedia.org/wiki/AND_gate
https://en.wikipedia.org/wiki/OR_gate
https://en.wikipedia.org/wiki/XOR_gate
https://en.wikipedia.org/wiki/NAND_gate

Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

Carry Kill, Propagate, Generate conditions (1)

| X	Y		
0	0	K	Kill (=$\overline{P}\overline{G}$)
0	1	P	Propagate
1	0	P	Propagate
1	1	G	Generate

https::/electronics.stackexchange.com/questions/21251/critical-path-for-carry-skip-adder

Carry Kill, Propagate, Generate conditions (2)

killed carry

killed carry

propagated carry

propagated carry

generated carry

generated carry
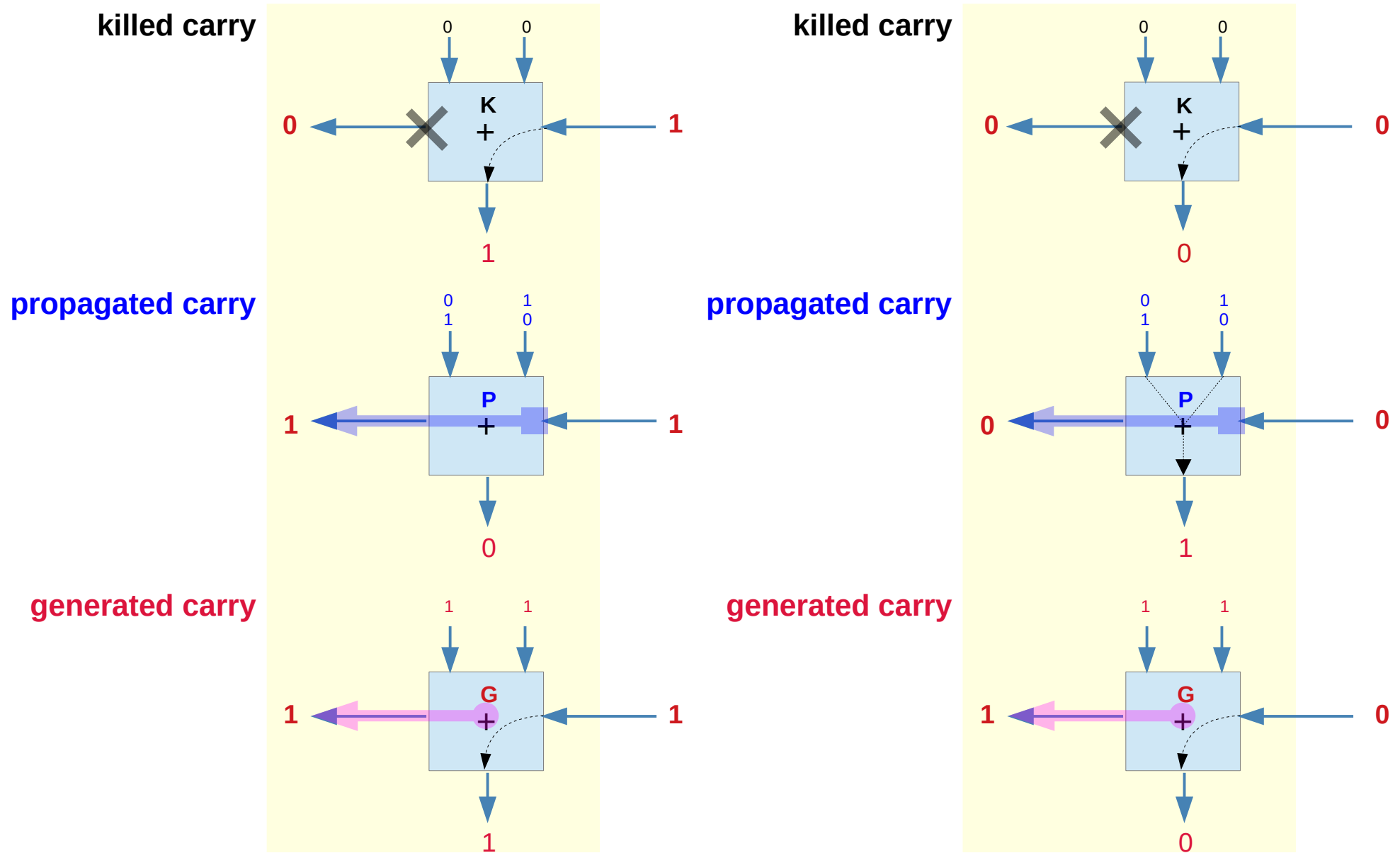
K, **P**, and **G** conditions in a 2-bit adder (1)

X	Y		
0	0	K	Kill (=$\overline{P}\,\overline{G}$)
0	1	P	Propagate
1	0	P	Propagate
1	1	G	Generate

X_0 Y_0 X_0 Y_0

FA1   FA0

C_{out} C_{in}

S_0 S_0
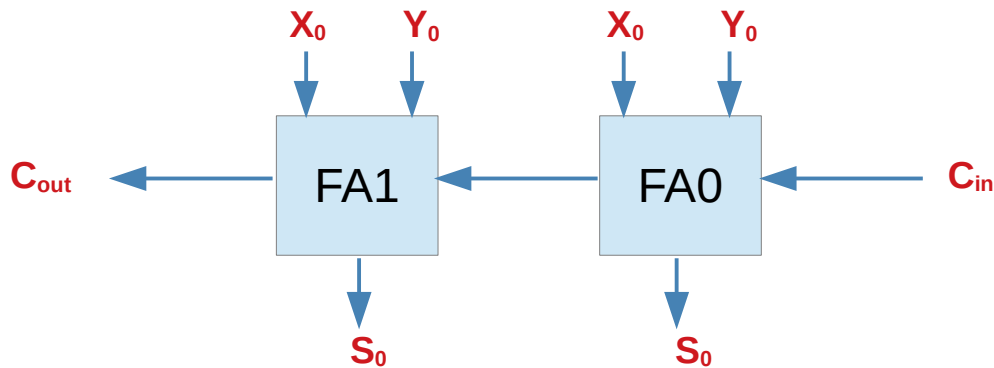
Unless the two FA's are in propagate mode,
the transition of Cin does not affect
the transition of Cout

Critical path – all FA's in propagate mode

Broken paths for any FA in other mode
- kill mode, generate mode

K, **P**, and **G** conditions in a 2-bit adder (2)

X	Y		
0	0	K	Kill (=$\overline{P}\overline{G}$)
0	1	P	Propagate
1	0	P	Propagate
1	1	G	Generate

C_{out} ← **FA1** ← **FA0** ← C_{in}
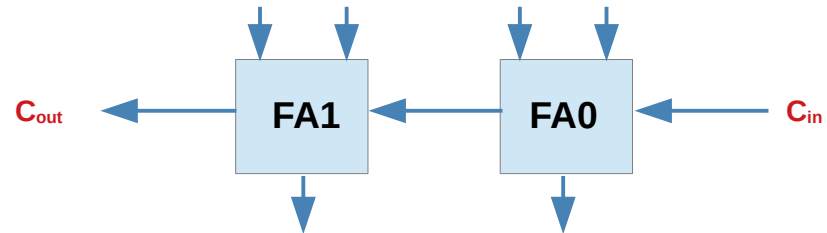
FA1	FA0	C_{in}
K	K	0
K	K	1
K	P	0
K	P	1
K	G	0
K	G	1
P	K	0
P	K	1
P	P	0
P	P	1
P	G	0
P	G	1
G	K	0
G	K	1
G	P	0
G	P	1
G	G	0
G	G	1

1. Cases when **FA1** is in the **K** mode

KK1

0   0
↓   ↓
0 ←✕ K +   0 ←✕ K + ← 1
     ↓   ↓
     0   1

KK0

0   0
↓   ↓
0 ←✕ K +   0 ←✕ K + ← 0
     ↓   ↓
     0   0

KP1

0   0
↓   ↓
0 ←✕ K + ← 1 P + ← 1
     ↓   ↓
     1   0

KP0

0   0
↓   ↓
0 ←✕ K + ← 0 P + ← 0
     ↓   ↓
     0   1

KG1

0   0   1   1
↓   ↓   ↓   ↓
0 ←✕ K + ← 1 G + ← 1
     ↓   ↓
     1   1

KG0
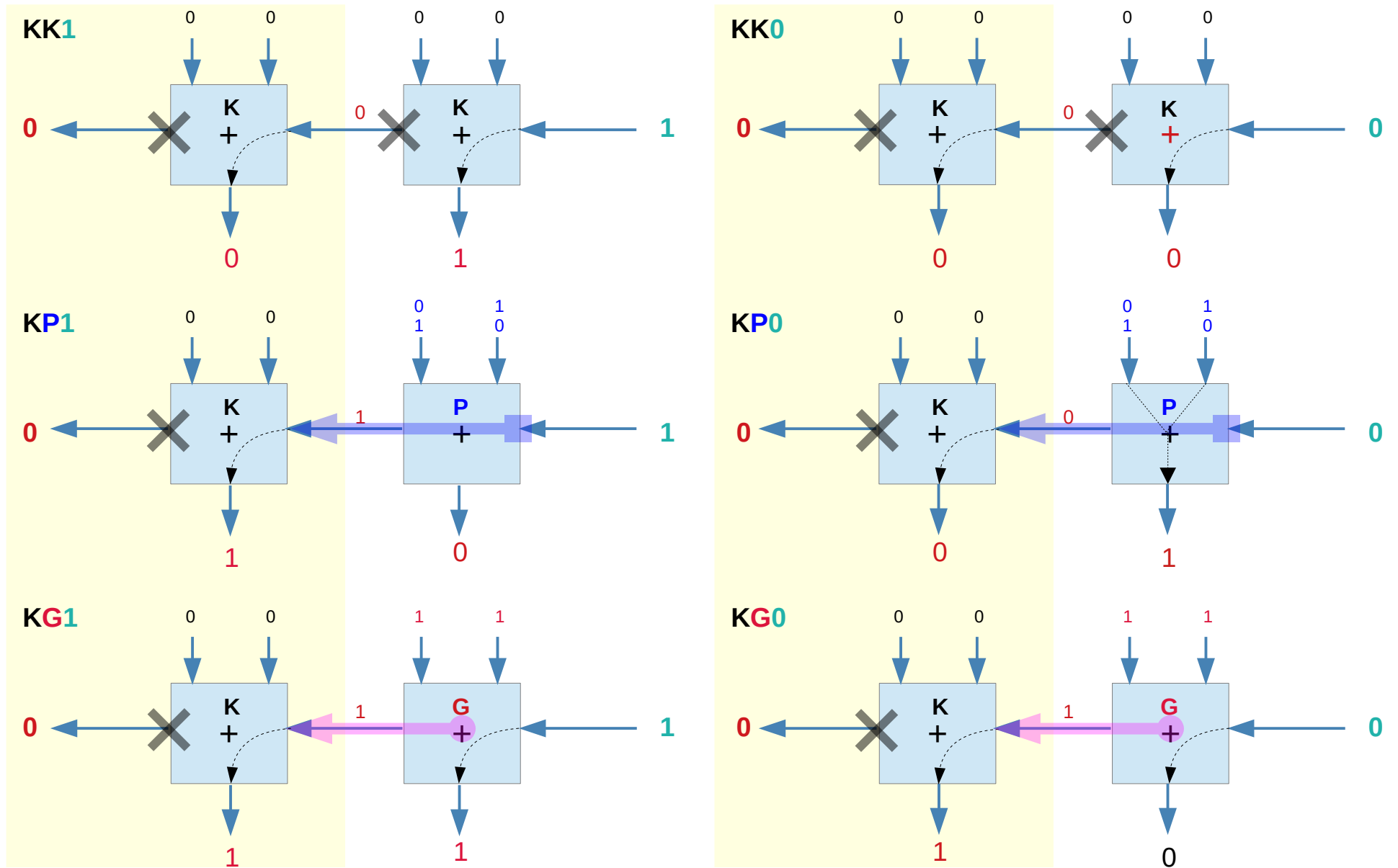
0   0   1   1
↓   ↓   ↓   ↓
0 ←✕ K + ← 1 G + ← 0
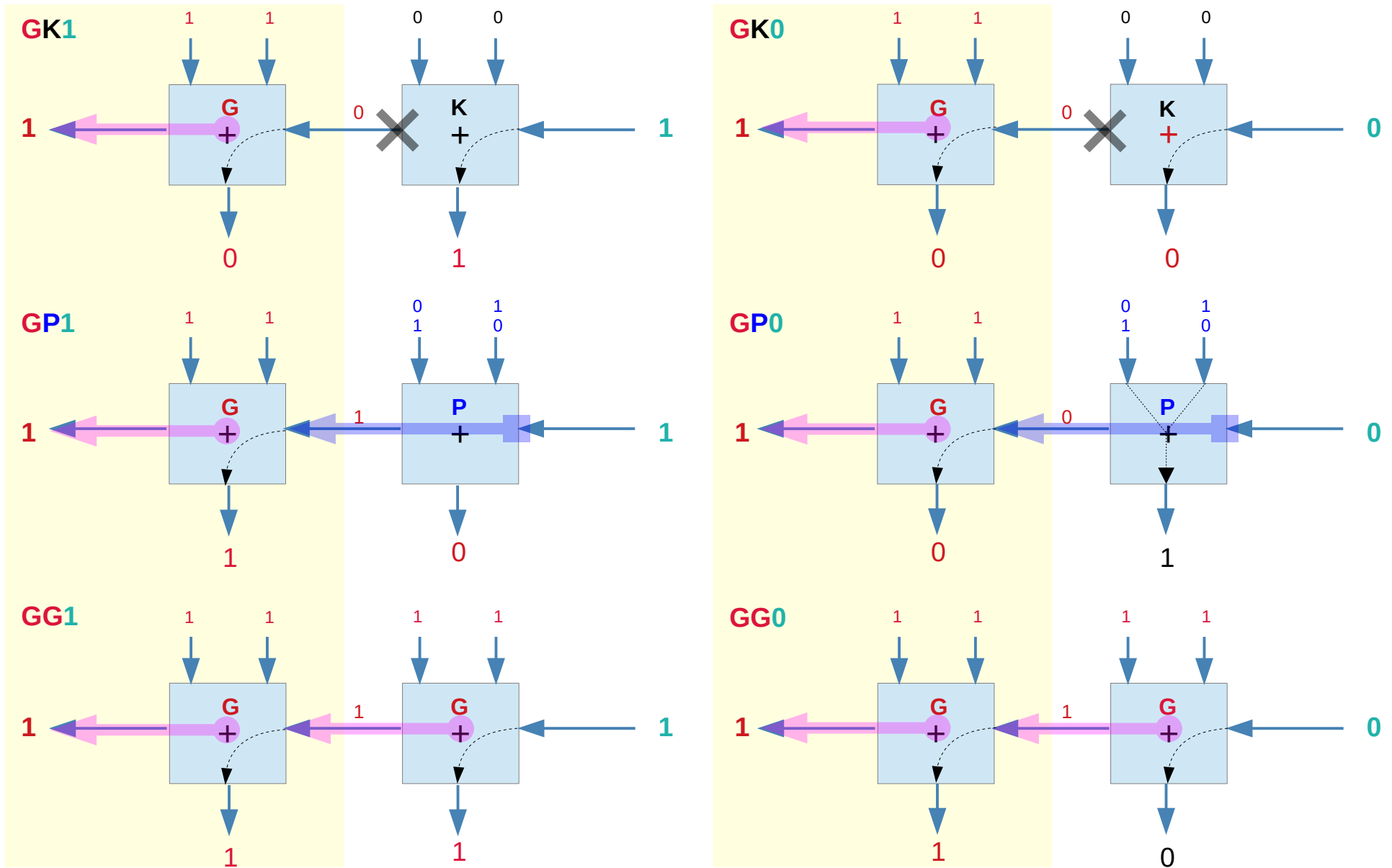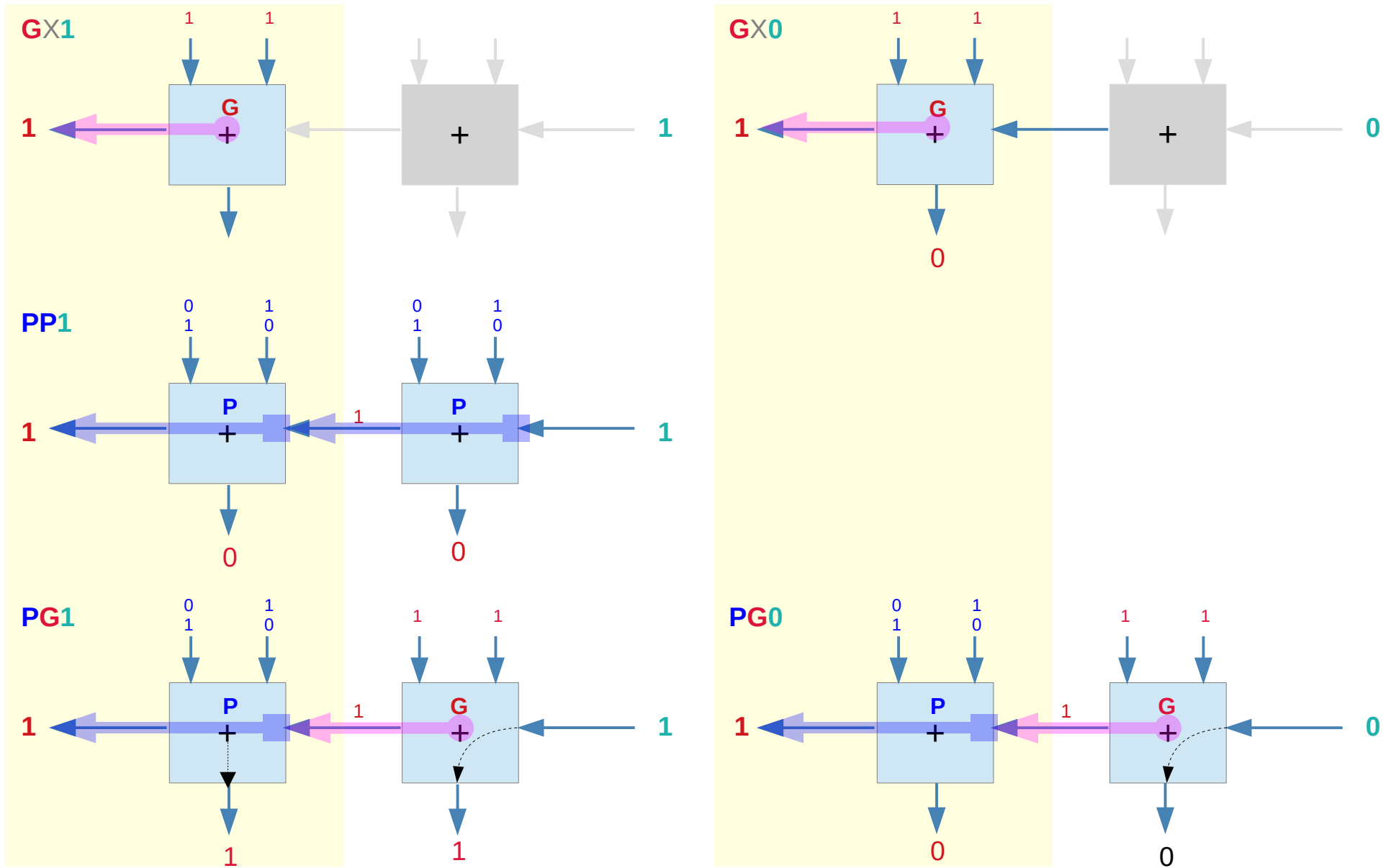   ↓   ↓
     1   0

2. Cases when **FA1** is in the **P** mode
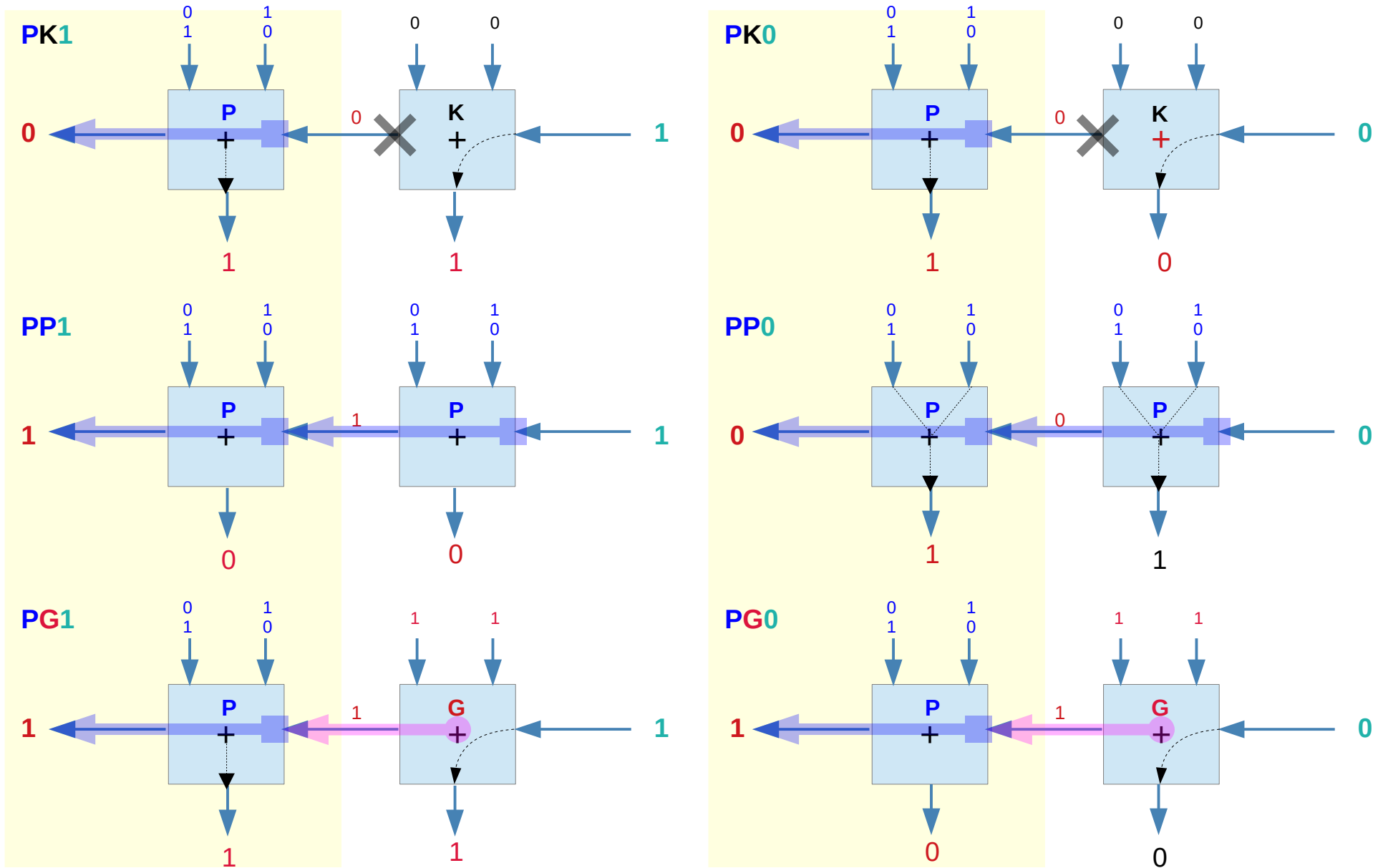
3. Cases when **FA1** is in the **G** mode

Cases for $C_{out} = 1$

GX**1**

1   1

G

1 ← +

0

GX**0**

1   1

G

1 ← +

1   0

0

PP1

0   1   0 1   1   0
1   0

P   **P**

1 ← + ← 1 + ← 1

0   0

PG1

0   1   0 1   1   1
1   0

P   **G**

1 ← + ← 1 + ← 1

1   1

PG0

0   1   0 1   1   1
1   0

P   **G**

1 ← + ← 1 + ← 0

0   0

Cases for $C_{out} = 0$

FA with P & G

$$s = p \oplus c$$

$$p \wedge c$$

$$c_{out} = g + p \wedge c$$

Half Adder

$$p = a \oplus b$$

$$g = a \wedge b$$

Half Adder

c

a

b
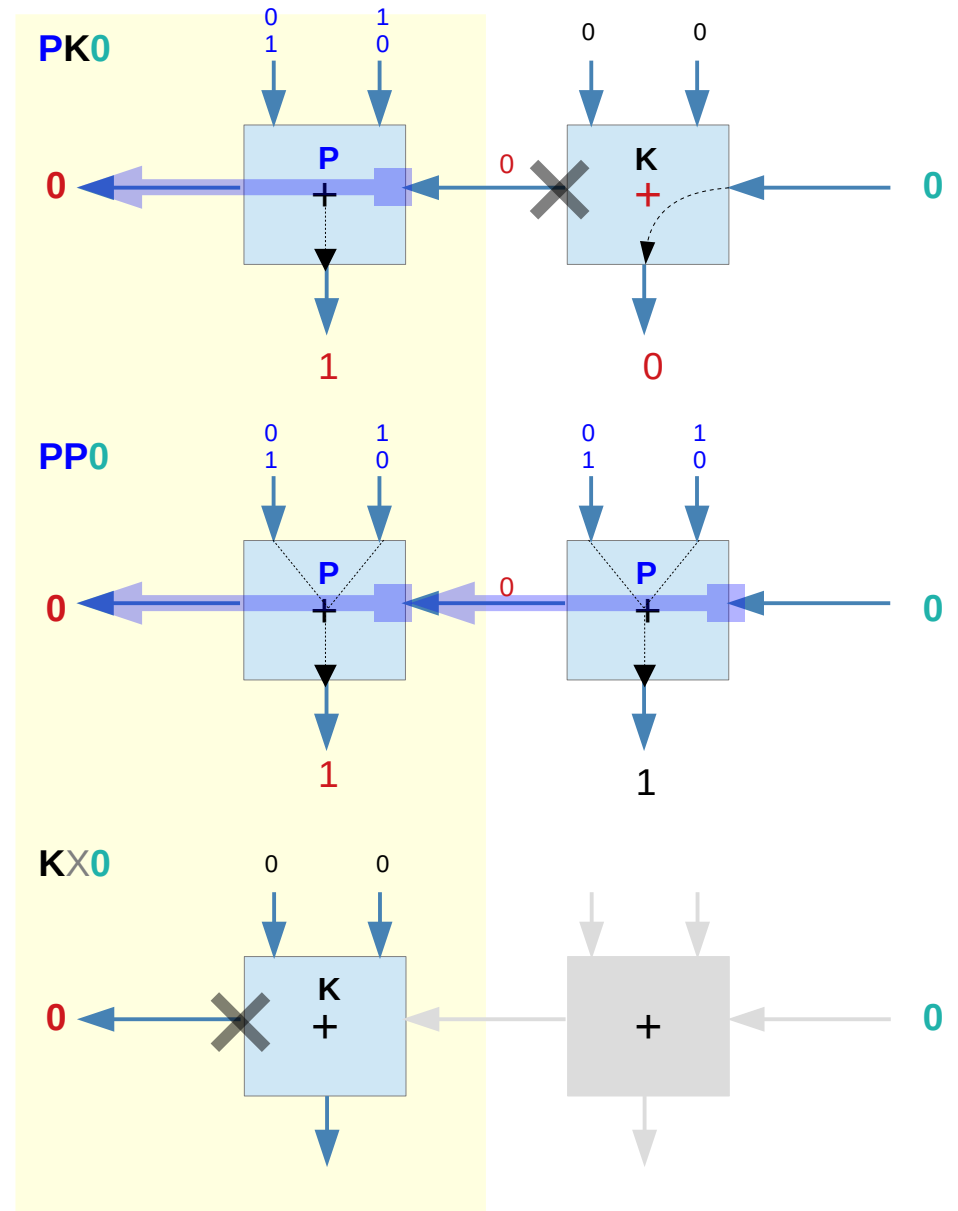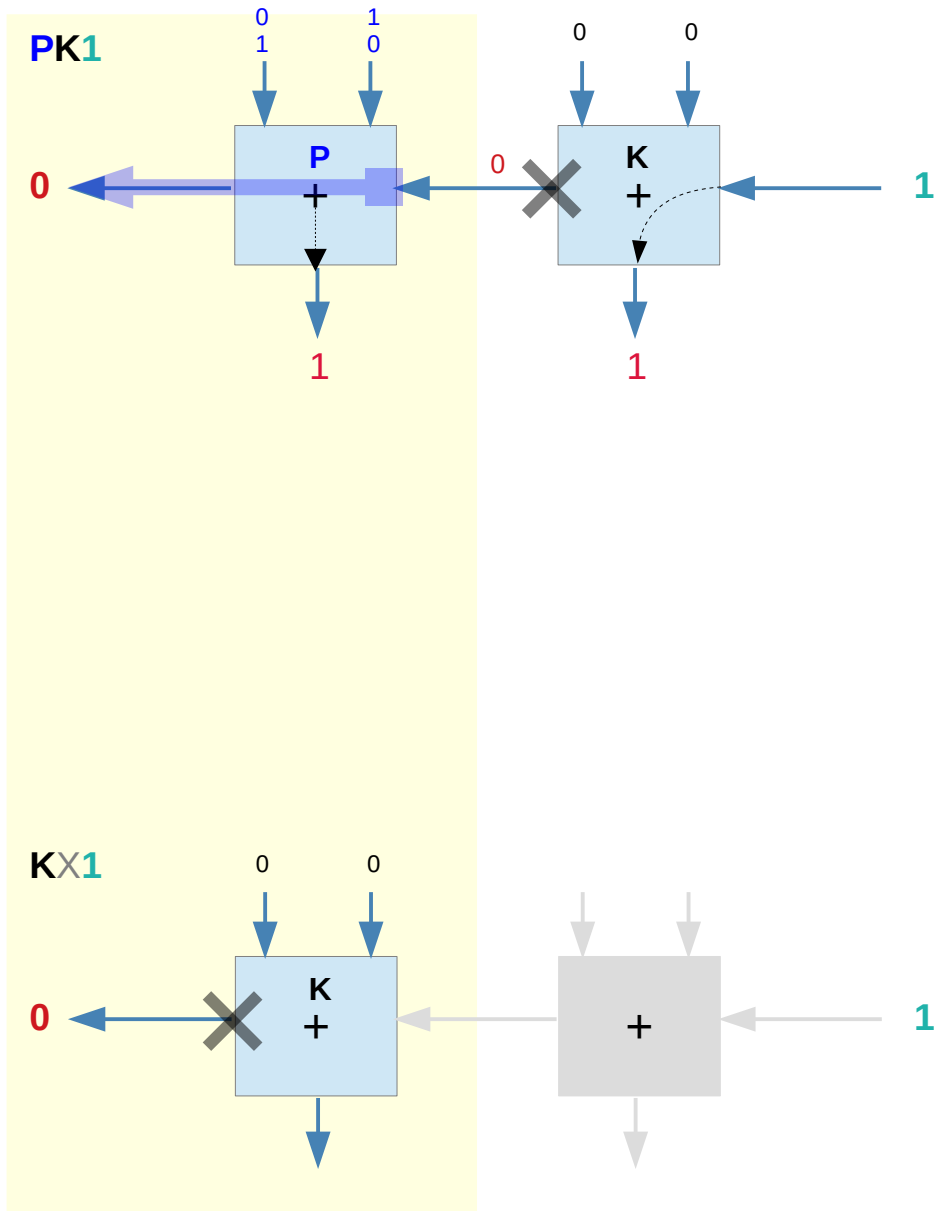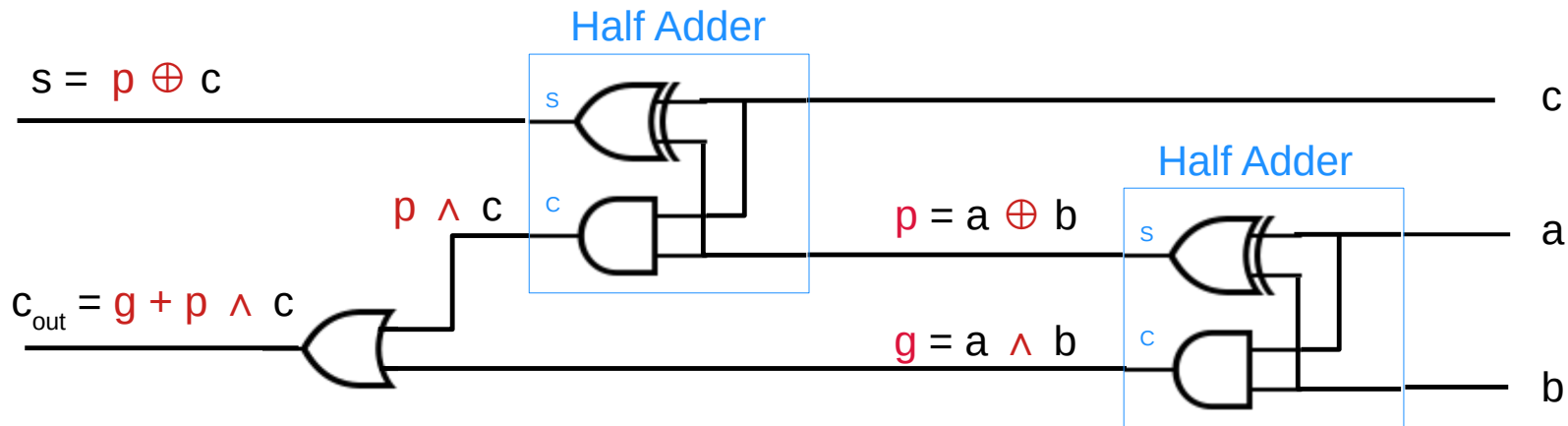
Half Adder
S = a ⊕ b
C = a ∧ b

a	b	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

p   S = a ⊕ b

g   C = a ∧ b

Half Adder

a

b
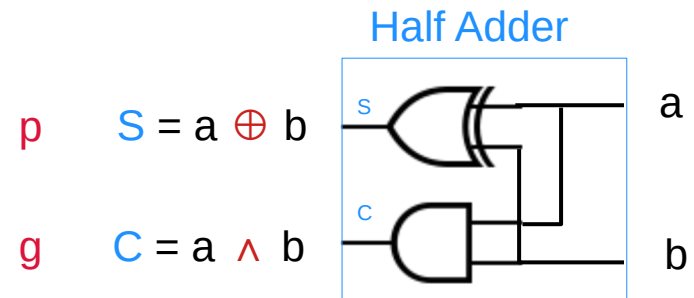
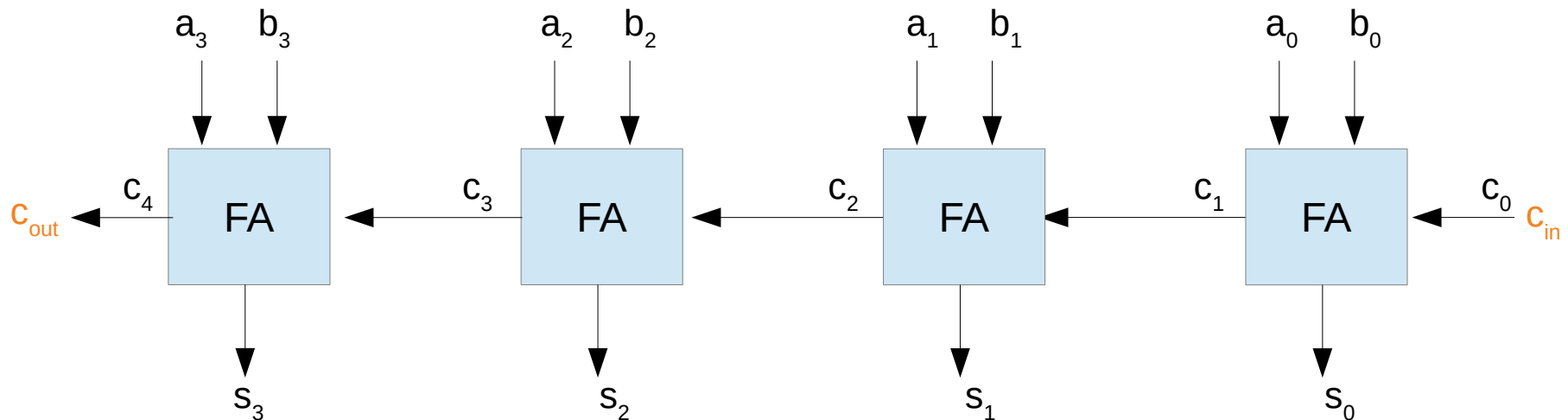Full adder with additional generate and propagate signals.

Ripple Carry Adder

$p_i = a_i \oplus b_i$

$g_i = a_i \wedge b_i$

$c_1 = g_0 + p_0 \wedge c_0$

$c_2 = g_1 + p_1 \wedge c_1$

$c_3 = g_2 + p_2 \wedge c_2$
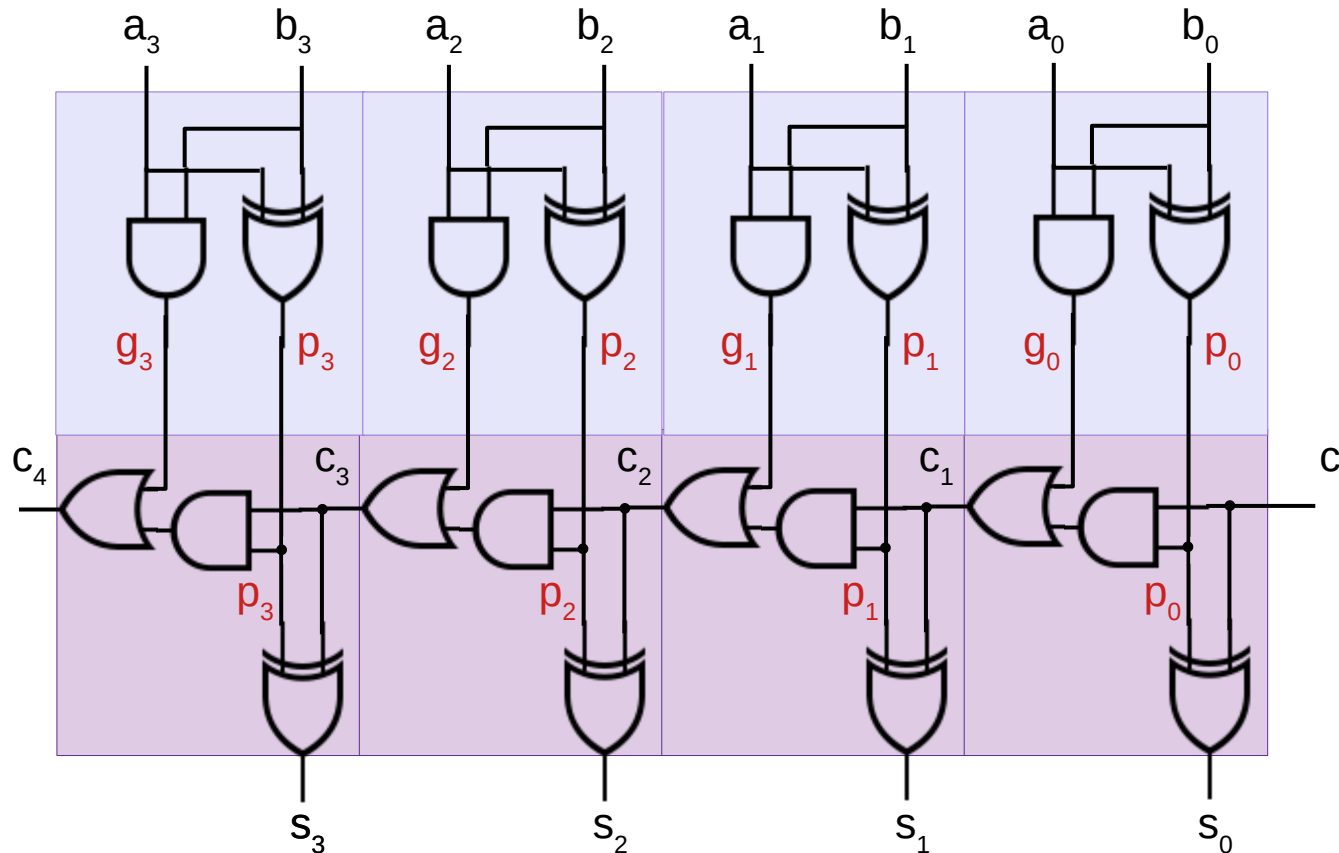
$c_4 = g_3 + p_3 \wedge c_3$

generated carry   propagated carry

https://en.wikipedia.org/wiki/Carry-skip_adder

4-bit Full Adder with P and G

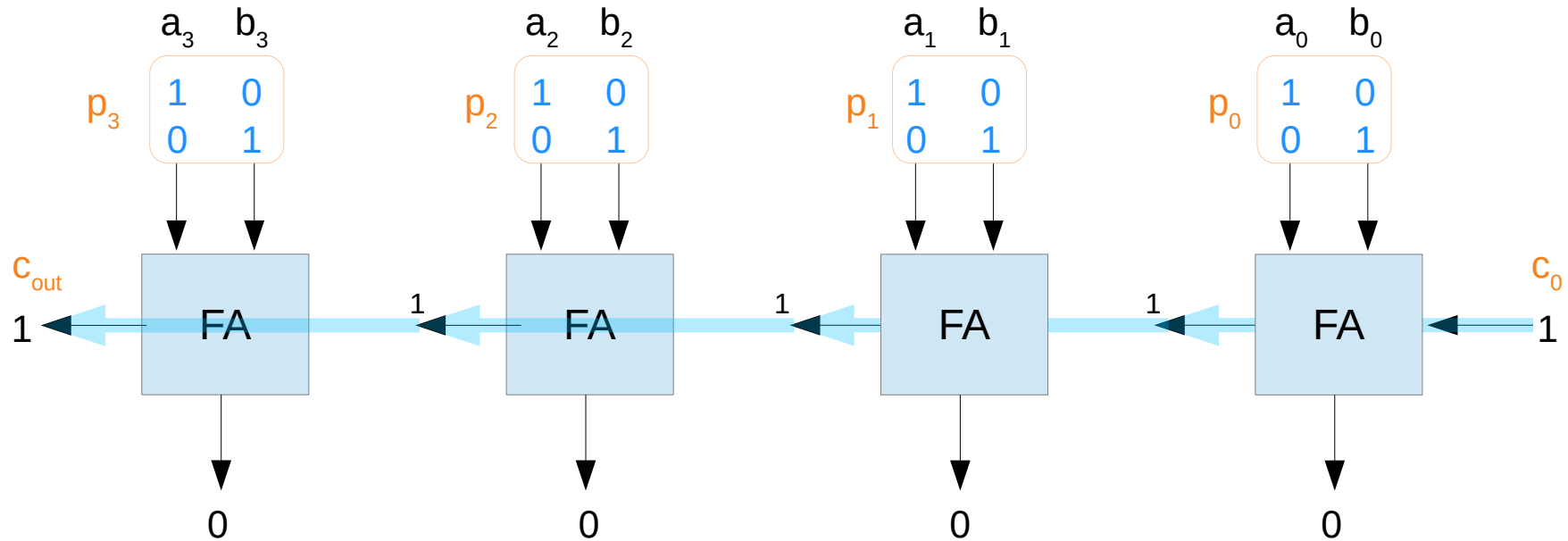**Half Adder**

$p_i = a_i \oplus b_i$

$g_i = a_i \wedge b_i$

Half Adder

$c_{i+1} = g_i + p_i \wedge c_i$
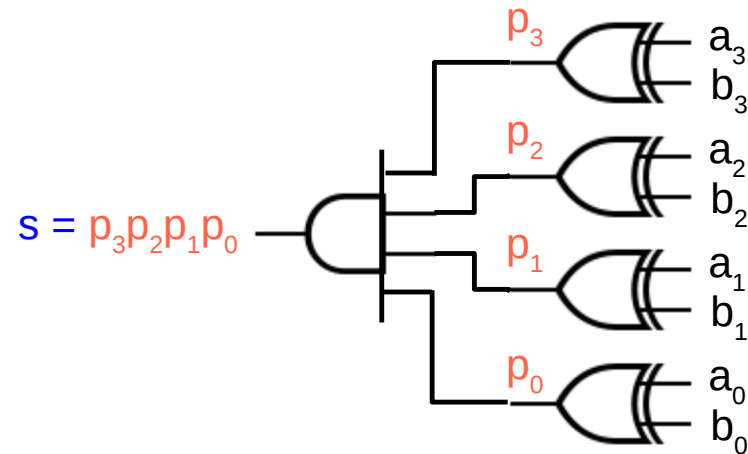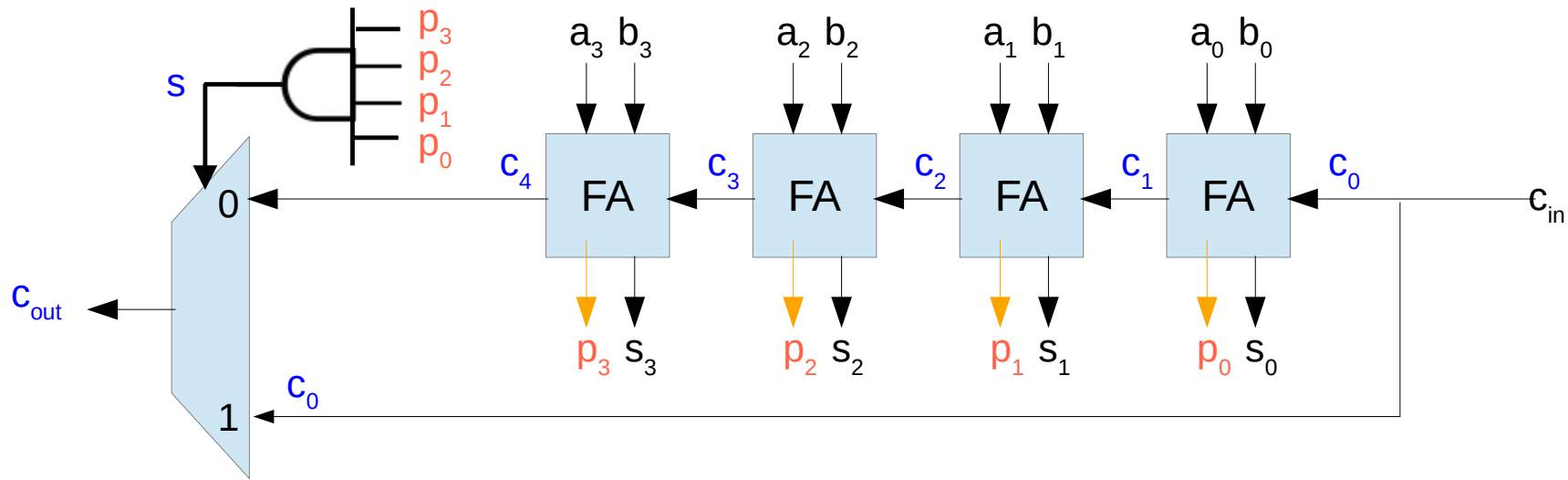
$s_i = p_i \oplus c_i$

C$_0$ propagation condition

a_3 b_3 $\quad$ a_2 b_2 $\quad$ a_1 b_1 $\quad$ a_0 b_0

p_3
1	0
0	1

p_2
1	0
0	1

p_1
1	0
0	1

p_0
1	0
0	1

c_{out}

1 ← FA ←1 FA ←1 FA ←1 FA ← 1

c_0

0 $\quad$ 0 $\quad$ 0 $\quad$ 0

c_0 can be propagated to c_{out} only when s = 1

$s \quad = p_3 \wedge p_2 \wedge p_1 \wedge p_0 = p_{[3:0]}$
$= (a_3 \oplus b_3)$
$\wedge (a_2 \oplus b_2)$
$\wedge (a_1 \oplus b_1)$
$\wedge (a_0 \oplus b_0)$

$s = p_3p_2p_1p_0$

p_3 a_3 b_3
p_2 a_2 b_2
p_1 a_1 b_1
p_0 a_0 b_0

https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder

The n-bit Carry Skip Adder consists of

a n-bit **carry-ripple-chain**,
a n-input **AND-gate** and
one **multiplexer**.

a multiplexer switches
either the last carry-bit c_n or the carry-in c_0
to the carry-out signal c_{out}

$s = p_3 \wedge p_2 \wedge p_1 \wedge p_0 = p_{[3:0]}$

when $s = 1$, $c_{out} \leftarrow c_0$

otherwise, internally generated carries
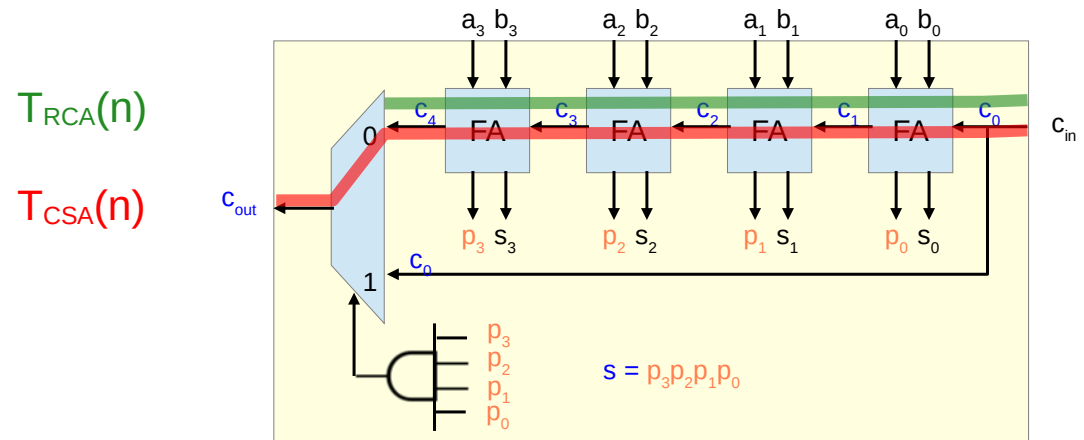can be propagated to $c_{out} \leftarrow c_4$

https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder

$$s = p_3 p_2 p_1 p_0$$

https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder

The critical path of a Carry Skip Adder begins at the first full adder,
passes through all adders and ends at the sum bit s_{n-1}

Since a <u>single</u> *n-bit* Carry Skip Adder has <u>no</u> real speed <u>benefit</u>
compared to a *n-bit* Ripple Carry Adder

$$T_{CSA}(n) = T_{RCA}(n)$$

$T_{RCA}(n)$

$T_{CSA}(n)$

Carry Skip Adder

the <u>skip logic</u> consists of a k-input AND gate and one MUX

$T_{SK1} = T_{AND}(k) + T_{MUX}$ delay path through the AND gate

$T_{SK2} = T_{MUX}$ delay path from the ripple carry   … the critical path

T_{SK2} late signal

T_{SK1} early signal

2 input multiplexer

late signal
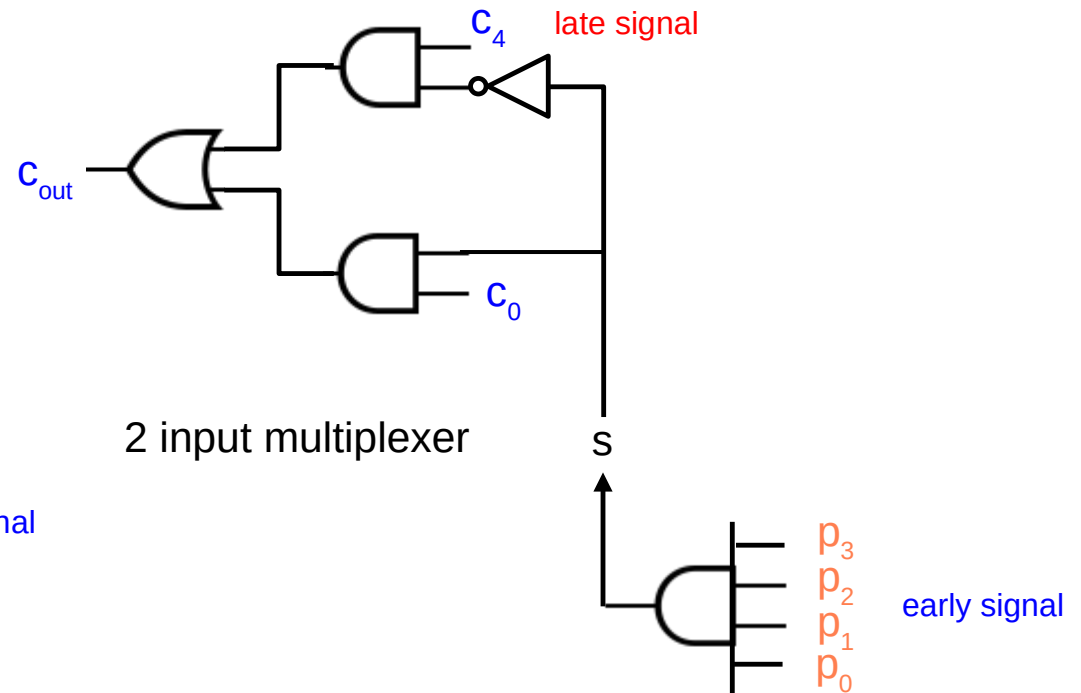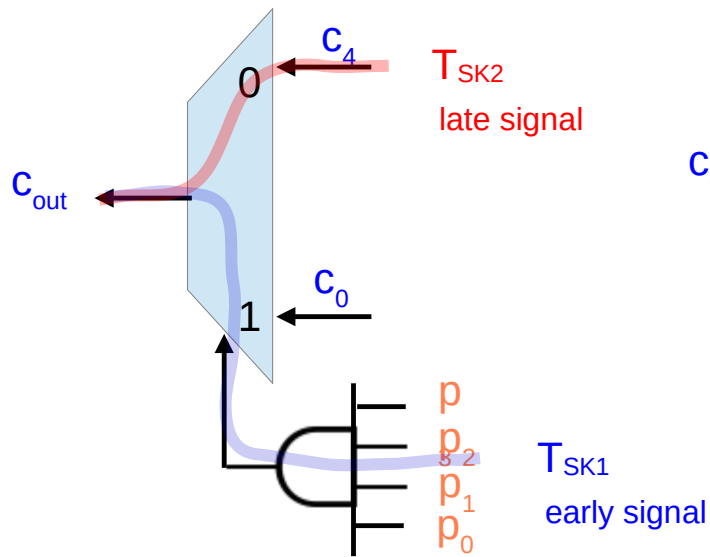
early signal

https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder

As the propagate signals
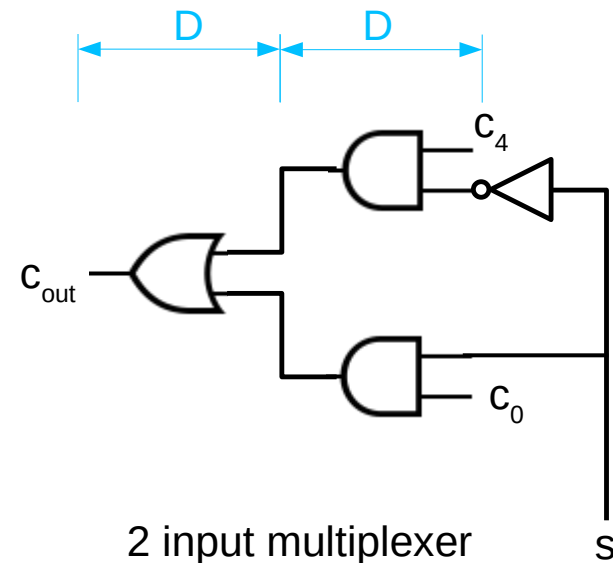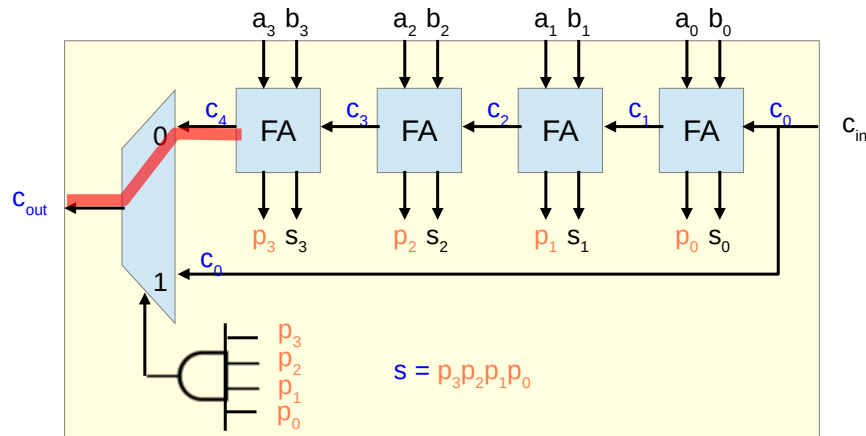 are computed in parallel and
  are early available,

$$p_i = a_i \oplus b_i$$

the critical path for the skip logic in a Carry Skip Adder
consists of the delay imposed by the multiplexer (conditional skip)

T_{CSK} skip logic delay in the critical path

$$T_{CSK} = T_{SK2} = T_{MUX} = 2D$$

2 input multiplexer

https://en.wikipedia.org/wiki/Carry-skip_adder

Block Carry Skip Adder

Block carry skip adders are composed of a number of carry skip adders

There are two types of block carry skip adders

The two operands $A = (a_{n-1}, a_{n-2}, \ldots a_1, a_0)$ and $B = (b_{n-1}, b_{n-2}, \ldots b_1, b_0)$
are split in k blocks of $(m_k, m_{k-1}, \ldots m_2, m_1)$ bits

- Why are block carry skip adders used
- Should the block size be <u>constant</u> or <u>variable</u>?
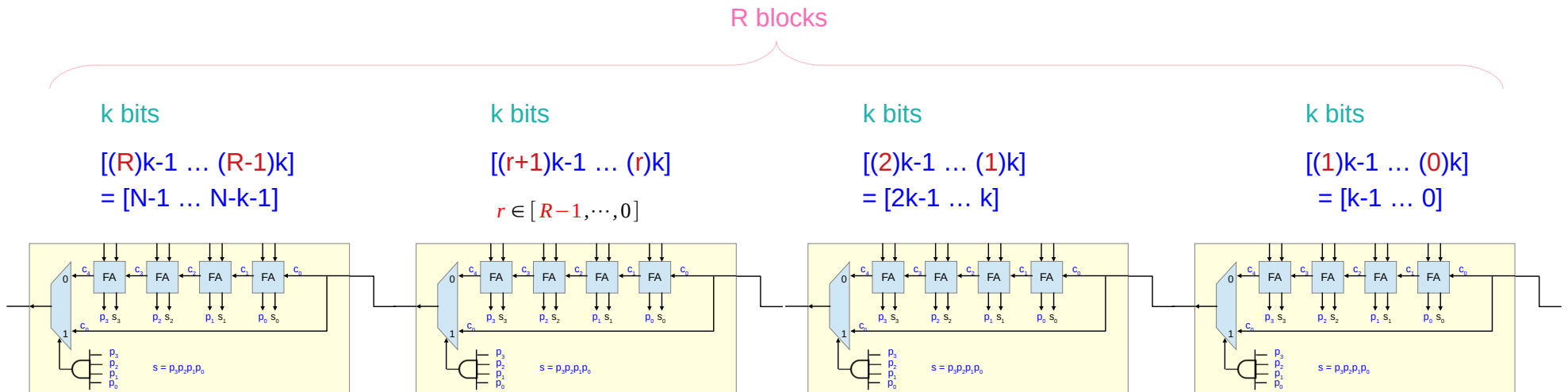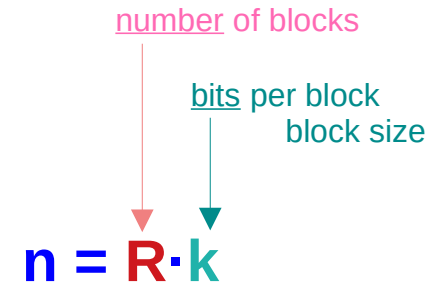- <u>Fixed</u> block size vs. <u>variable</u> block size

Oklobdzija: High-Speed VLSI arithmetic units : adders and multipliers

Fixed-size Block Carry Skip Adder

Carry Skip Adders are <u>chained</u> to reduce the <u>overall</u> critical path,
(Block Carry Skip Adders)

Fixed size block <u>Carry Skip Adders</u> (FCSA) split the *n* bits of the input bits
Into blocks of *k* bits each, resulting in R = *n* / *k* blocks.

Fixed-size block CSA (FCSA)

<u>number</u> of blocks

<u>bits</u> per block
block size

$$n = R \cdot k$$

R blocks

k bits	k bits	k bits	k bits
$[(R)k\text{-}1 \ldots (R\text{-}1)k]$	$[(r+1)k\text{-}1 \ldots (r)k]$	$[(2)k\text{-}1 \ldots (1)k]$	$[(1)k\text{-}1 \ldots (0)k]$
$= [N\text{-}1 \ldots N\text{-}k\text{-}1]$	$r \in [R-1, \cdots, 0]$	$= [2k\text{-}1 \ldots k]$	$= [k\text{-}1 \ldots 0]$

Carry Skip Adder

the critical path

the longest carry path must be
- <u>generate</u> in the <u>first</u> block
- <u>terminated</u> in the <u>last</u> block
- <u>propagated</u> in the blocks between the first and the last

X	Y		
0	0	K	Kill (=$\overline{P}\overline{G}$)
0	1	P	Propagate
1	0	P	Propagate
1	1	G	Generate

R groups

k bits

Fixed-size block CSA (FCSA)

$$n = R \cdot k$$

the last block

(R-2) blocks

the first block

carry terminated in the last FA

carry generated in the first FA
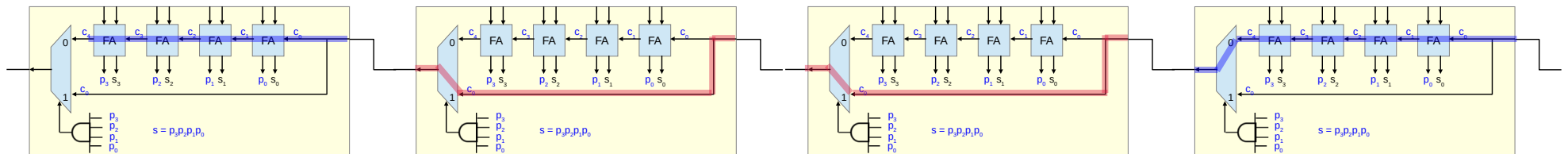
https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder

The critical path consists of

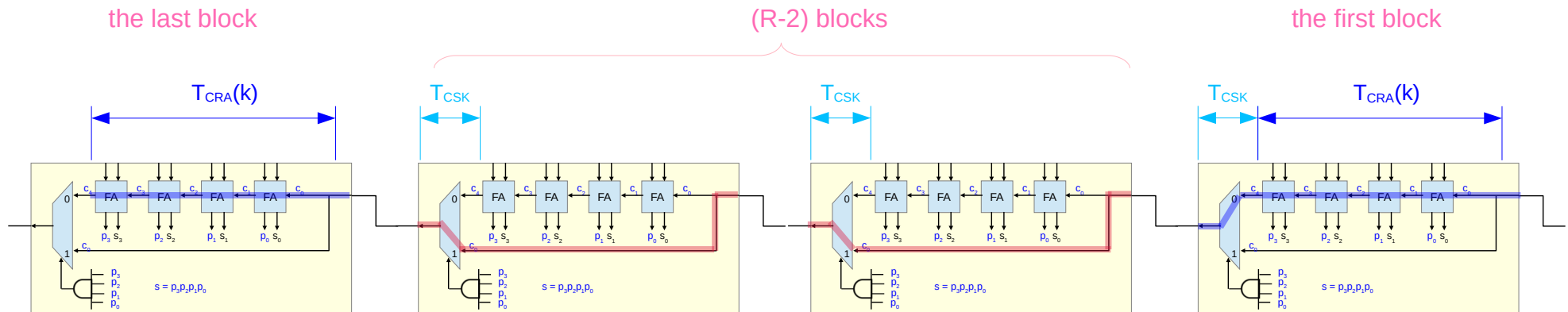- the <u>ripple path</u> and the <u>skip element</u> of the first block
  $T_{CRA}(k) + T_{CSK}$ $T_{CRA[0:cout]}(k)$

- the <u>skip paths</u> that are enclosed between the <u>first</u> and the <u>last</u> block
  $(R-2)T_{CSK}$

- finally the <u>ripple path</u> of the last block
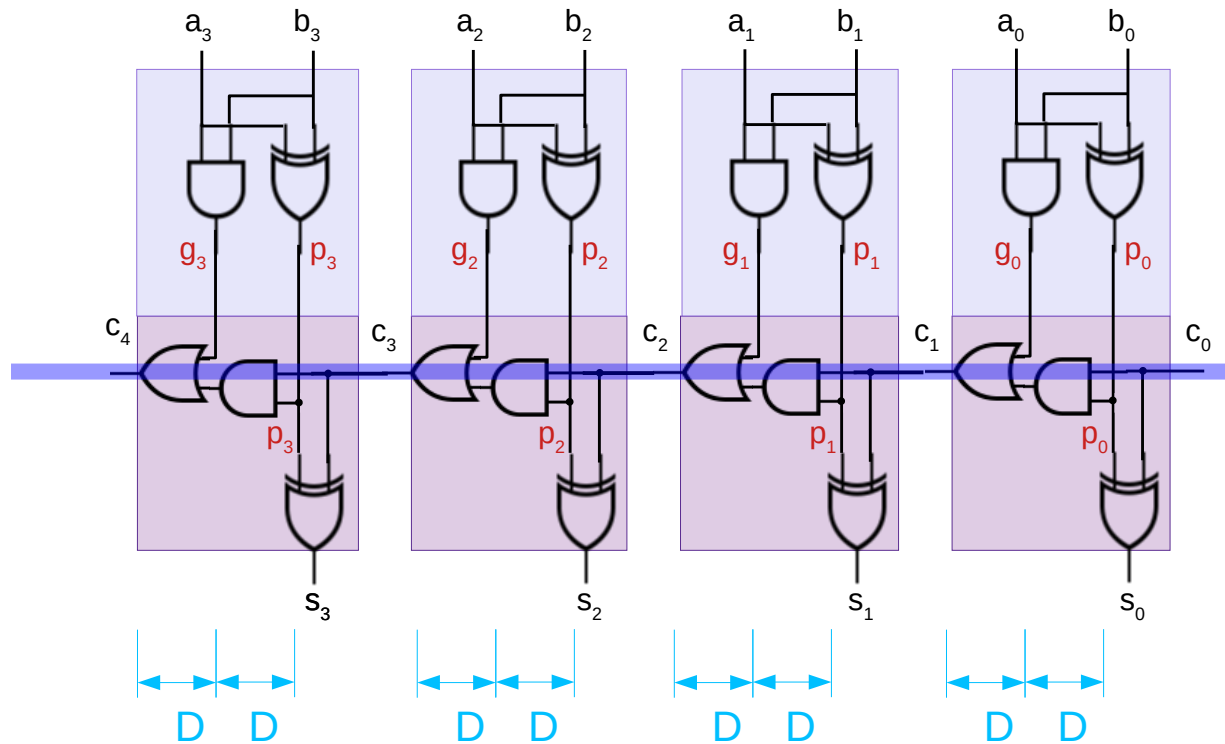 $T_{CRA}(k)$

Fixed-size block CSA (FCSA)

R groups

k bits

$$n = R \cdot k$$

the last block   (R-2) blocks   the first block

https://en.wikipedia.org/wiki/Carry-skip_adder

4-bit Full Adder with P and G

k bits

$T_{CRA}(k) = 2D \cdot k$

Critical Path Delay

The critical path consists of

- the <u>ripple path</u> and the <u>skip element</u> of the first block $T_{CRA}(k) + T_{CSK}$
- the <u>skip paths</u> that are enclosed between the <u>first</u> and the <u>last</u> block $(R-2)T_{CSK}$
- finally the <u>ripple path</u> of the last block $T_{CRA}(k)$

$$
\begin{aligned}
T_{FCSA}(n) \quad &= T_{CRA}(k) + T_{CSK} + (R-2)T_{CSK} + T_{CRA}(k) \\
&= k\,2D + 2D + (R-2)2D + k2D \\
&= k2D + 2D + (R-1)2D - 2D + k2D \\
&= k2D + (R-1)2D + k2D \\
&= 2k2D + (R-1)2D \\
&= (2k+R)2D \\
&= (2k+n/k)2D
\end{aligned}
$$

$$
\begin{aligned}
&= k\,2D + 3D + (R-1)2D + (k+2)2D \\
&= 3D + k2D + R2D - 2D + k2D + 4D \\
&= (2k+R)2D + 5D
\end{aligned}
$$

R groups

k bits

$$n = R \cdot k$$

Optimal block size k

$T_{FCSA}(n)$ $= T_{CRA}(k) + T_{CSK} + (R-2)T_{CSK} + T_{CRA}(k)$
              $= (2k+R)2D$
              $= (2k+n/k)2D$

$$\left(2k + \frac{n}{k}\right)2D$$

The optimal block size k for a given adder width n

$dT_{FCSA}(n) / dk = 0$

$$\frac{dT_{FCSA}(n)}{dk} = 0$$

$(2-n(1/k^2)) = 0$
$2 = n/k^2$
$k^2 = n / 2$

$$k^2 = \frac{n}{2}$$

$k = \text{sqrt}(n/2)$

$$k_{opt} = \sqrt{\frac{n}{2}}$$

$5.6 = \text{sqrt}(64/2)$ $n = 64\text{bits} \to k = 6$
$4 = \text{sqrt}(32/2)$ $n = 32\text{bits} \to k = 4$

Fixed-size block CSA (FCSA)

R groups

k bits

n = R·k

Examples of Optimal Block Sizes

$$T_{FCSA,opt}(n) = \left(2k + \frac{n}{k}\right)2D$$

$$T_{FCSA,opt}(n) = \left(2k + \frac{n}{k}\right)2D$$
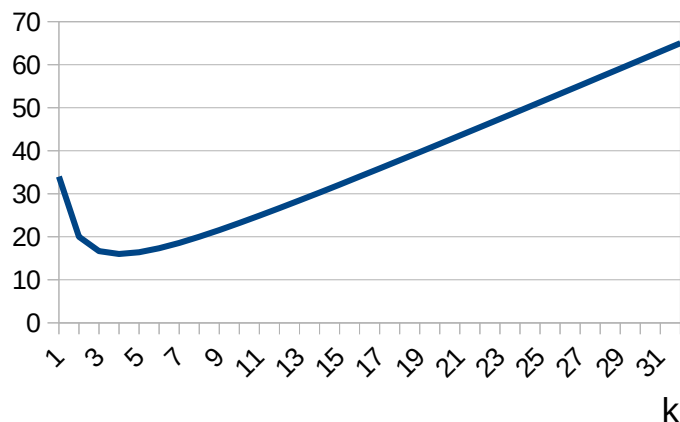
Fixed-size block CSA (FCSA)

$T_{FCSA}(32) = (2k+32/k)2D$

$T_{FCSA}(64) = (2k+64/k)2D$

R groups

k bits

n = R·k

(2k+32/k)

(2k+64/k)

k

k

$4 = sqrt(32/2)$ $k_{opt} = \sqrt{\frac{n}{2}}$
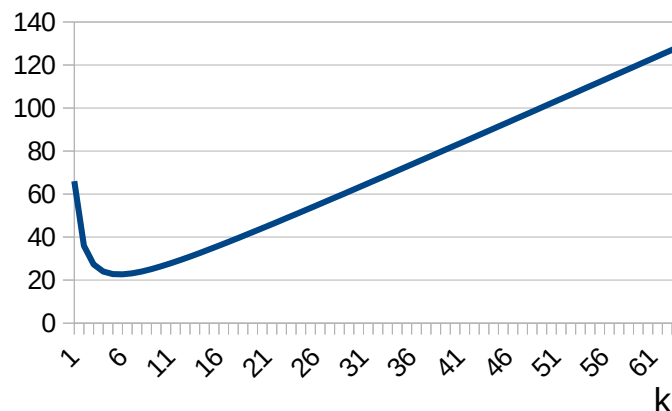
$5.6 = sqrt(64/2)$ $k_{opt} = \sqrt{\frac{n}{2}}$

n = 32bits
→ k = 4

n = 64bits
→ k = 6

https://en.wikipedia.org/wiki/Carry-skip_adder

Asymptotic Analysis

$T_{FCSA}(n) = (2k+n/k)2D$

The optimal block size k for a given adder width n
k = sqrt(n/2)

$T_{FCSA, opt}(n)$ = (2sqrt(n/2) +n/sqrt(n/2))2D
= (sqrt(2n) + sqrt(n^2 /n / 2)) 2D
= (sqrt(2n) + sqrt(2n))2D
= (2sqrt(2n))2D

$$T_{FCSA,opt}(n) = \left(2\sqrt{n/2}+\frac{n}{\sqrt{n/2}}\right)2D$$

$$= (2\sqrt{2n})2D \qquad when \quad k_{opt} = \sqrt{\frac{n}{2}}$$

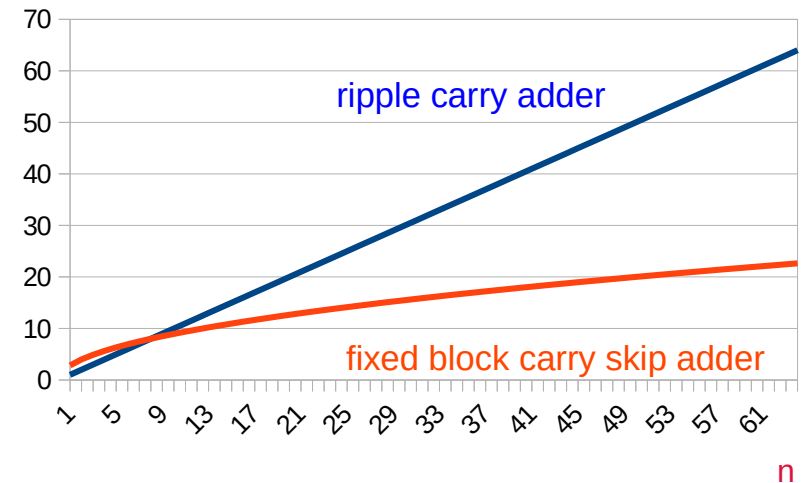https://en.wikipedia.org/wiki/Carry-skip_adder

Fixed-size block CSA (FCSA)

R groups

k bits

n = R·k

$T_{CRA}(n) = 2D·n$

$T_{FCSA,opt}(n) = 2D·(2sqrt(2n))$

ripple carry adder

fixed block carry skip adder

n

Critical Carry Path (1)

$T_s < 3T_p$

For longest carry path, if any block <u>generates</u> a carry,
that carry will <u>propagate</u> through the remaining 3 FA's of that block
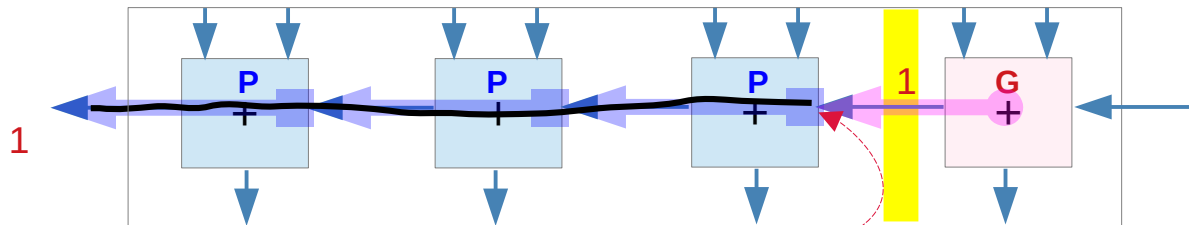
Least Significant Block

$C_{in} = 1$ or 0

carry delay path starts from this FA

and then through the carry skip gates to the <u>final</u> block,
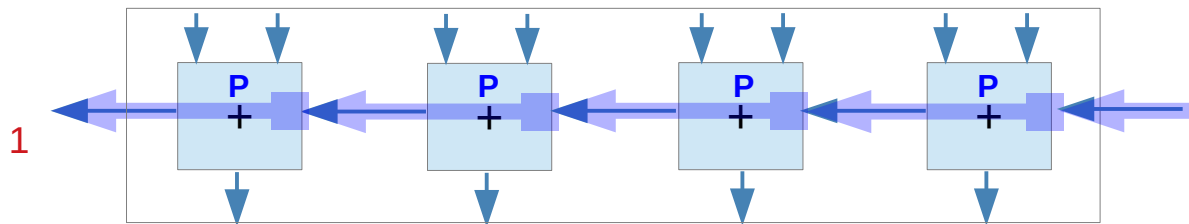
Middle Blocks

1

since all FA's are in the propagate mode, skip path is taken → no ripple delay

Critical Carry Path (2)

At the <u>final</u> block, it may have to <u>propagate</u> through 3 FA's to reach the most significant adder

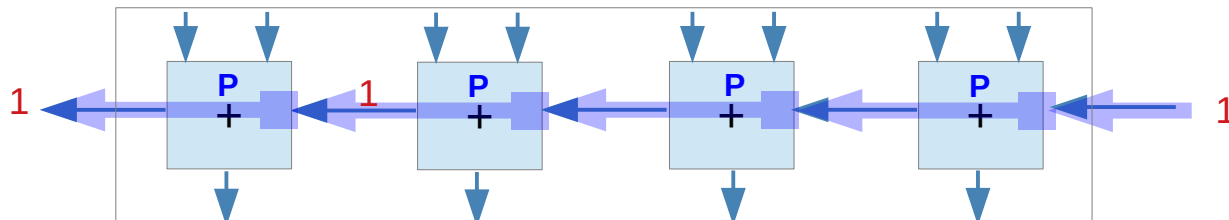**Cases for the Most Significant Block**

carry delay path stops at this FA
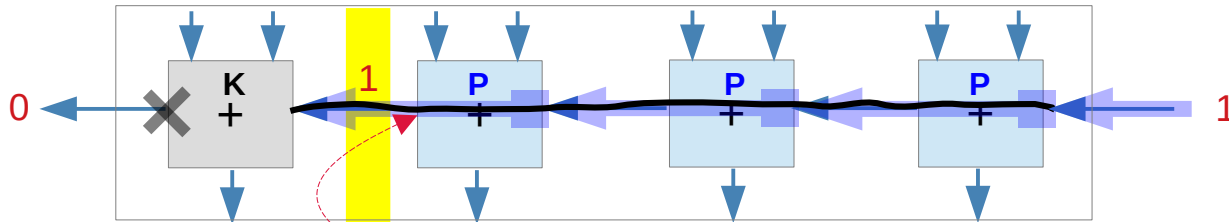
the propagated carry must be terminated at the most significant adder
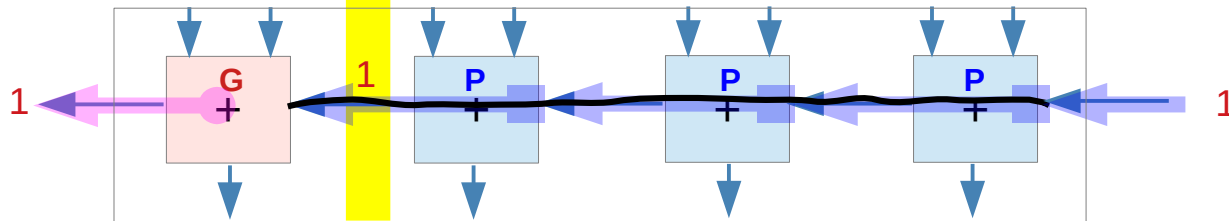
the new carry can be generated at the most significant adder

a new path starts here

Otherwise, the whole block is to be skipped
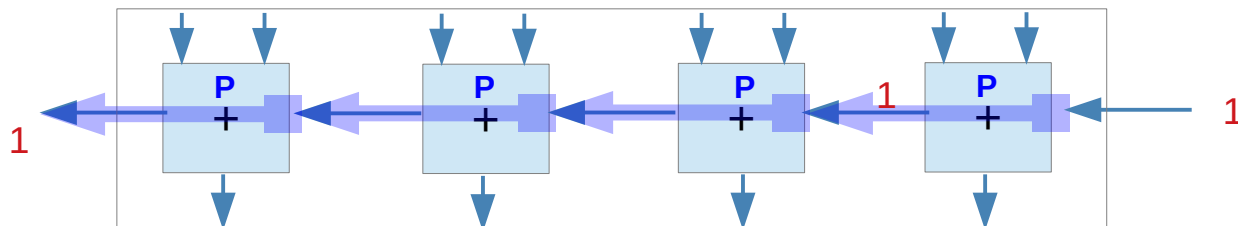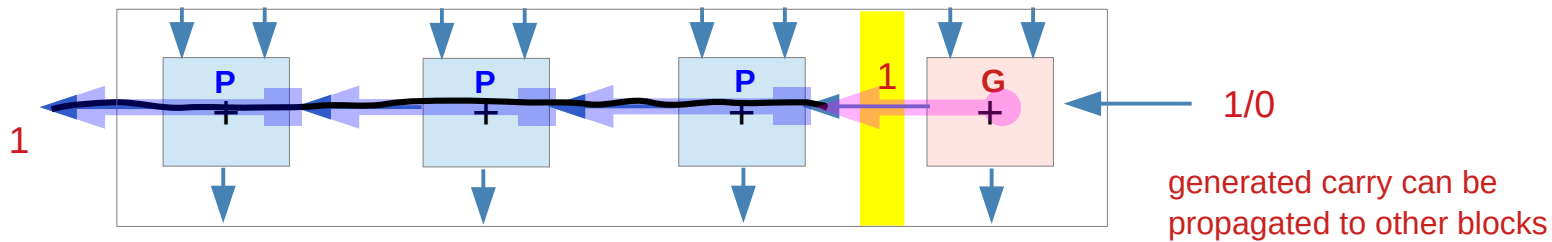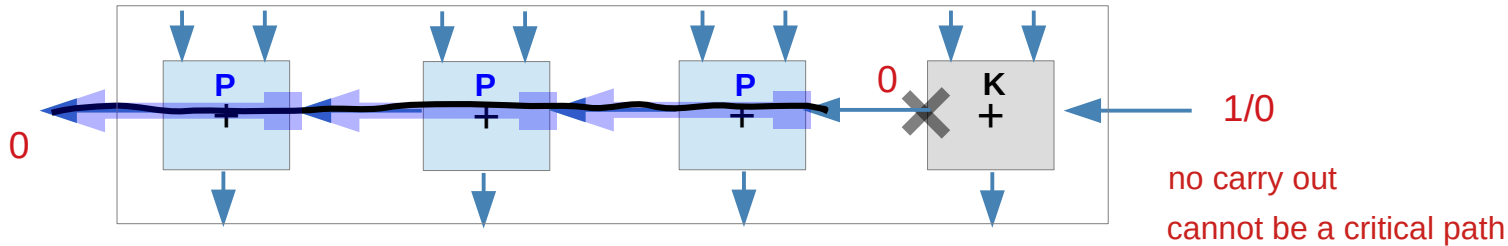
smaller delay than ripple delay

$T_s < 3T_p$

cannot be a critical path   since all FA's are propagate mode, <u>skip path</u> is taken

Critical Carry Path (3)

$T_s < 3T_p$

Cases for the Least Significant Block

0 | P+ | P+ | P+ | 0 ✗ K+ | 1/0

no carry out
cannot be a critical path

1 | P+ | P+ | P+ | 1 G+ | 1/0
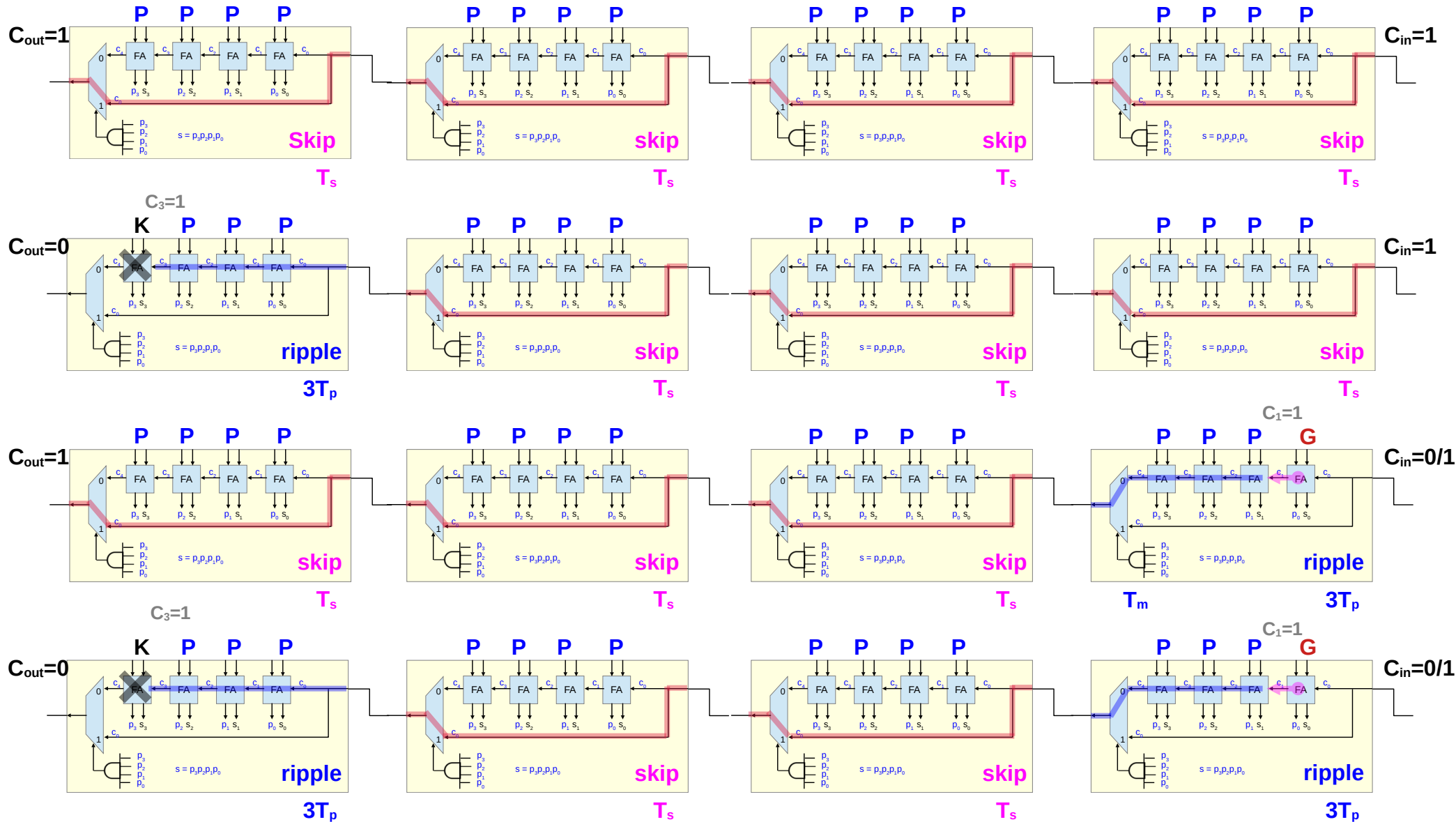
generated carry can be
propagated to other blocks

1 | P+ | P+ | P+ | 1 P+ | 1

$T_s < 3T_p$

cannot be a critical path   since all FA's are propagate mode, skip path is taken → no ripple delay
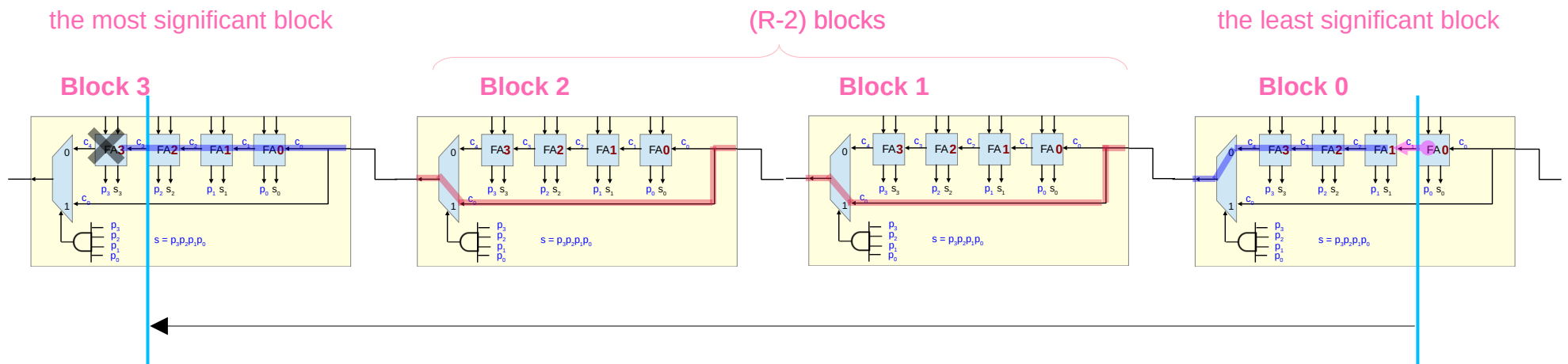
Critical Carry Path (4)

Carry Skip Adder

The longest delay path from c_1 to c_{n-1}

begins with a carry generated in FA0 in the least significant block 0,
propagates through FA3 in block 0,
then through the skip element (MUX can be replaced with OR gate),
then through carry skip units of (R-2) blocks,
and then through fa0, fa1, fa2 in the most significant block (R-1),
to the c_{n-1} signal

Fixed-size block CSA (FCSA)

R groups

k bits

$$n = R \cdot k$$

the most significant block

(R-2) blocks

the least significant block

Block 3

Block 2

Block 1

Block 0

More Fast Adders, Ivor Page, University of Texas at Dallas

Carry Skip Adder

The longest delay path from c_1 to c_{n-1}

$(k-1)T_p + D + (n/k-2)T_s + (k-1) T_p$

T_p is the time to propagate a carry
through one stage of the full adder
(from c_i to c_{i+1})

T_s is the delay through one carry-skip stage

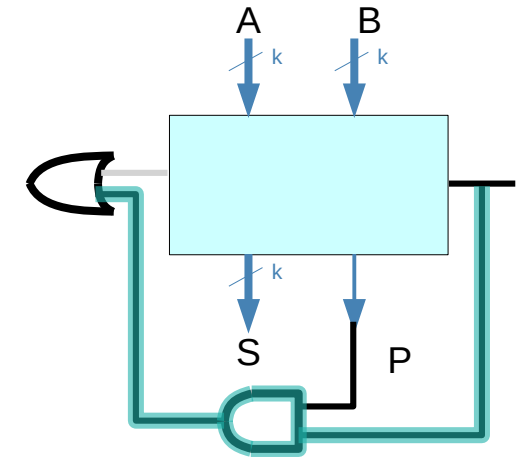**Fixed-size block CSA
(FCSA)**

R groups

k bits

$n = R \cdot k$

More Fast Adders, Ivor Page, University of Texas at Dallas

Carry Skip Adder

A carry signal centering a certain block
can be propagated past the block
<u>without</u> <u>waiting</u> for the signal to propagate
through the 4 individual stages of the block

If all n/4 blocks propagate, a carry entering the least significant stage
will pass to the most significant carry-out
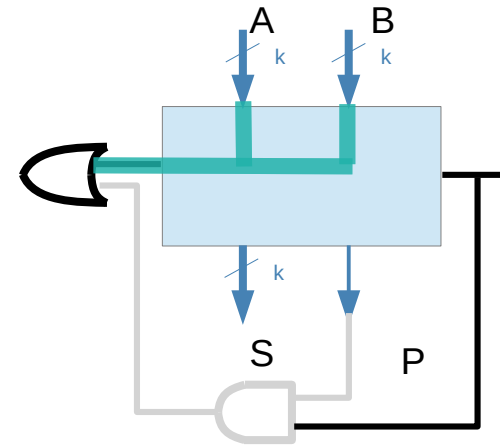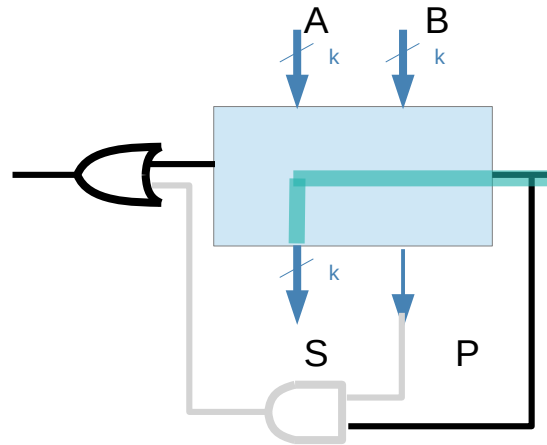in time n/4 times the delay through the carry-skip unit
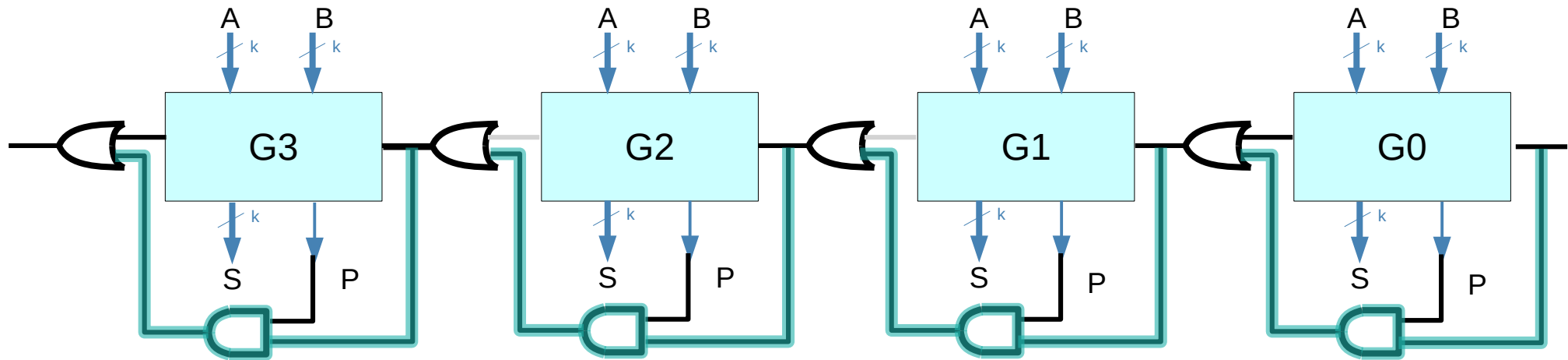
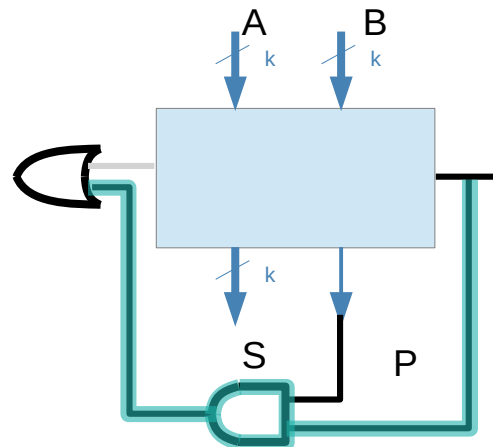More Fast Adders, Ivor Page, University of Texas at Dallas

Carry Skip Adder

Ripple through k-1 bits

$(k - 1) \Delta_{rca}$

Skip carry

Δ_{SKIP}

Oklobdzija: High-Speed VLSI arithmetic units : adders and multipliers

Carry Skip Adder

The <u>maximal delay</u> Δ of a Carry Skip Adder is encountered
<u>when</u> carry is generated in the least-significant bit position,

- rippling through *k-1* bit positions,
- skipping over *R-2 = N/k-2* groups in the middle,
- rippling to the *k-1* bits of most significant group and
- being assimilated in the *N-th* bit position to produce the sum S_N :

$$\Delta_{CSA} = (k - 1)\, \Delta_{rca} + (R - 2)\, \Delta_{SKIP} + (k - 1)\, \Delta_{rca}$$
$$= 2\,(k - 1)\, \Delta_{rca} + (R - 2)\, \Delta_{SKIP}$$
$$= 2\,(k - 1)\, \Delta_{rca} + (N/k - 2)\, \Delta_{SKIP}$$

Oklobdzija: High-Speed VLSI arithmetic units : adders and multipliers

Carry Skip Adder

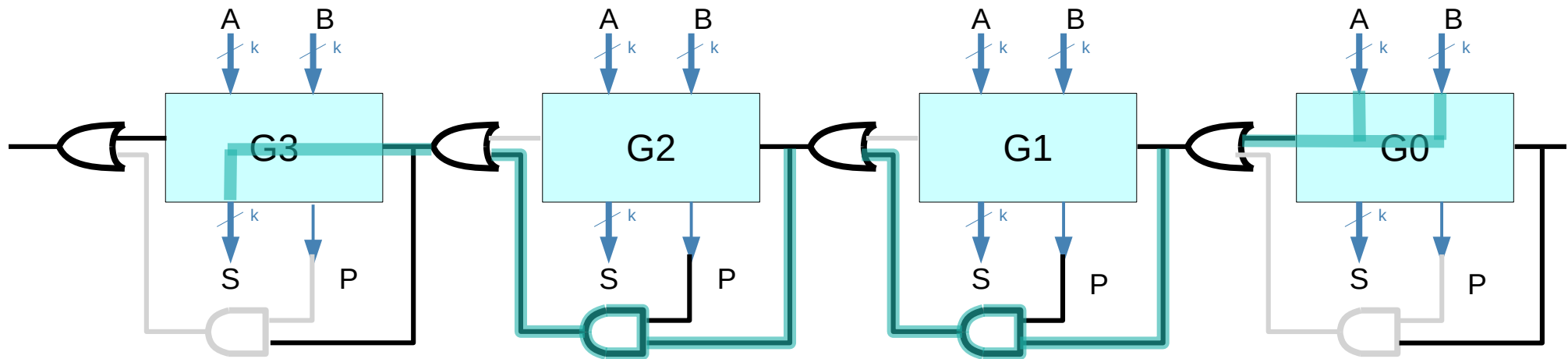$$\Delta_{CSA} = (k-1)\,\Delta_{rca} + (R-2)\,\Delta_{SKIP} + (k-1)\,\Delta_{rca}$$
$$= 2\,(k-1)\,\Delta_{rca} + (R-2)\,\Delta_{SKIP}$$
$$= 2\,(k-1)\,\Delta_{rca} + (N/k-2)\,\Delta_{SKIP}$$

Carry Skip Adder is faster than RCA at the expense
of a few relatively simple modifications.

$N = R \cdot k$
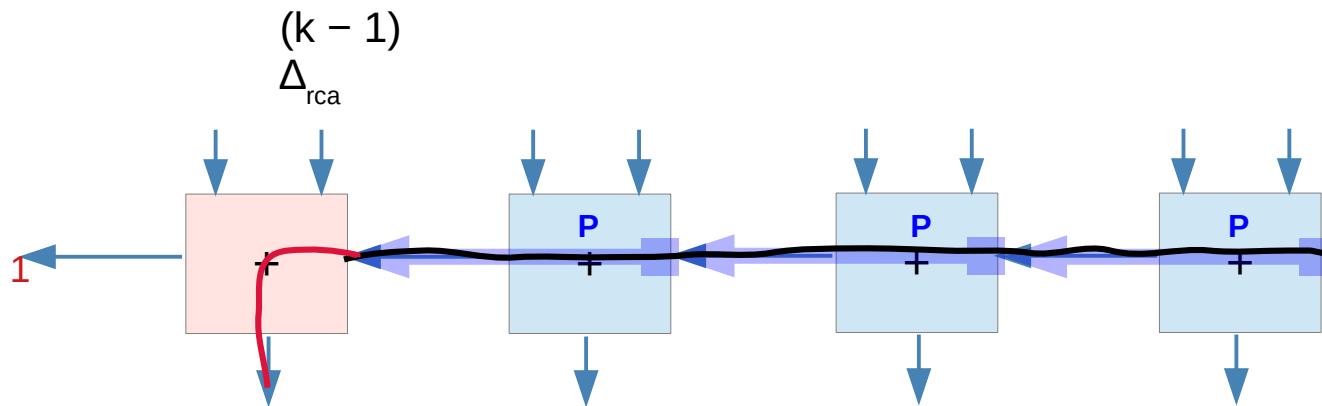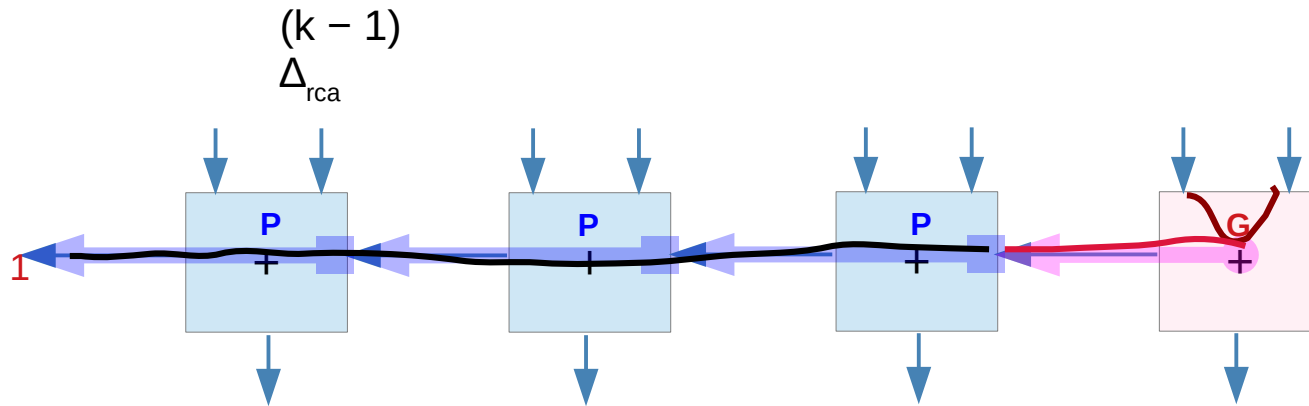
The delay is still linearly dependent on the size of the adder N,
however this linear dependence is reduced by a factor of *1/k*

Oklobdzija: High-Speed VLSI arithmetic units : adders and multipliers

Design C (9) – When Cout1 = 1

$(k - 1)$ Δ_{rca}

$(k - 1)$ Δ_{rca}

High Performance Carry Chains for FPGAs, S. Hauck, M. M. Hosler, T. W. Fry

Carry Skip Adder

If an arbitrary block generated a carry by itself,
The carry will always propagate to the next block
However, if the second block generates a carry itself,
Or kill the carry, then that is the end of the critical path

If the second block propagates the carry, then we see
The advantage of the CSA architecture

https::/electronics.stackexchange.com/questions/21251/critical-path-for-carry-skip-adder

Variable size Block Carry Skip Adder

The performance can be improved, ie.
all carries propagated quickly
by varying the block sizes

Accordingly the initial blocks of the adder are
made smaller so as to quickly detect carry generates
that must be propagated the furthers,
the middle blocks are made larger
because they are not the problem case,
and then the most significant blocks are again
made smaller so that the late arriving carry inputs
can be processed quickly

https::/electronics.stackexchange.com/questions/21251/critical-path-for-carry-skip-adder

References

[1]   en.wikipedia.org
[2]   Parhami, "Computer Arithmetic Algorithms and Hardware Designs"