Latch Based Pipeline (4B)

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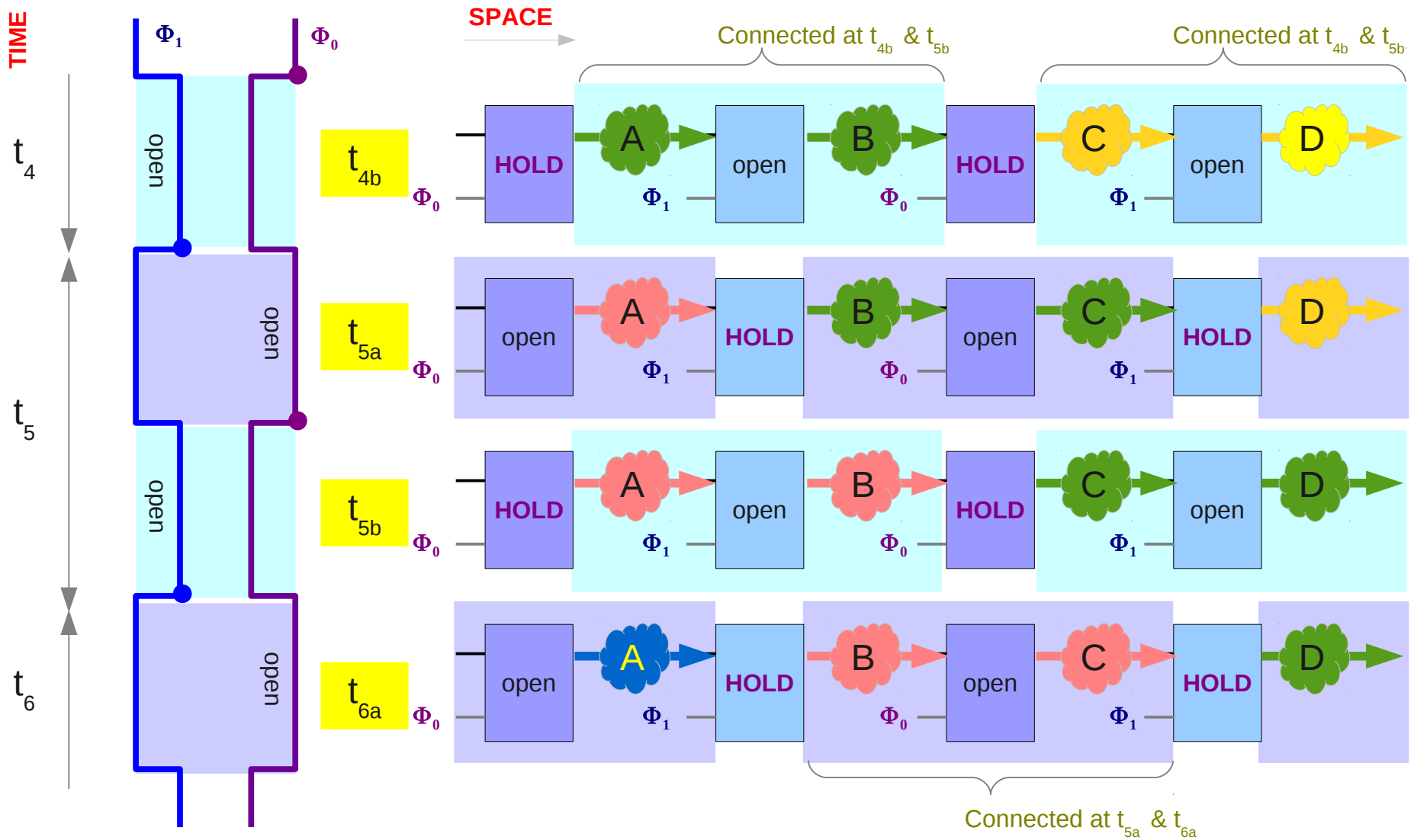
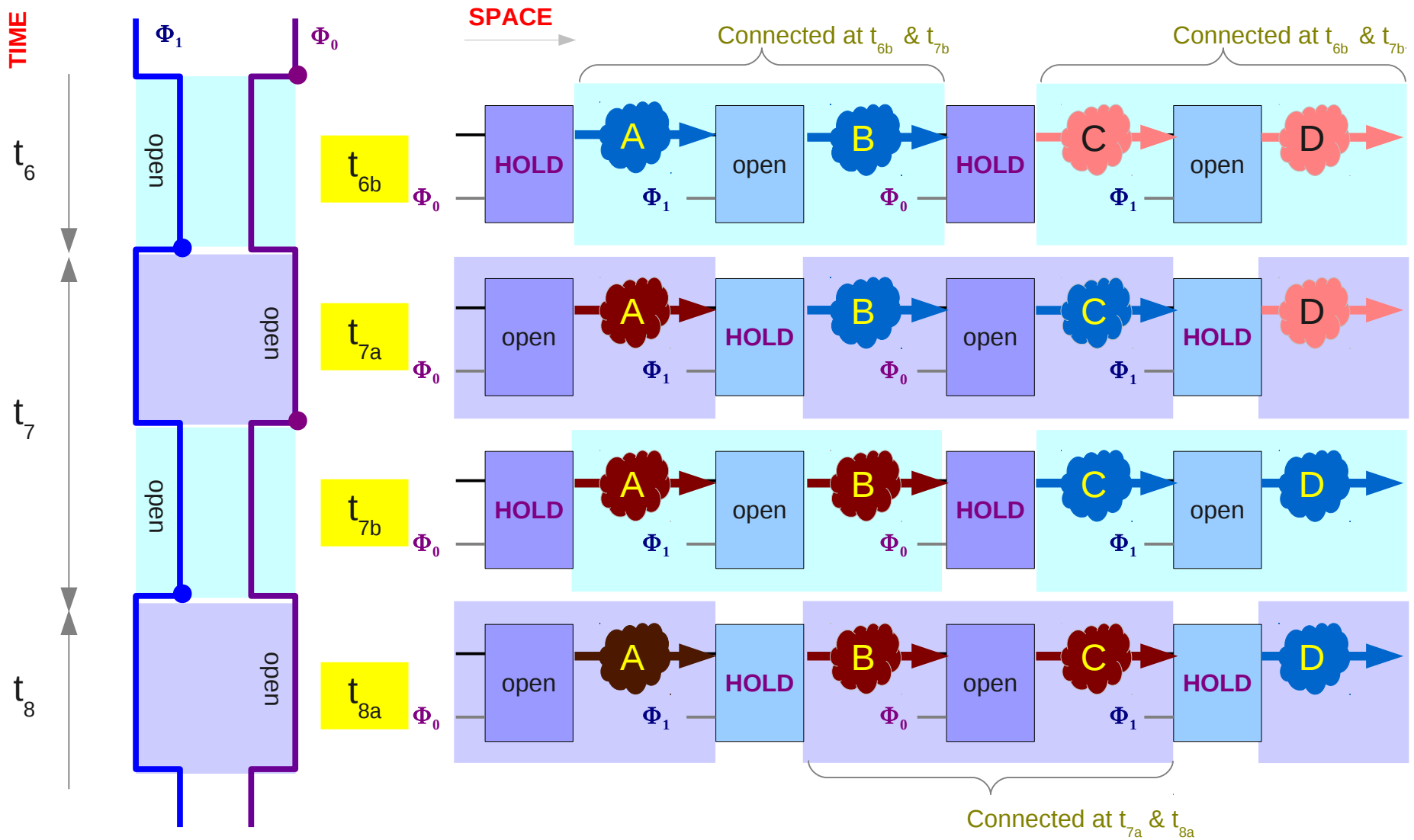
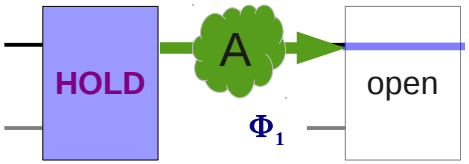
Latch Based Pipeline (1)

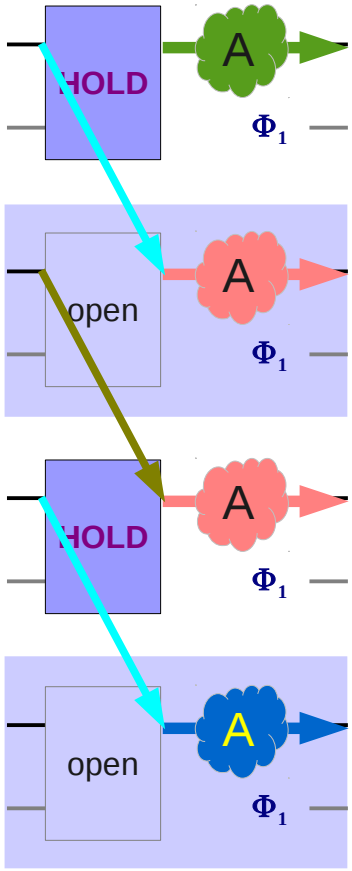


Latch Based Pipeline (2)



- The Open State
- The Transition between States
- The Outputs after Transitions
- The Combinational Circuits





using stable output of the latch while its input may change

using changing output of the latch, transparently transferred inputs

HOLD → open

Changing output

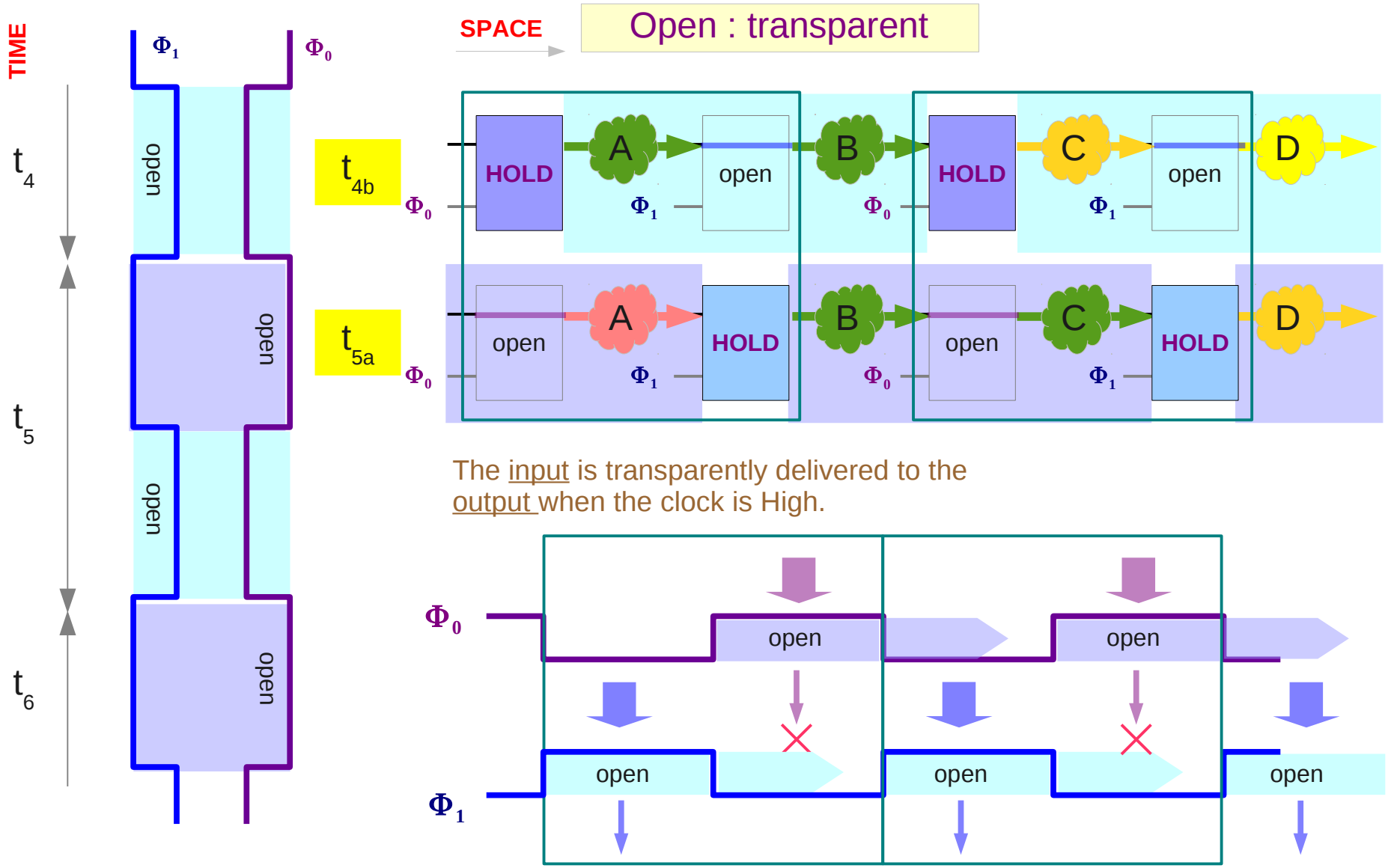
Begin to pass a new data to the output

open → **HOLD**

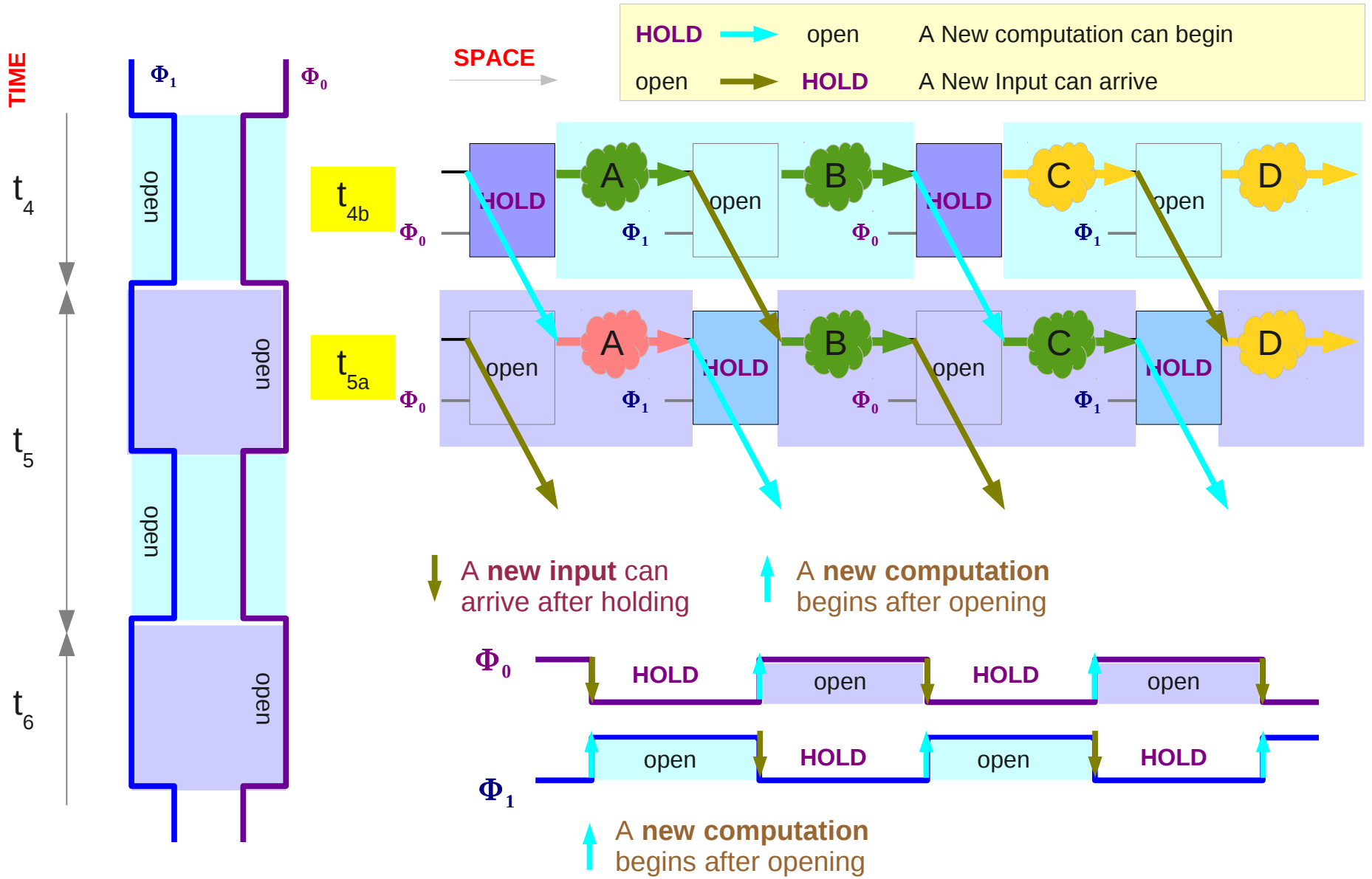
Stable output

Stop to pass the current data to the output

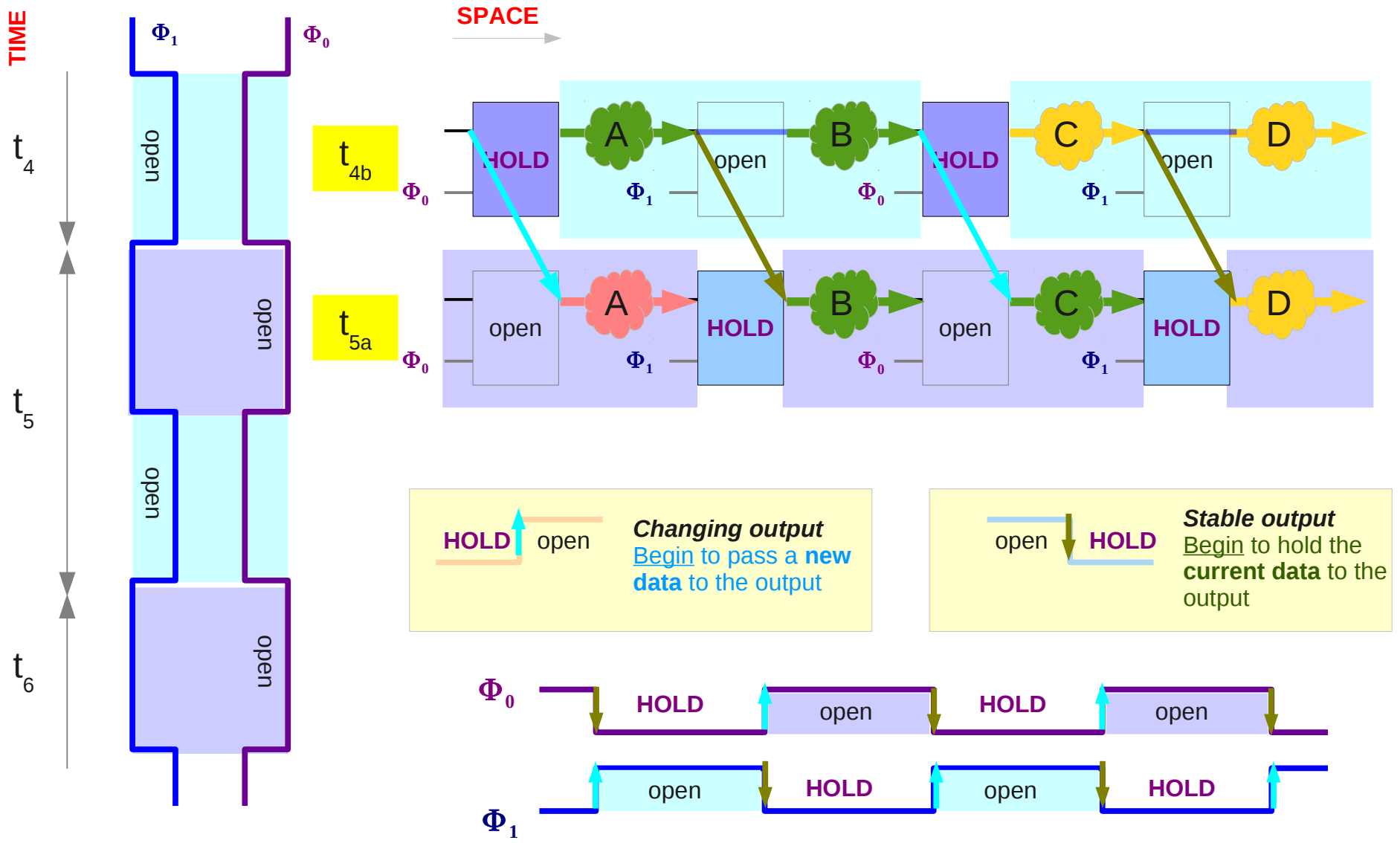
The Open State



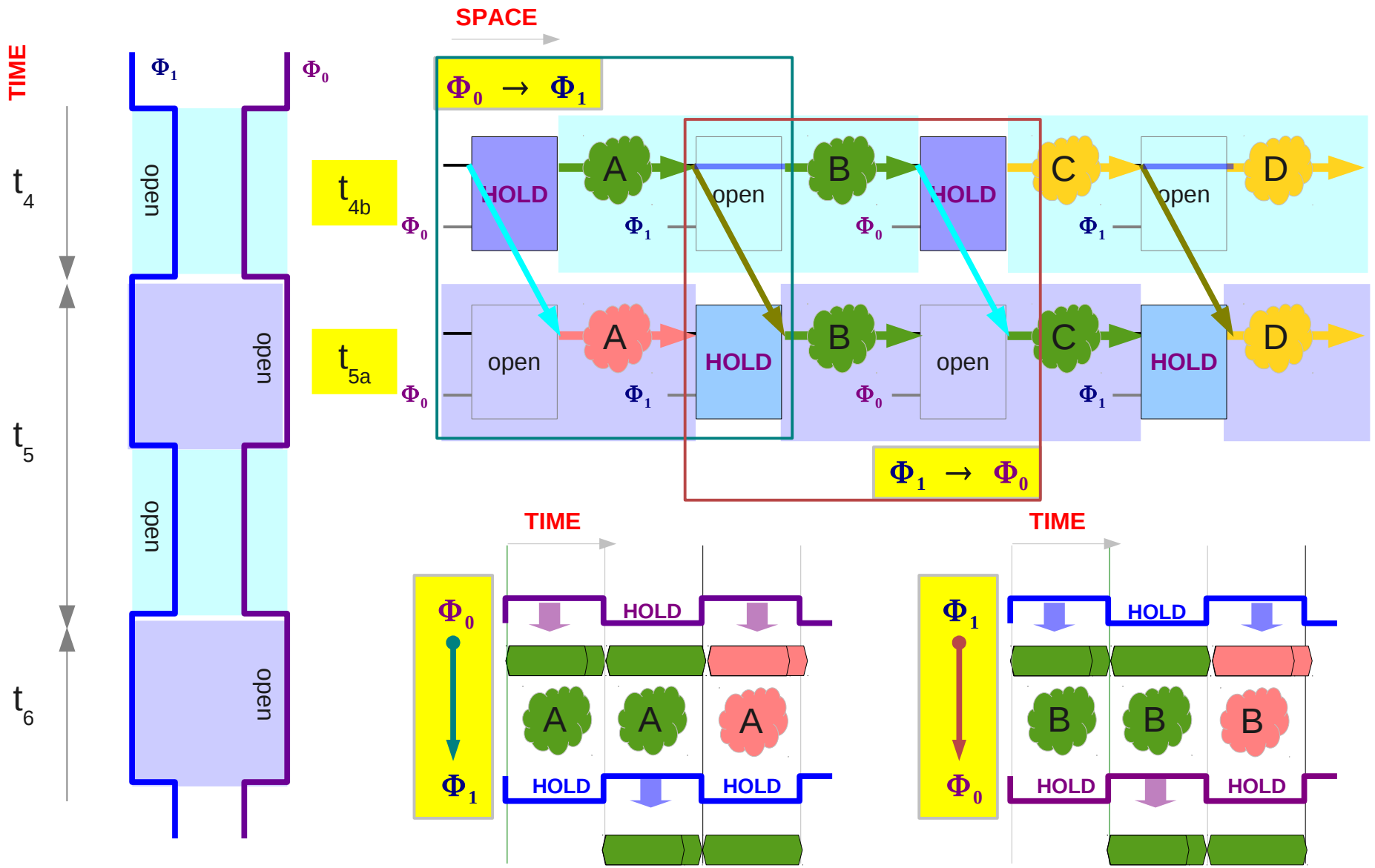
The Transition between States



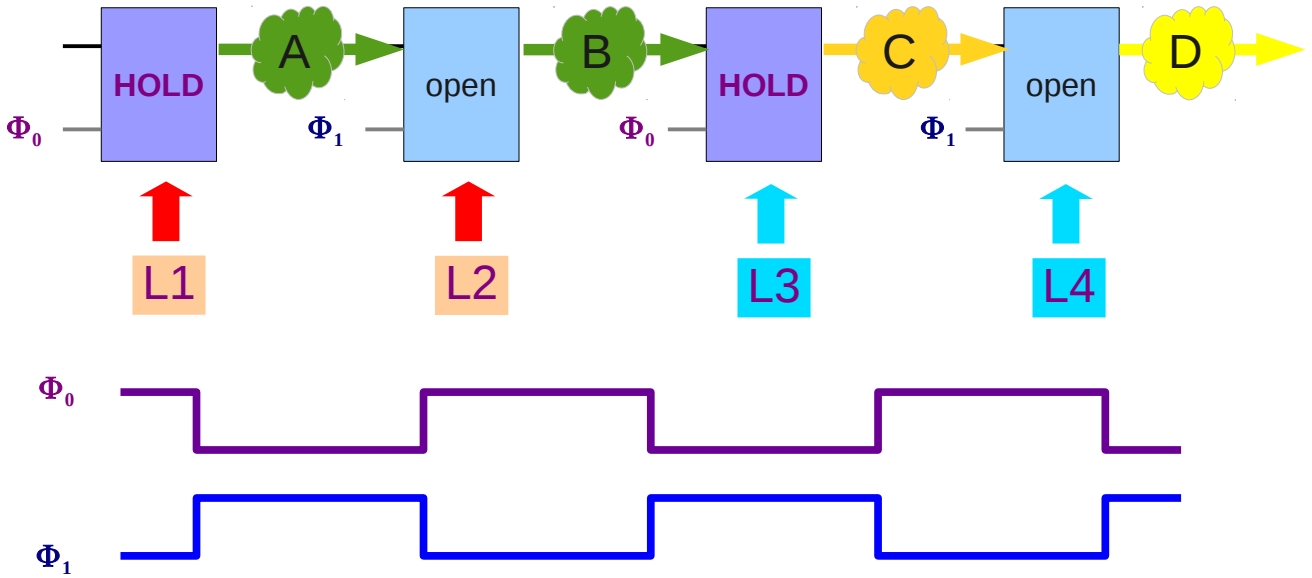
The Outputs after Transitions



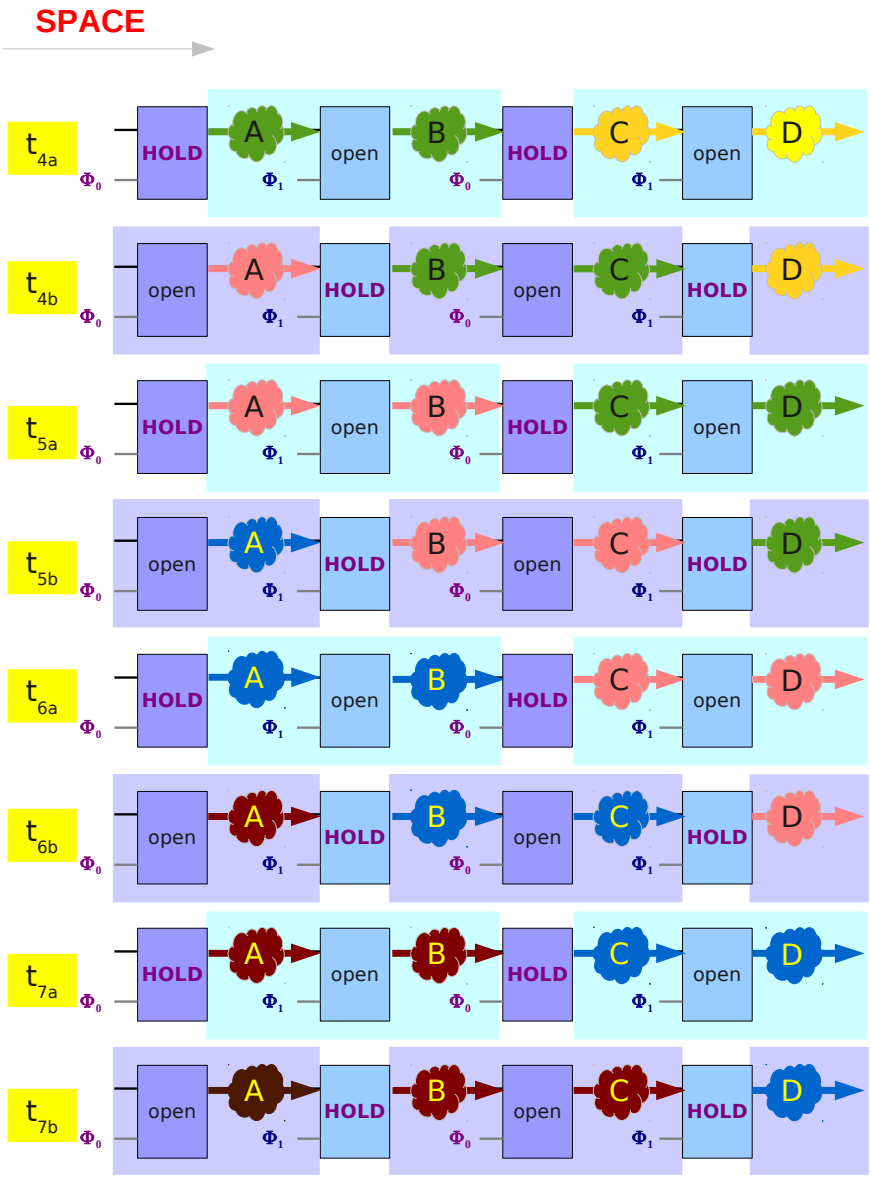
The Combinational Circuits

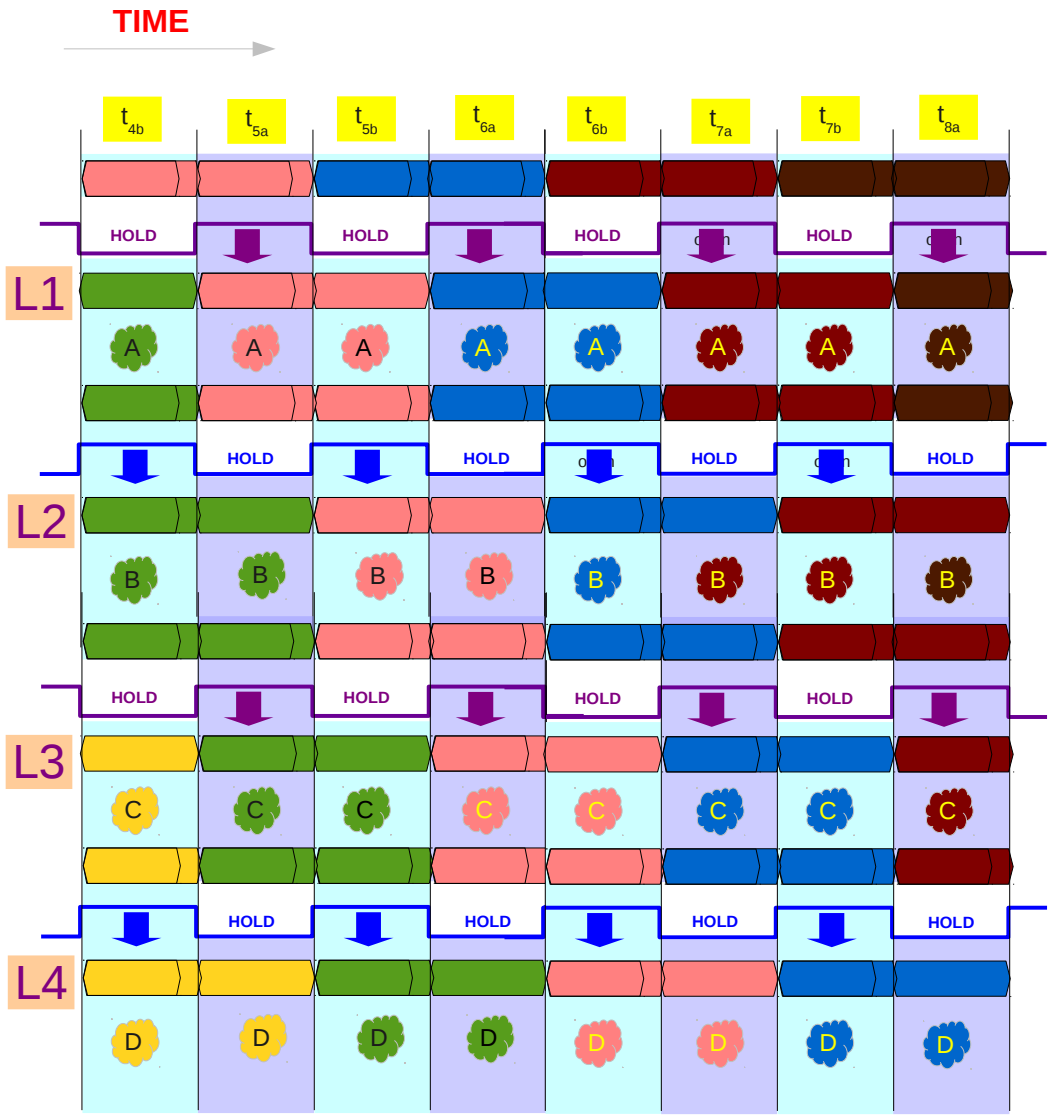


- The Latch Timing
- The Latch L1 & L2 Timing (1, 2)
- The Latch L3 & L4 Timing (1, 2)
- The FlipFlop Based Pipeline Timing
- The Latch Based Pipeline Timing

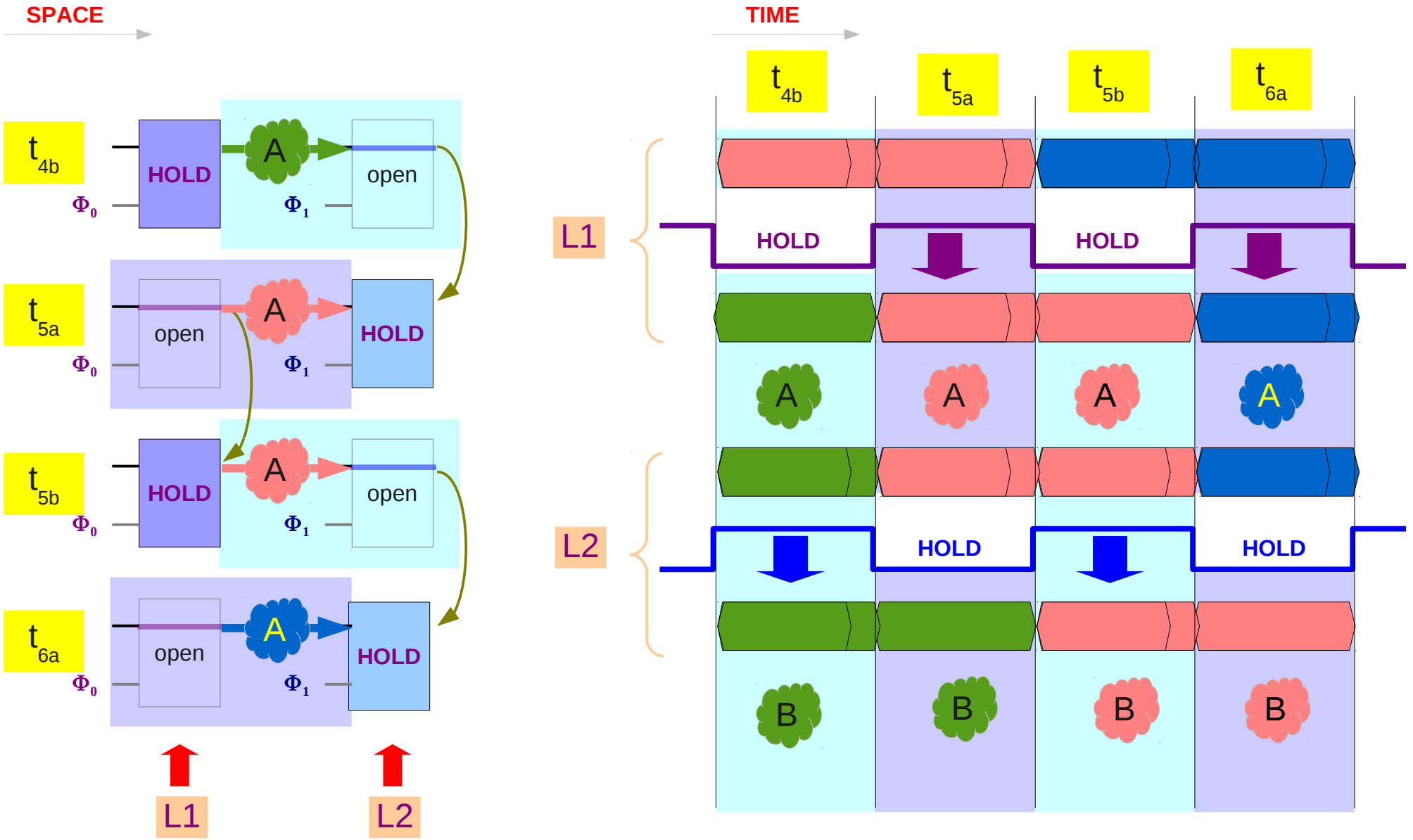


The Latch Timing

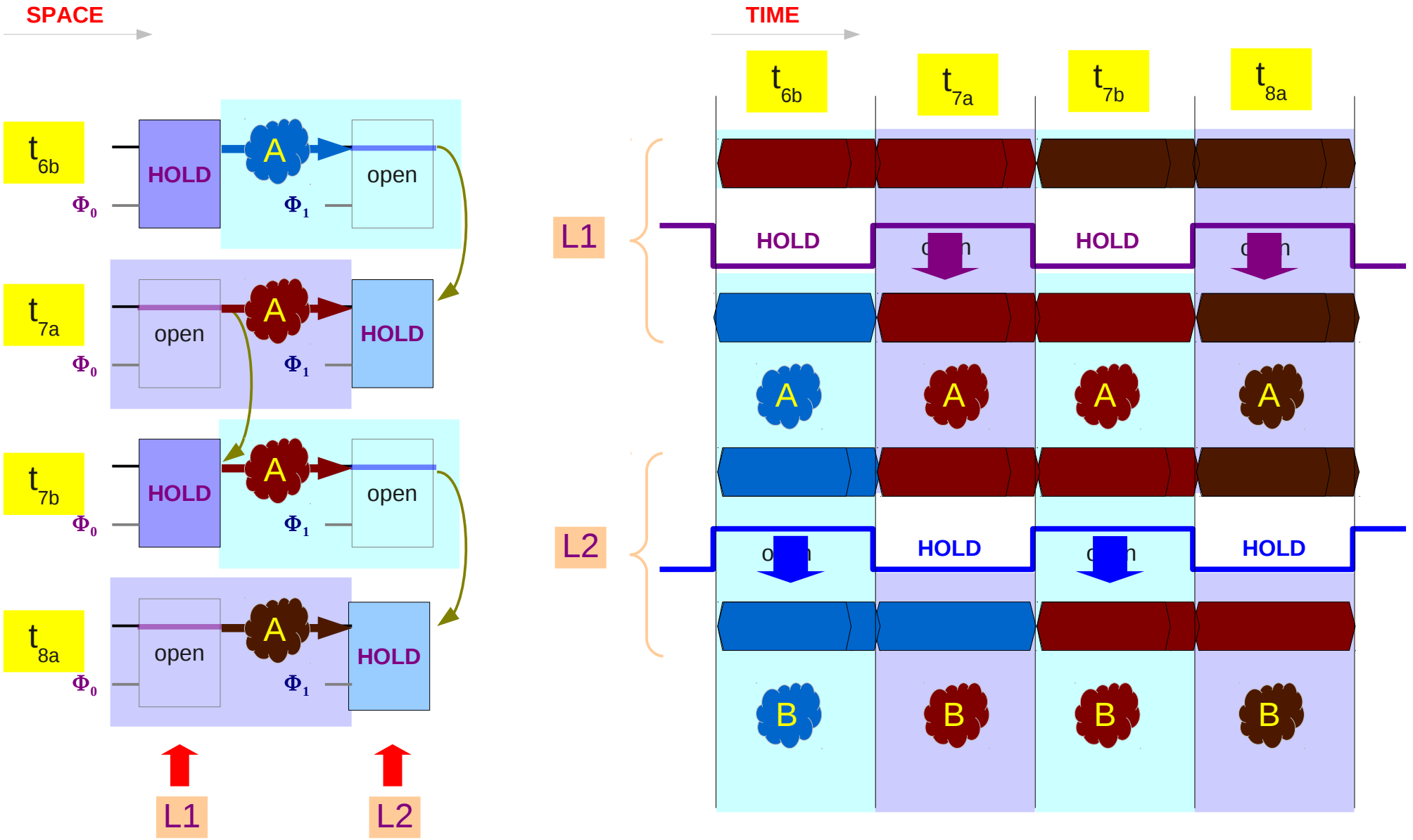




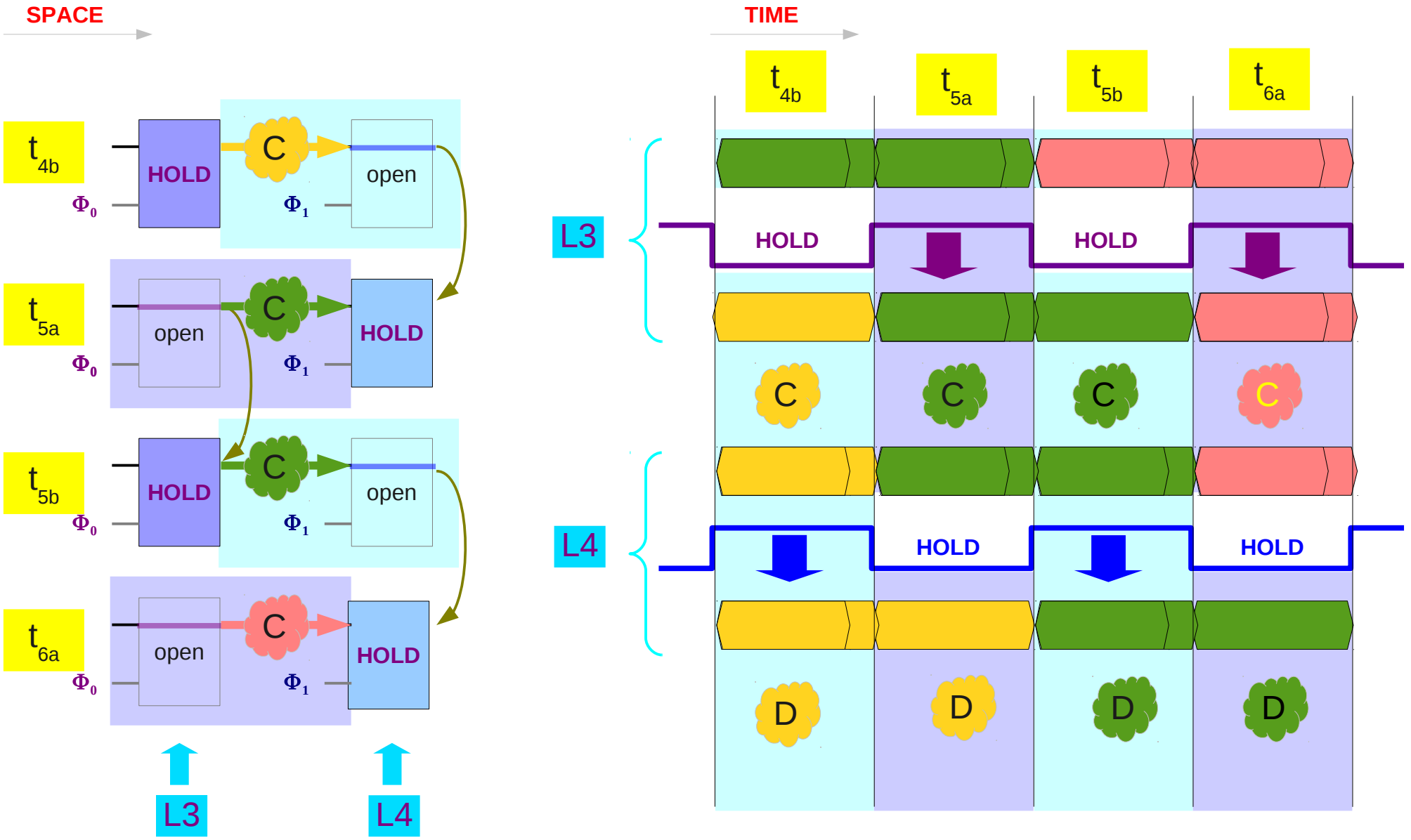
The Latch L1 & L2 Timing (1)



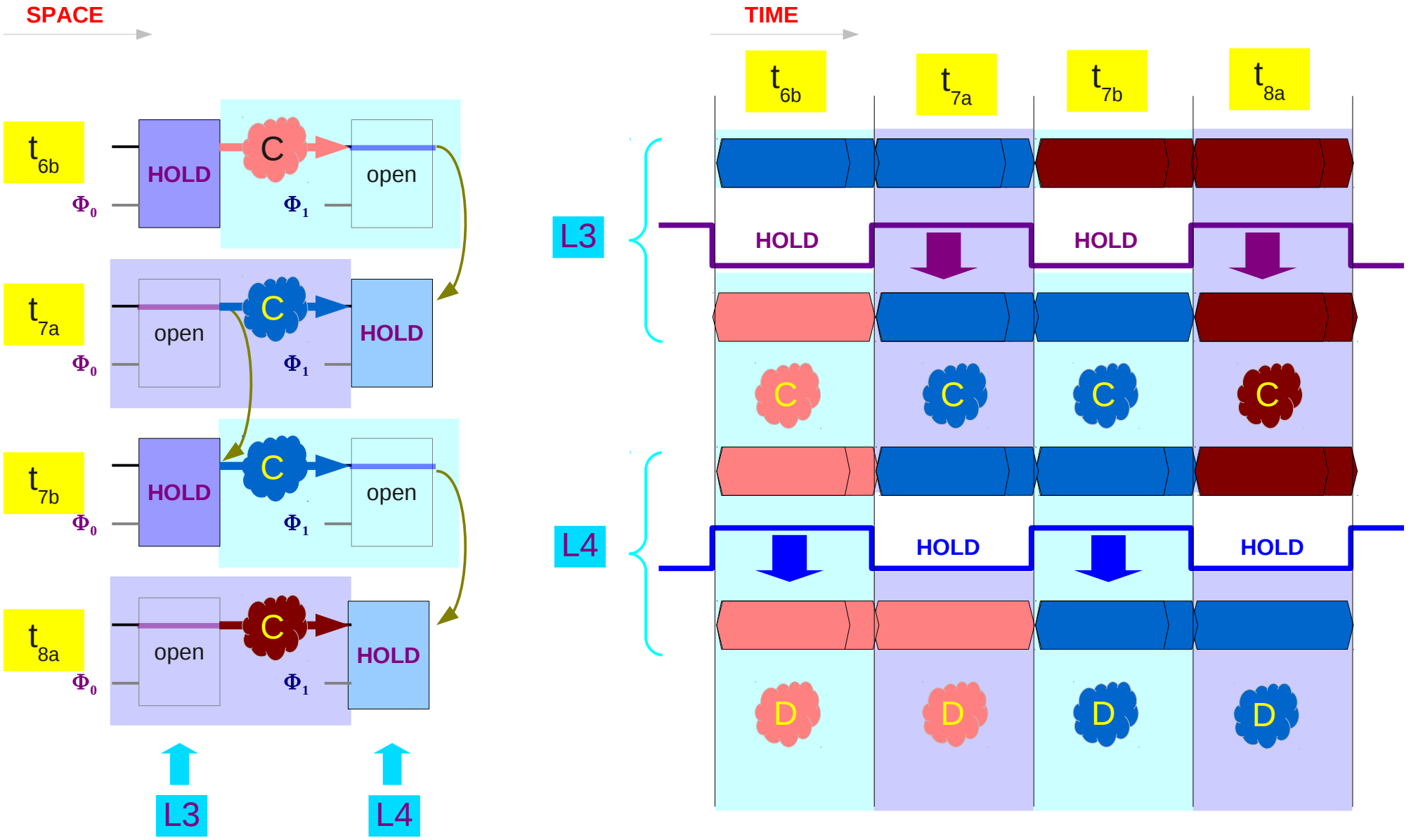
The Latch L1 & L2 Timing (2)



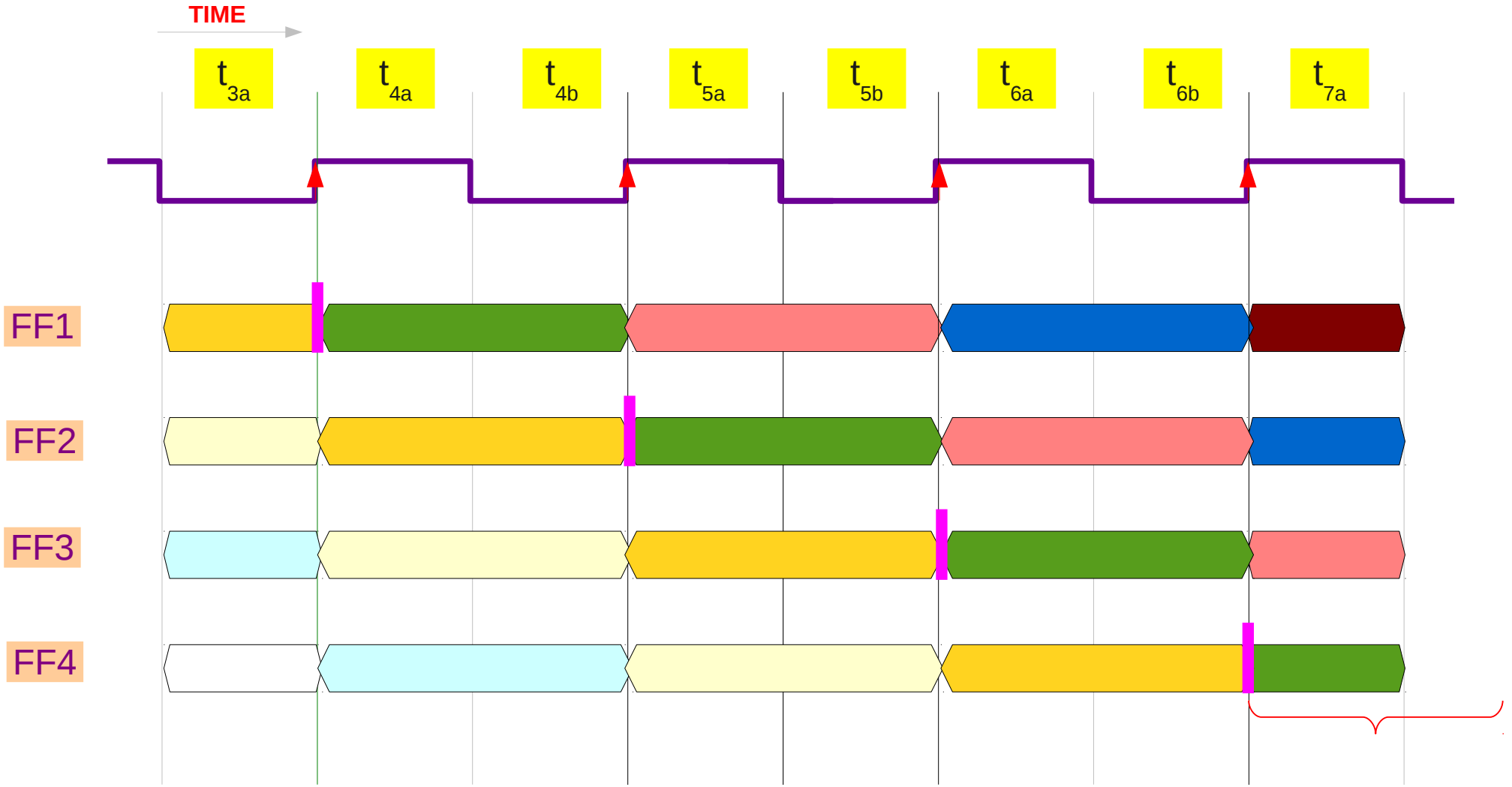
The Latch L3 & L4 Timing (1)



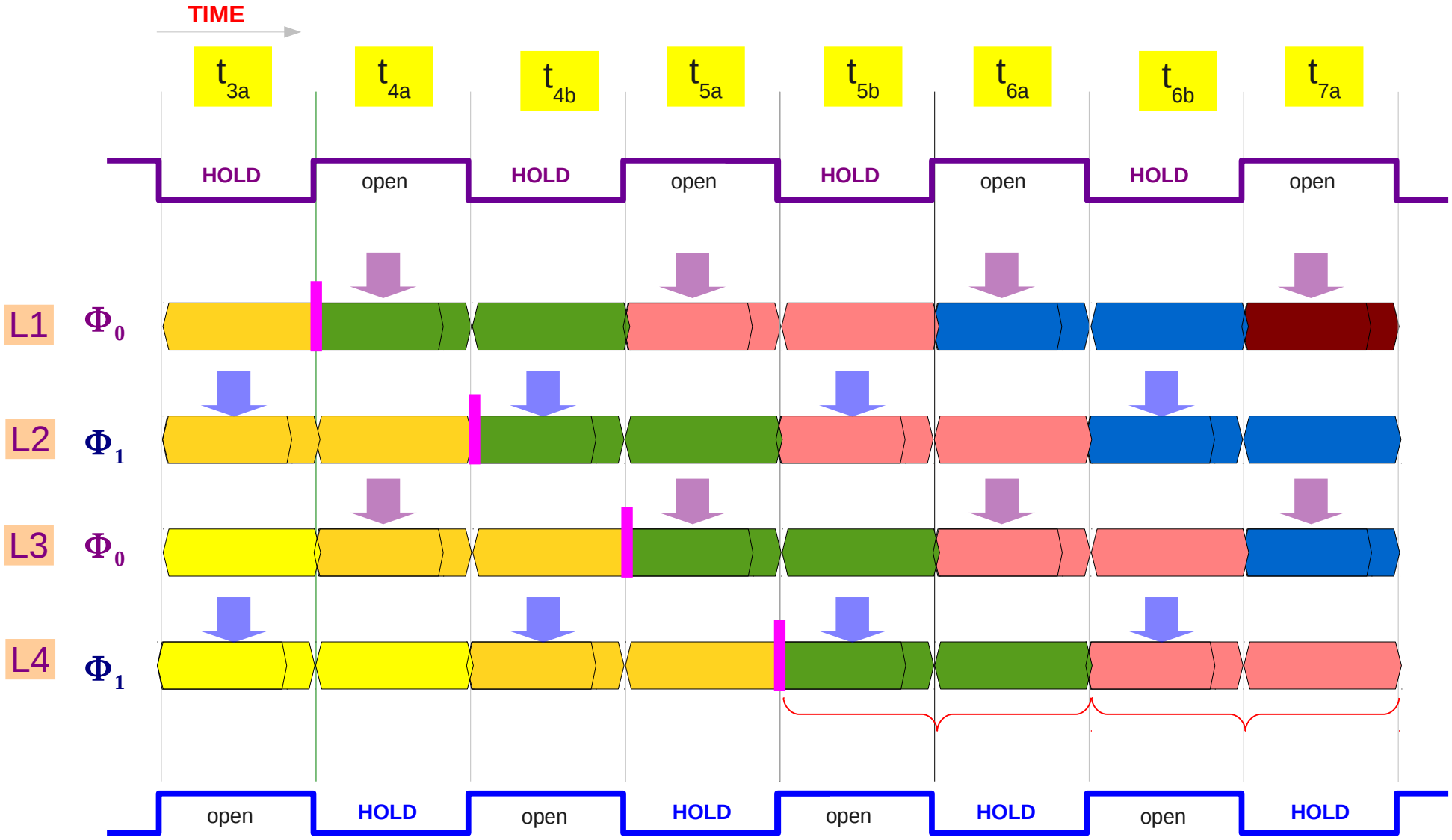
The Latch L3 & L4 Timing (2)



The FlipFlop Based Pipeline Timing



The Latch Based Pipeline Timing



References

[1] http://en.wikipedia.org/