FPGA RAM (C1)

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This document was produced by using LibreOffice and Octave.

Virtex LUT RAM

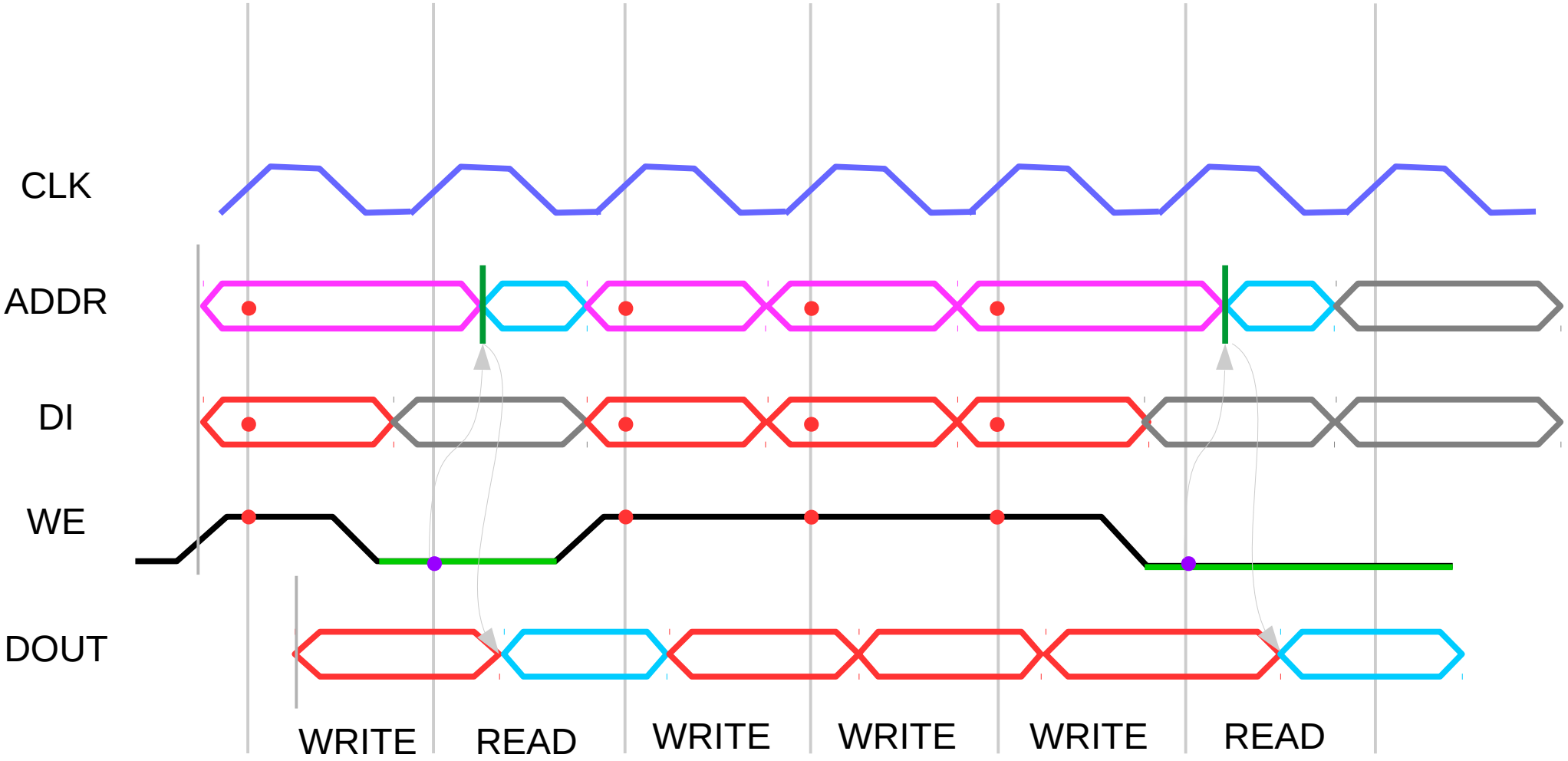
```
module ram16x1(q, a, d, we, clk);
output      q;
input       d;
input [3:0] a;
input       clk, we;

reg         mem [15:0];

always @(posedge clk) begin
   if(we)
      mem[a] <= d;
end

assign q = mem[a];

endmodule
```

Synchronous Write

Asynchronous Read

http://www-inst.eecs.berkeley.edu/~cs150

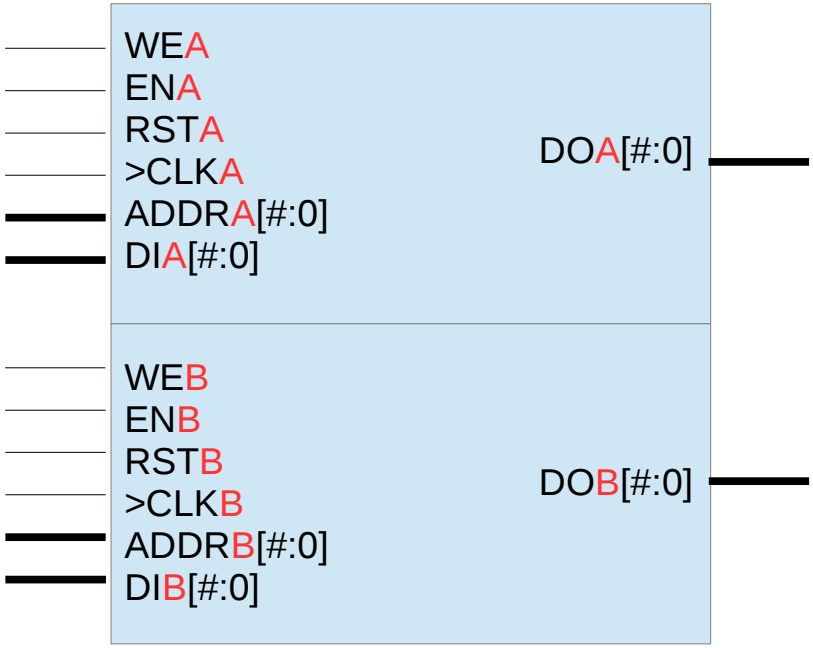
LUT RAM Timing



Xilinx Document

Virtex Block RAM

Every block SelectRAM
- synchronous write
- syncrhronous read
- dual-ported
- independent control signals
- independent data widths
- independent CLKA & CLKB
- 4096-bit RAM



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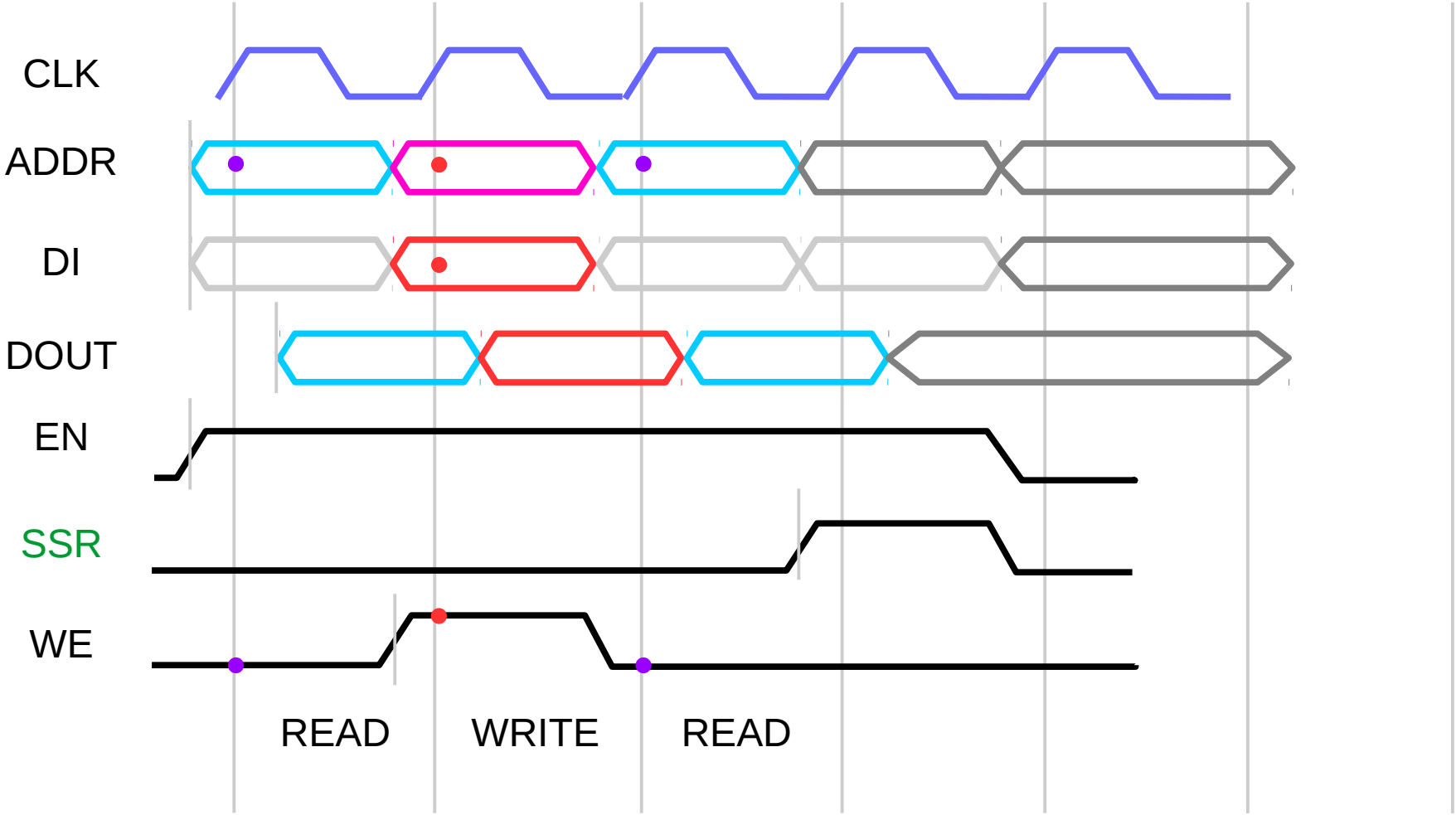
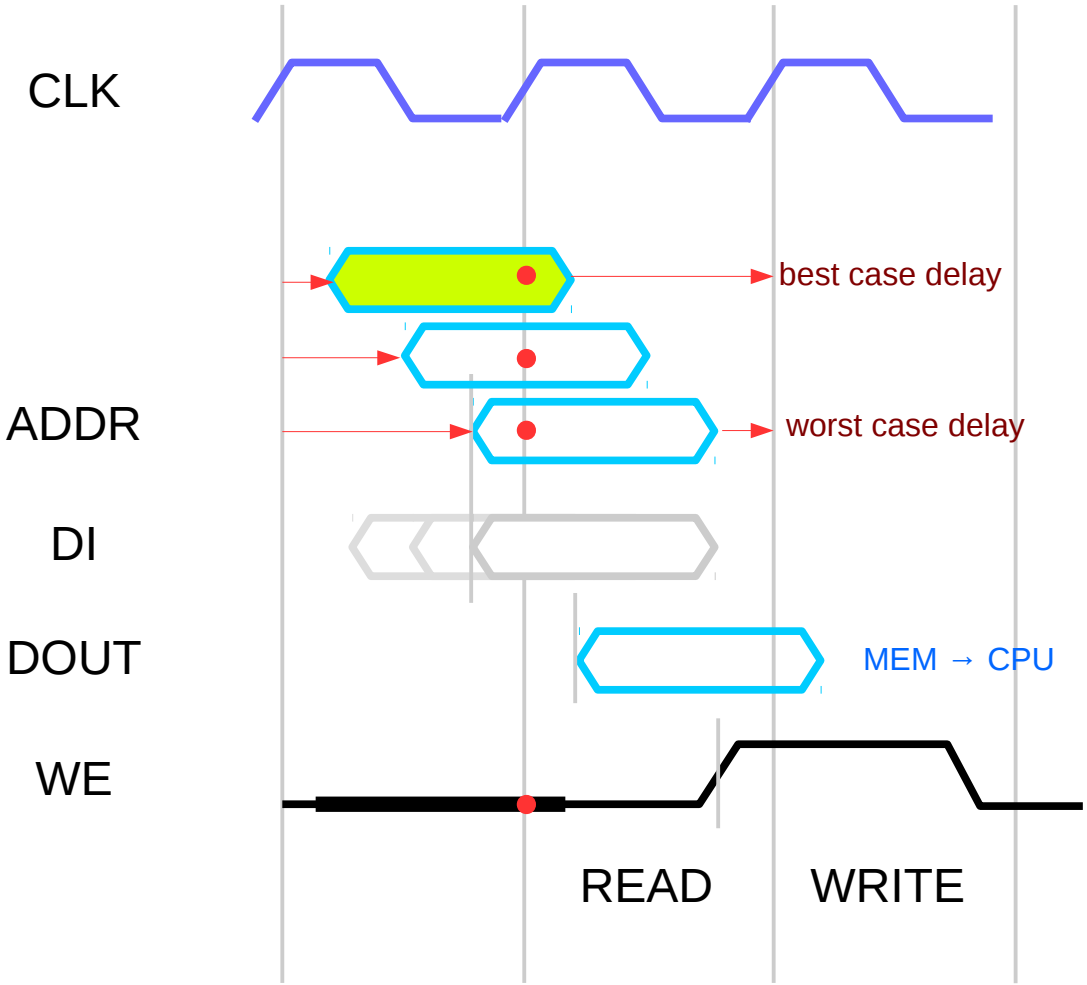
Virtex Block RAM Timing



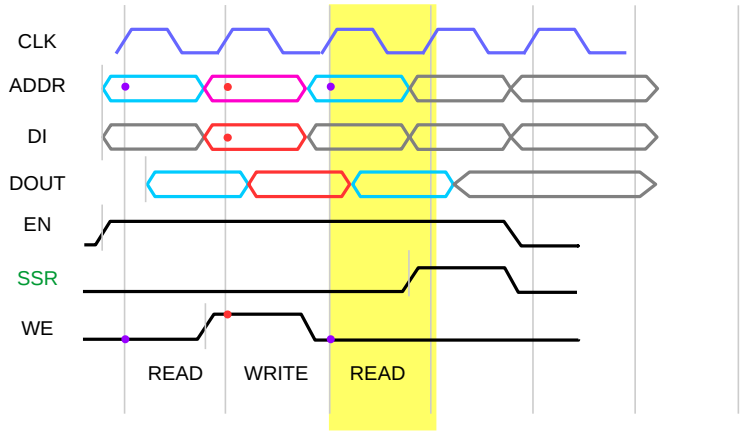
Xilinx Document

SSR (Synchronous Set Rest) value = 1010

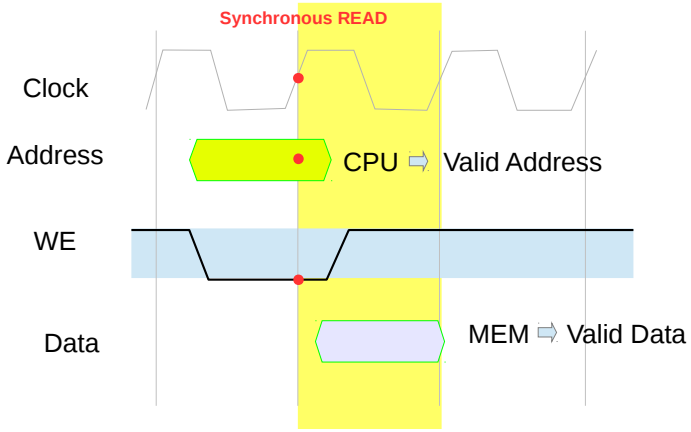
Sync **RD** Cycle - worst & best case



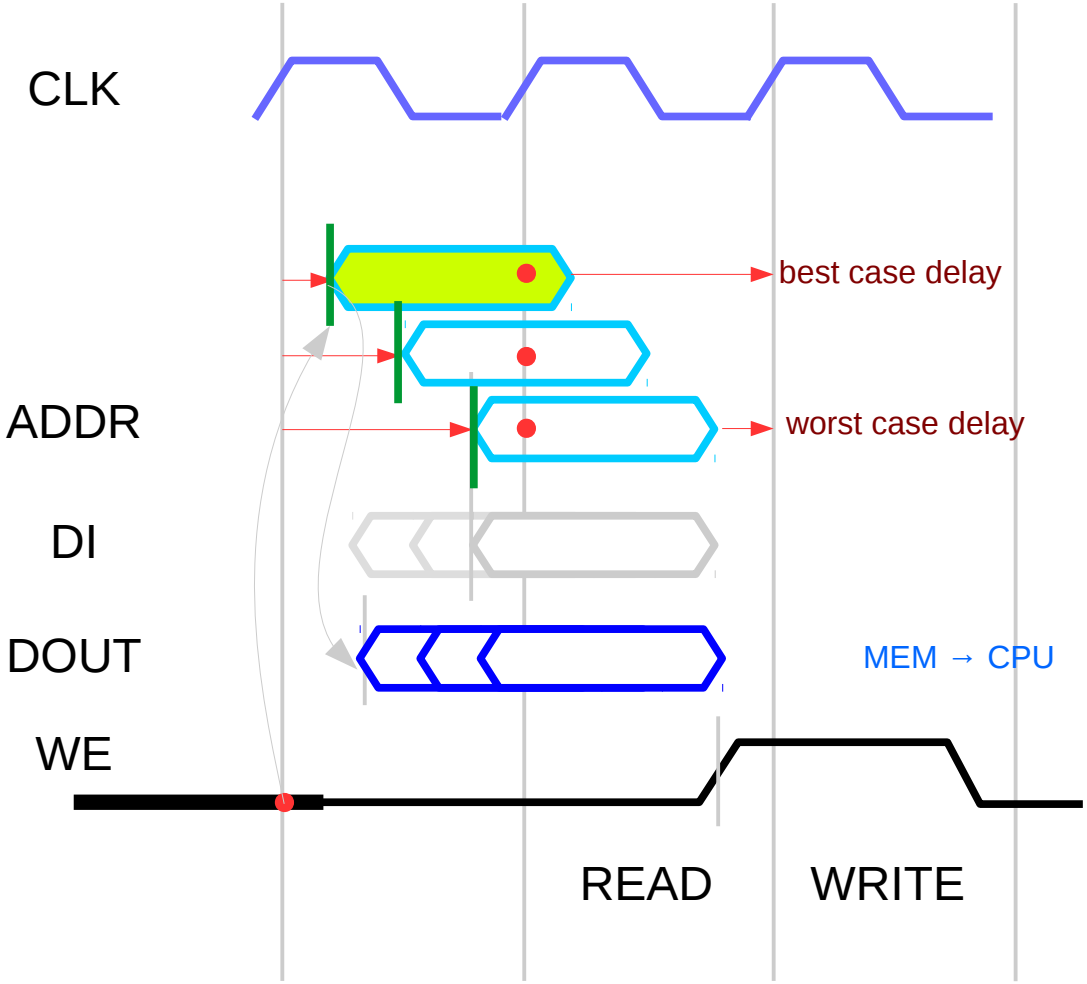
Timing Specification



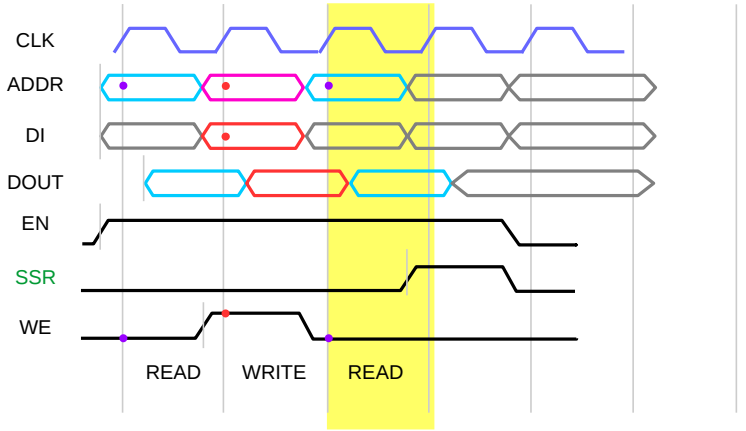
more realistic timing



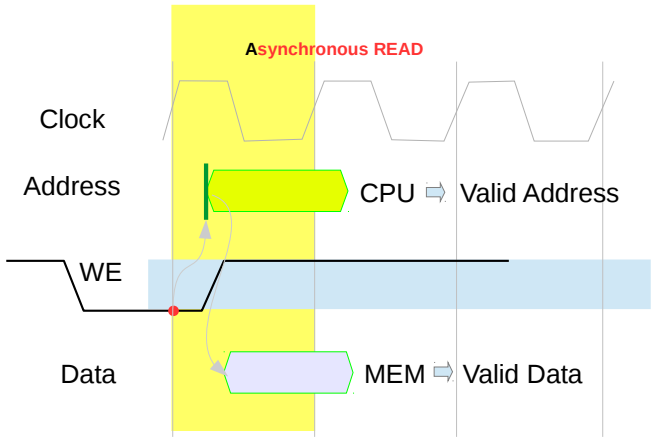
Async **RD** Cycle - worst & best case



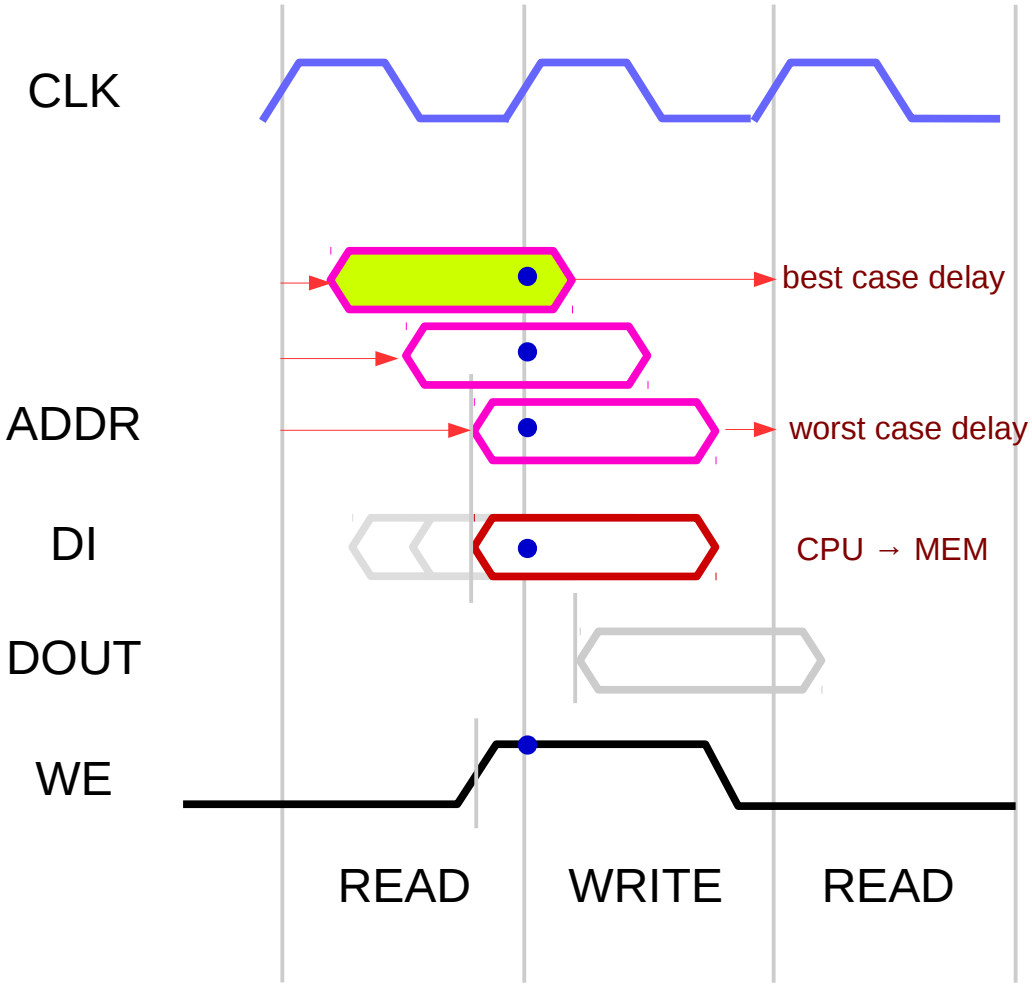
Timing Specification

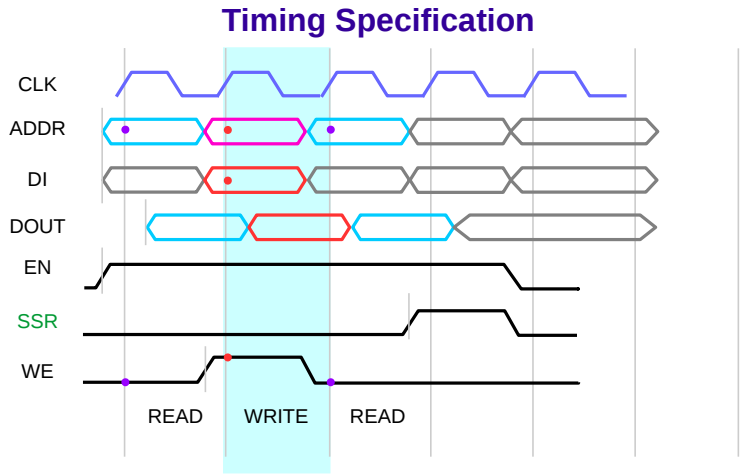


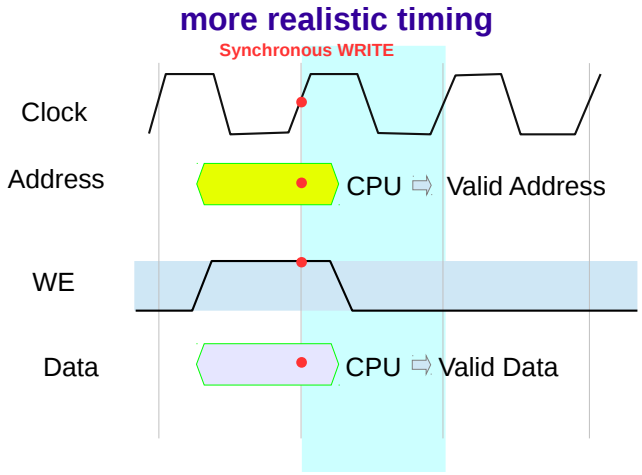
more realistic timing



WR Cycle – worst & best case







Waveform Viewer Timing (1)

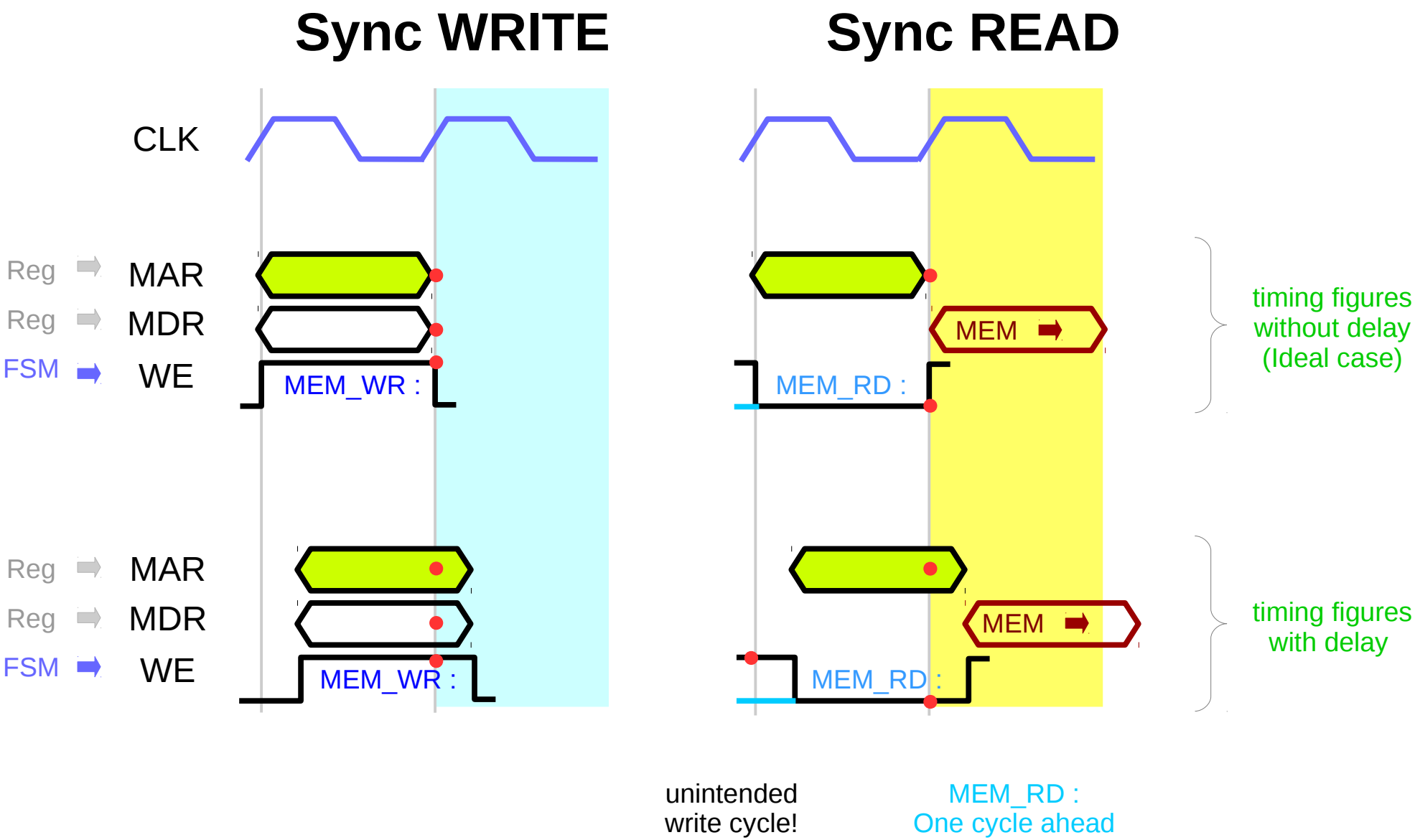
* timing figures without delay (Ideal case)

RTL functional simulation

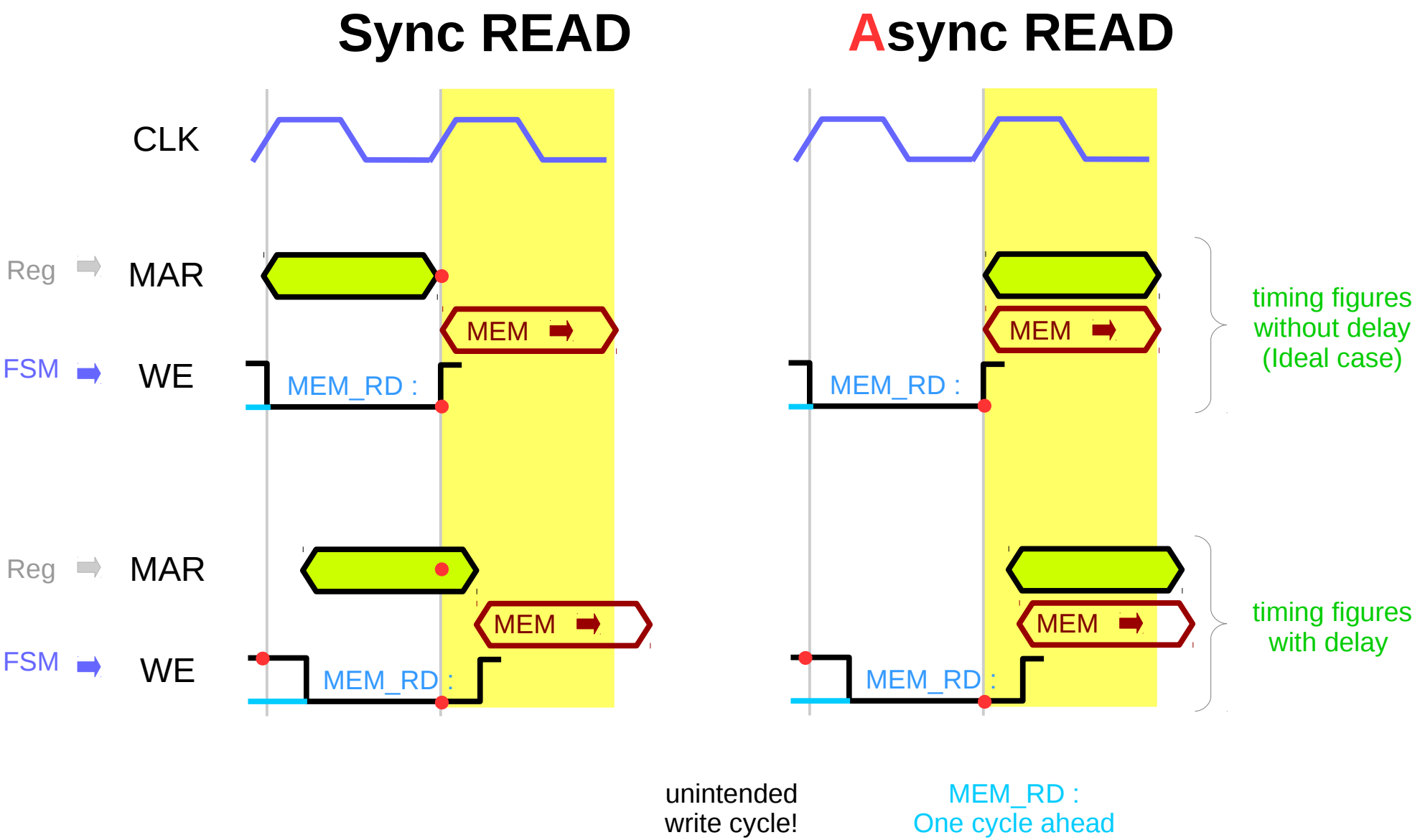
* timing figures with delay

Gate level simulation
with SDF annotation

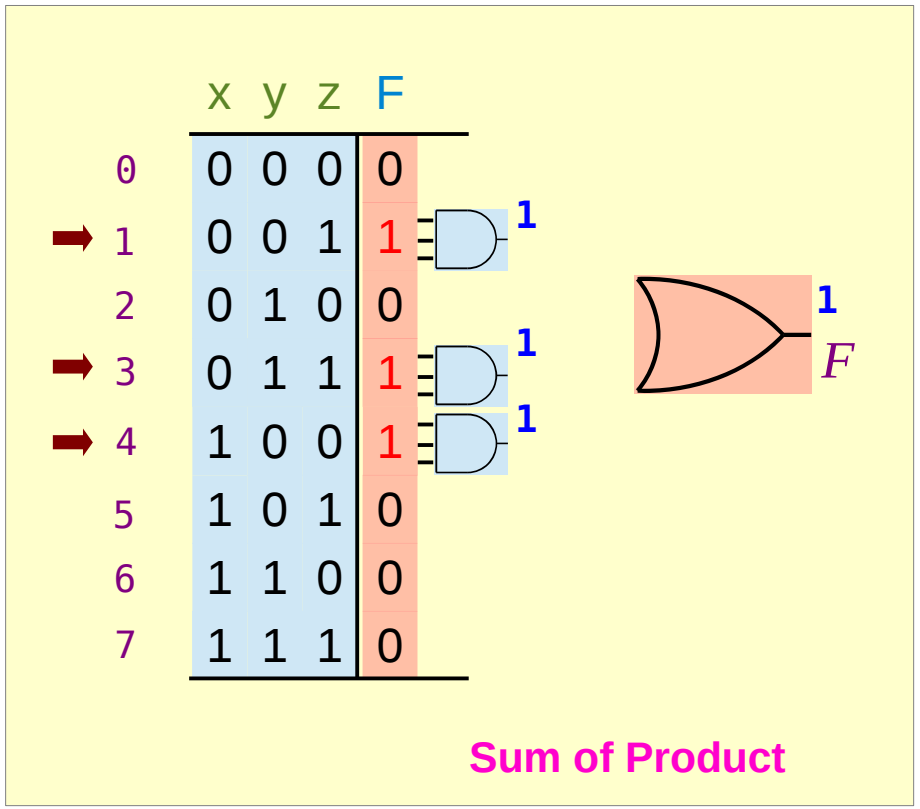
Waveform Viewer Timing (2)

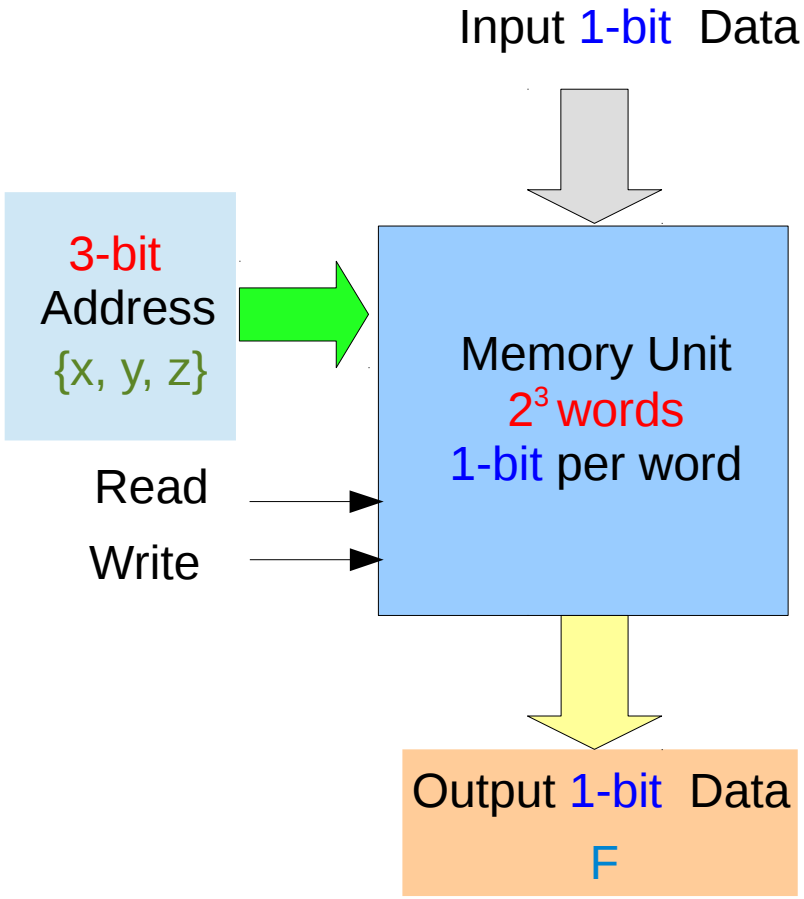


Waveform Viewer Timing (3)



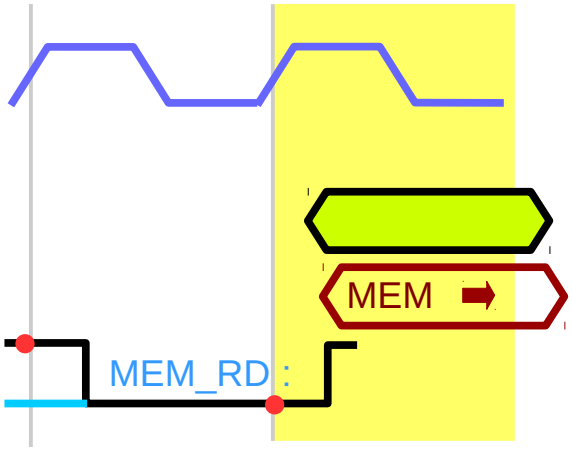
LUT as a combination logic block

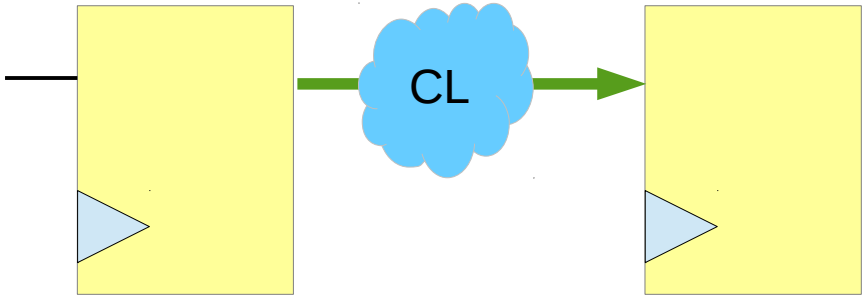




LUT : Async Read

Async READ



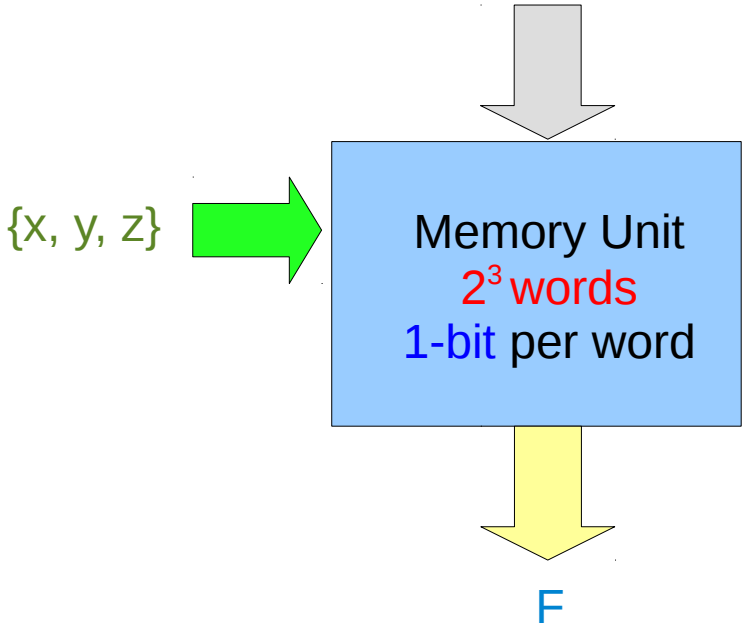


Address : Inputs
Data : Outputs

The outputs available in the same cycle where the inputs are applied

Combinational Logic Block :
A set of Boolean Functions

LUT Data Write



References

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