Path Delay

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## Path Delay

Max-Path<br>Min-Path<br>Critical Path<br>Timing Check<br>False Path<br>Multi-Cycle Path

## Max Path / Min Path

Max path


## Rise / Fall Times


Fall Time

$$
\frac{\beta_{n}}{\beta_{p}}>1 \quad \frac{R_{n}}{R_{p}}<1
$$

$$
\frac{t_{f}}{t_{r}}=\frac{2.2 \tau_{n}}{2.2 \tau_{p}} \quad \frac{\tau_{n}}{\tau_{p}}=\frac{R_{n} C_{\text {out }}}{R_{p} C_{\text {out }}}=\frac{R_{n}}{R_{p}}<1
$$

Max delay



## PVT Variation

$\left\{\begin{array}{l}\text { Process } \\ \text { Voltage } \\ \text { Temperature }\end{array}\right.$

High temperature Max delay
Low temperature min delay

## FF Output Delay



$$
\begin{aligned}
& \text { flipflop clock-to-q } \\
& \qquad t_{c c q} \leq t_{\text {delay }} \leq t_{p c q} \\
& \text { min delay } \quad \text { Max delay }
\end{aligned}
$$

## Path Delay



## Reg-to-Reg Delay (1)



$$
t_{c c q} \leq t_{F F} \leq t_{p c q}
$$

min delay Max delay

$$
t_{c d} \leq t_{c o m b} \leq t_{p d}
$$

min delay
Max delay

$$
\begin{aligned}
t_{c c q}+t_{c d} \leq t_{\text {delay }} \leq & t_{p c q}+t_{p d} \\
\text { min delay } & \text { Max delay }
\end{aligned}
$$

## Reg-to-Reg Delay (2)



$$
\begin{gathered}
t_{c c q} \leq t_{F F} \leq t_{p c q} \\
\text { min delay Max delay } \\
t_{c d} \leq t_{c o m b} \leq t_{p d} \\
\text { min delay Max delay } \\
\\
\hline t_{c c q}+t_{c d} \leq t_{d e l a y} \leq t_{p c q}+t_{p d} \\
\hline \min \text { delay } \quad \text { Max delay }
\end{gathered}
$$

## Setup Time / Hold Time

Setup Time OK


Setup Time Violation


Hold Time OK


Hold Time Violation


## Setup Time / Hold Time

## Setup Time Violation



Since the delay is too small signal passes through the 2nd FF


## Waveform (1)

File Edit Search Time Markers View Help



## All gate delays are assumed to be the same

## Waveform (2)

## GTKWave - /home/young/WorkSpace/test.vcd

File Edit Search Time Markers View Help



| Type Signals | Signals |  |
| :---: | :---: | :---: |
| wire $\mathrm{A}[3: 0]$ |  |  |
| wire $\mathrm{B}[3: 0]$ |  |  |
| wire C[3:1] |  |  |
| wire Ci |  |  |
| wire Co |  |  |
| wire $\mathrm{S}[3: 0]$ |  |  |
| Filter: |  |  |
| Append | Insert | Replace |




## False Path

## Multi-Cycle Path

## References

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