Ripple Carry Adder (1A)

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Please send corrections (or suggestions) to youngwlim@hotmail.com.

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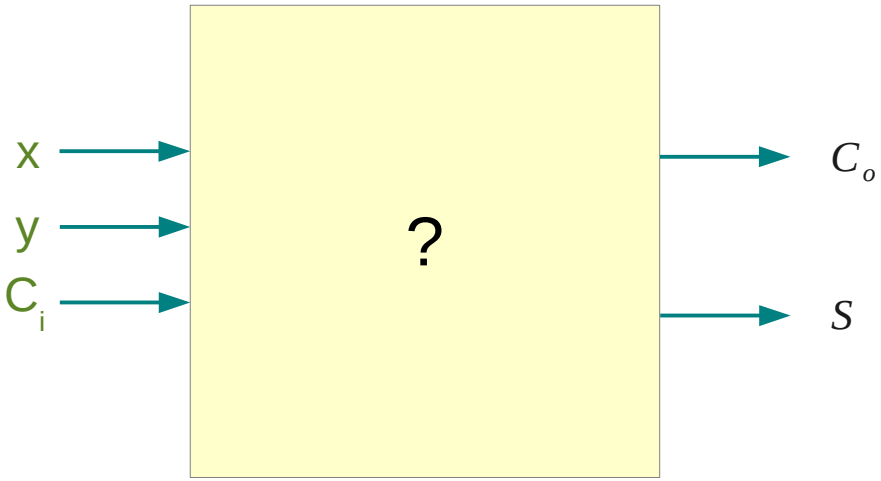
Truth Table

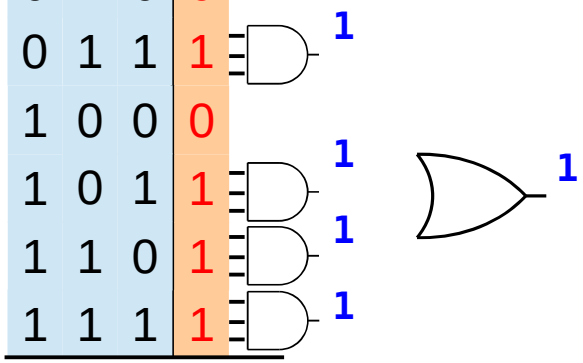
x	y	C_i	C_o	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

inputs output

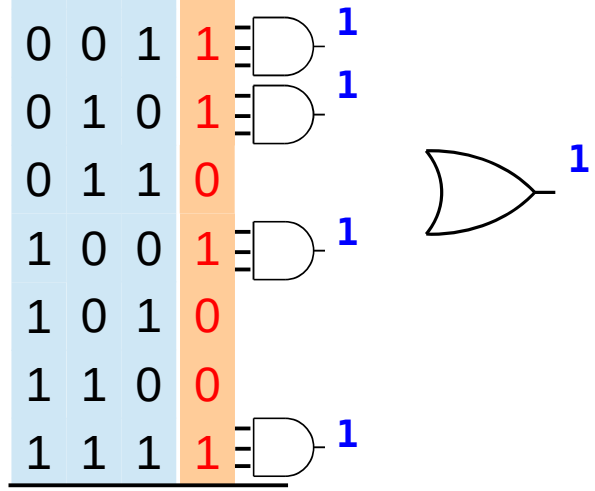


SOP

x	y	C_i	C_o
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



x	y	C_i	S
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

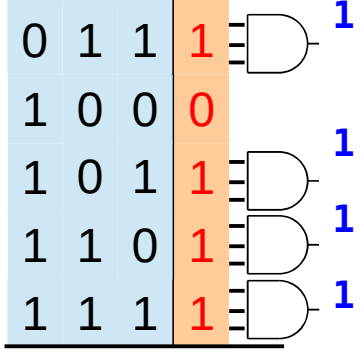


$$C_o = \bar{x}\,y\,C_i + x\,\bar{y}\,C_i + x\,y\,\bar{C}_i + x\,y\,C_i$$

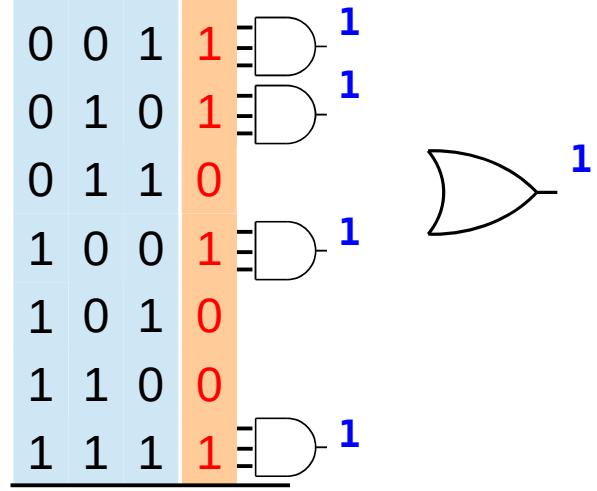
$$S = \bar{x}\,\bar{y}\,C_i + \bar{x}\,y\,\bar{C}_i + x\,\bar{y}\,\bar{C}_i + x\,y\,C_i$$

K-Map

x	y	C_i	C_o
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

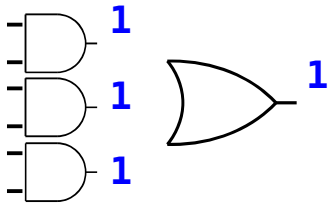


x	y	C_i	S
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



x \ y	0	1
0	0	0
1	0	1
1	1	1
0	1	0

C_i



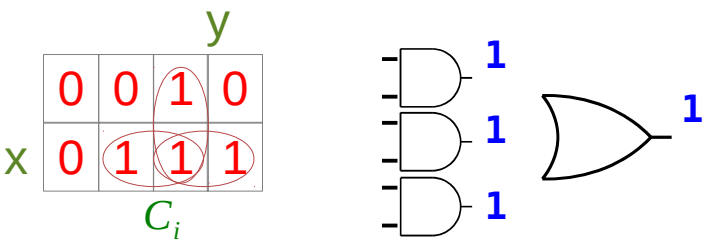
x \ y	0	1
0	0	1
1	1	0
1	0	1
0	1	0

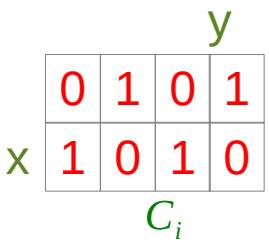
C_i

$$C_o = y C_i + x C_i + x y$$

$$S = \bar{x}\,\bar{y}\,C_i + \bar{x}\,y\,\bar{C}_i + x\,\bar{y}\,\bar{C}_i + x\,y\,C_i$$

Boolean Algebra





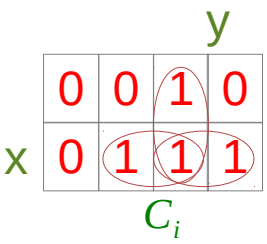
$$C_o = y C_i + x C_i + x y$$

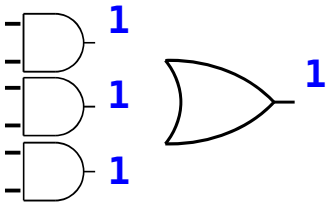
$$\begin{aligned} C_o &= (x + y) C_i + x y \\ &= (\bar{x} y + x \bar{y} + xy) C_i + x y \\ &= (\bar{x} y + x \bar{y}) C_i + xy (C_i + 1) \\ &= (x \oplus y) C_i + xy \end{aligned}$$

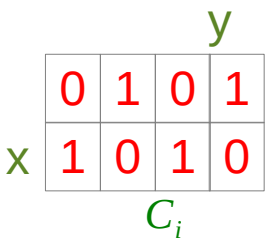
$$S = \bar{x}\,\bar{y}\,C_i + \bar{x}\,y\,\bar{C}_i + x\,\bar{y}\,\bar{C}_i + x\,y\,C_i$$

$$\begin{aligned} S &= (\bar{x}\,\bar{y} + xy) C_i + (\bar{x}\,y + x\,\bar{y}) \bar{C}_i \\ &= \overline{(x \oplus y)} C_i + (x \oplus y) \bar{C}_i \\ &= (x \oplus y) \oplus C_i \end{aligned}$$

Boolean Algebra





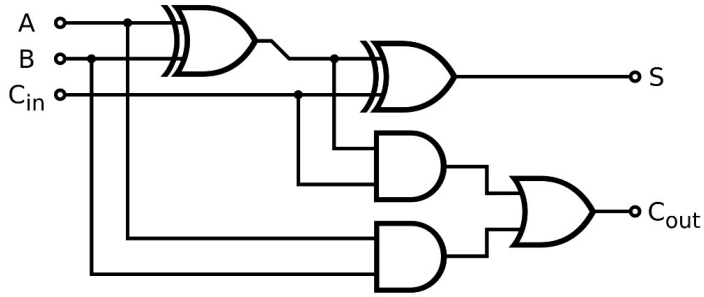


$$C_o = y C_i + x C_i + x y$$

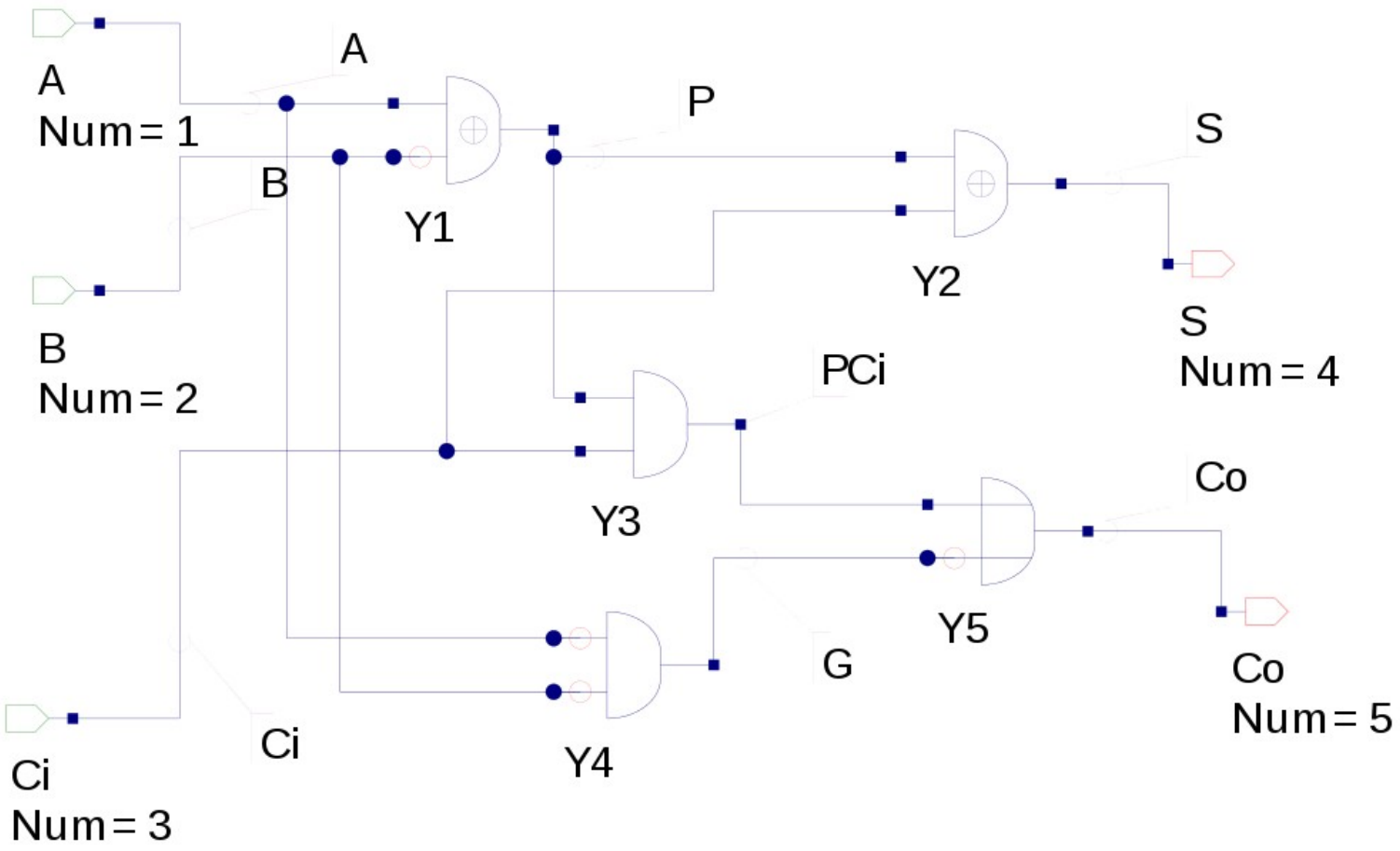
$$\begin{aligned} C_o &= (x + y) C_i + x y \\ &= (\bar{x} y + x \bar{y} + xy) C_i + x y \\ &= (\bar{x} y + x \bar{y}) C_i + xy (C_i + 1) \\ &= (x \oplus y) C_i + xy \end{aligned}$$

$$S = \bar{x}\,\bar{y}\,C_i + \bar{x}\,y\,\bar{C}_i + x\,\bar{y}\,\bar{C}_i + x\,y\,C_i$$

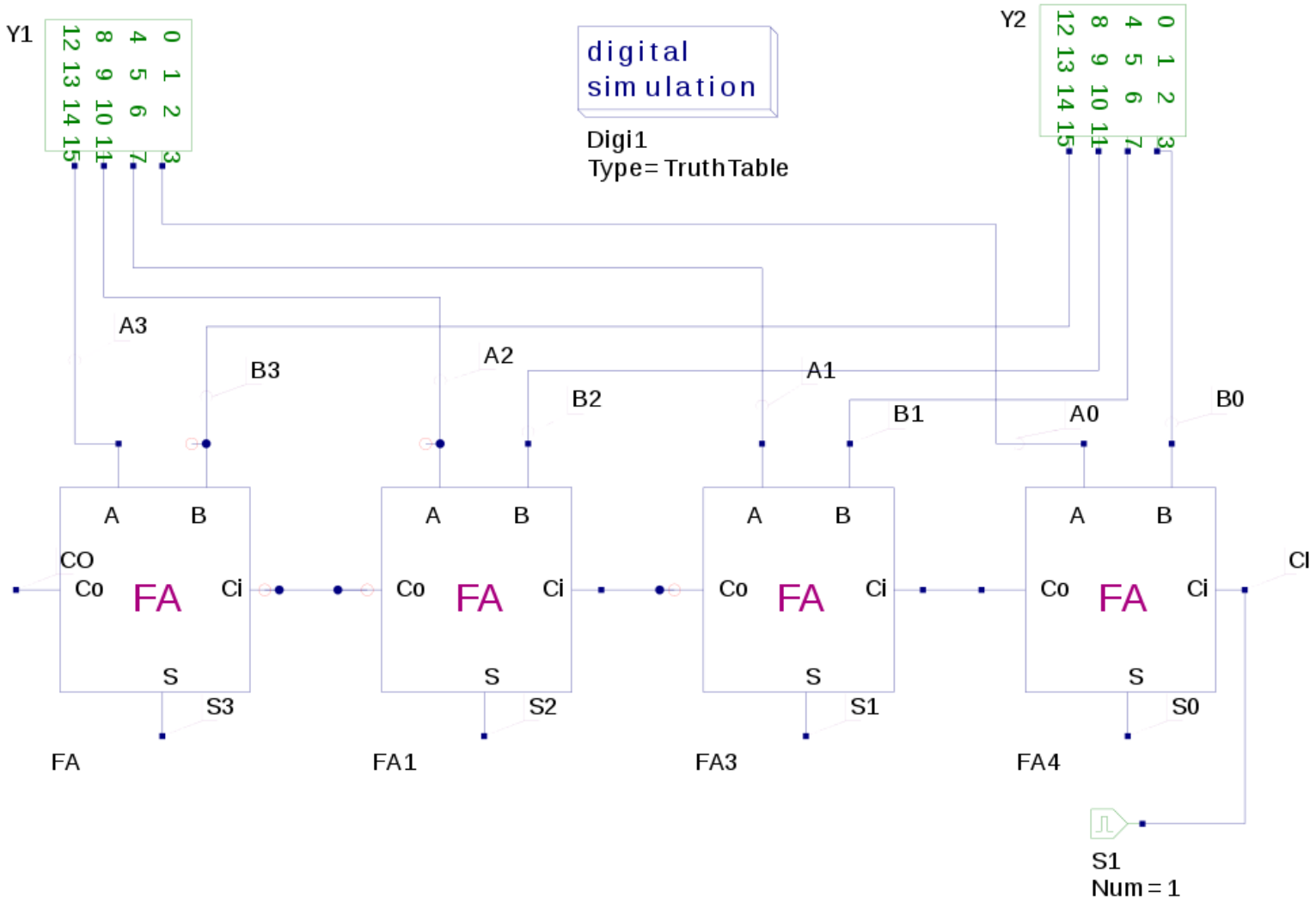
$$\begin{aligned} S &= (\bar{x}\,\bar{y} + xy) C_i + (\bar{x}\,y + x\,\bar{y}) \bar{C}_i \\ &= \overline{(x \oplus y)} C_i + (x \oplus y) \bar{C}_i \\ &= (x \oplus y) \oplus C_i \end{aligned}$$



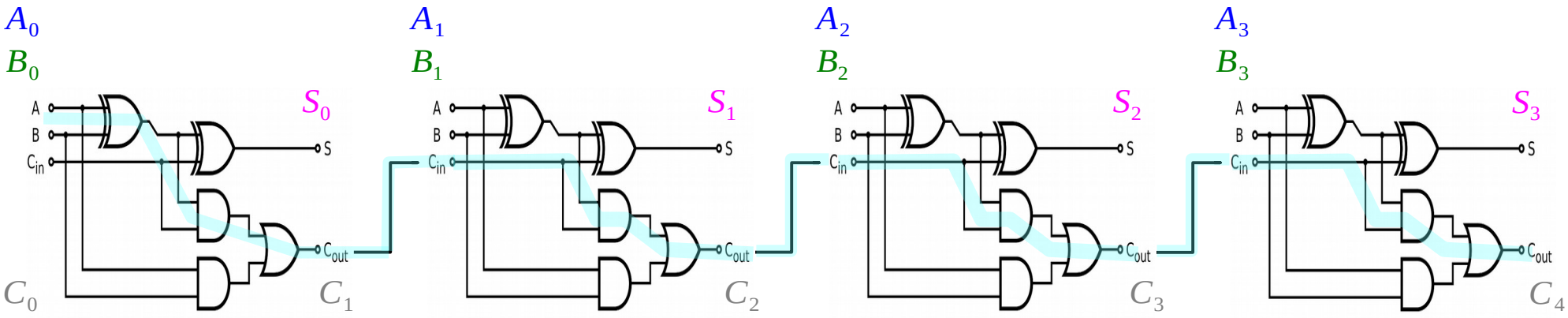
Full Adder in Qucs



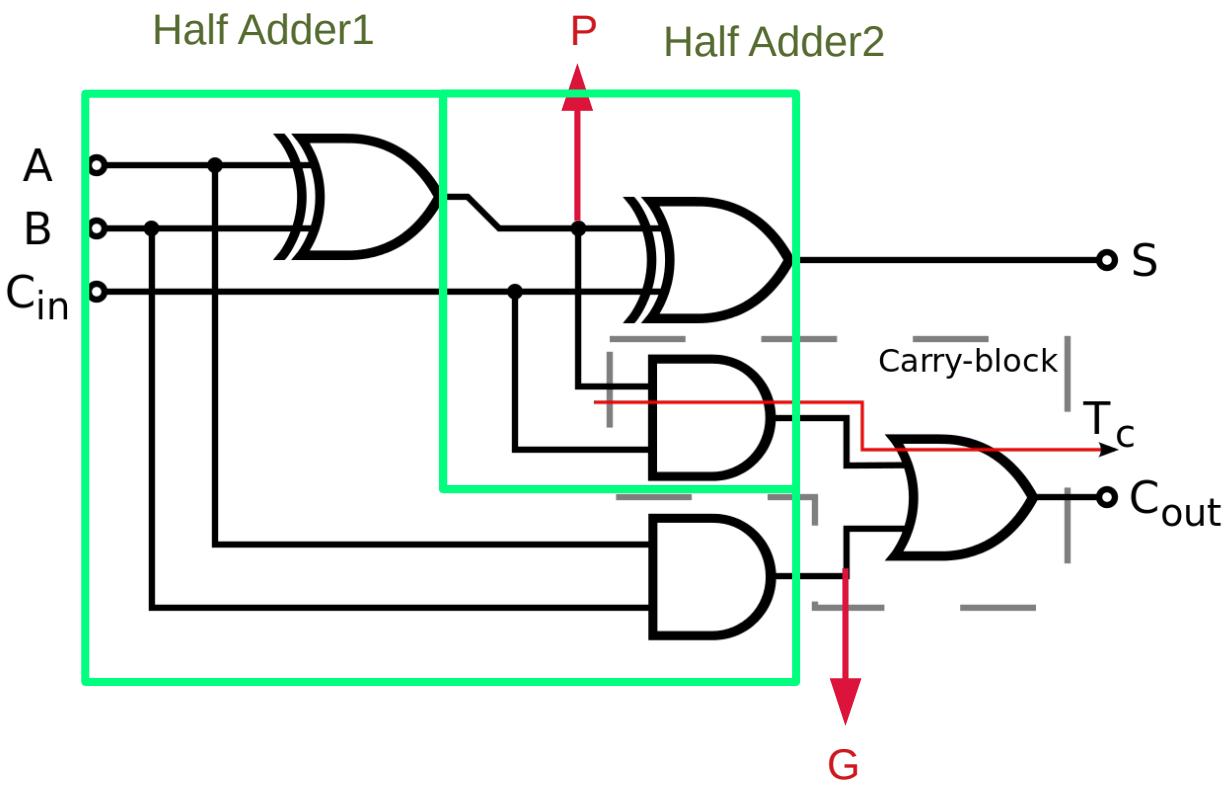
4-Bit Adder in Qucs

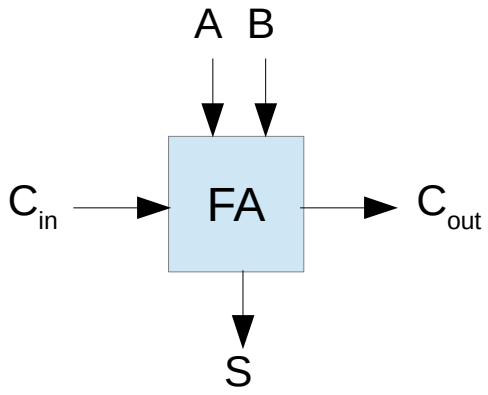


Critical Path



Gate Level Full Adder



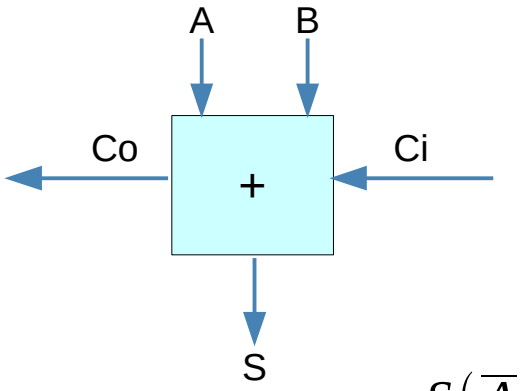


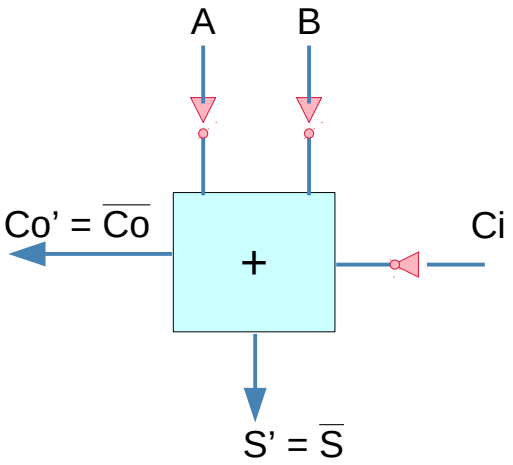
Www.cs.tufts.edu/103/notes/Lecture14(Adders-2).pdf

Inverting FA inputs

X	Y	Cin	Cout	S
0	0	0	0	0
0	1	0	0	1
1	0	0	0	1
1	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	0	1	1	0
1	1	1	1	1

$\overline{X}$	$\overline{Y}$	$\overline{Cin}$	$\overline{Cout}$	$\overline{S}$
1	1	1	1	1
1	0	1	1	0
0	1	1	1	0
0	0	1	0	1
1	1	0	1	0
1	0	0	0	1
0	1	0	0	1
0	0	0	0	0

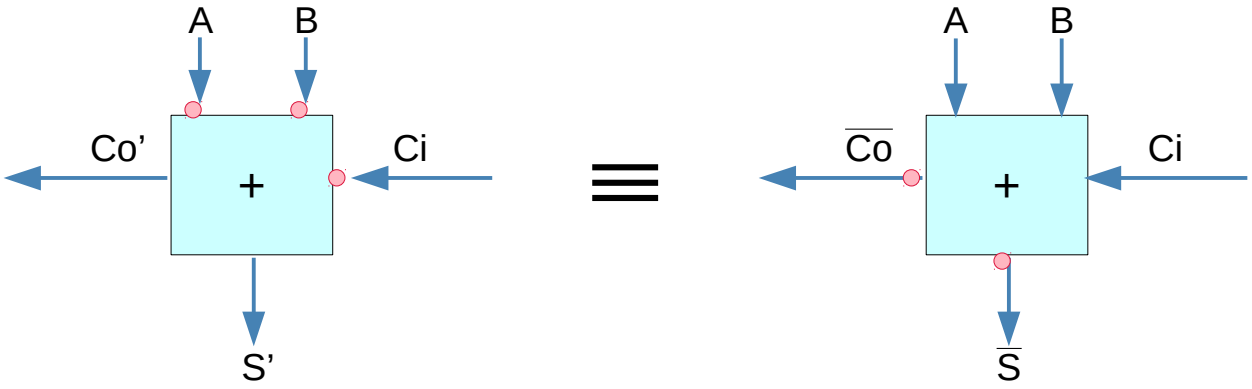




$$S(\overline{A},\overline{B},\overline{C_i}) = \overline{S(A,B,C_i)}$$

$$C_o(\overline{A},\overline{B},\overline{C_i}) = \overline{C_o(A,B,C_i)}$$

Inversion Property

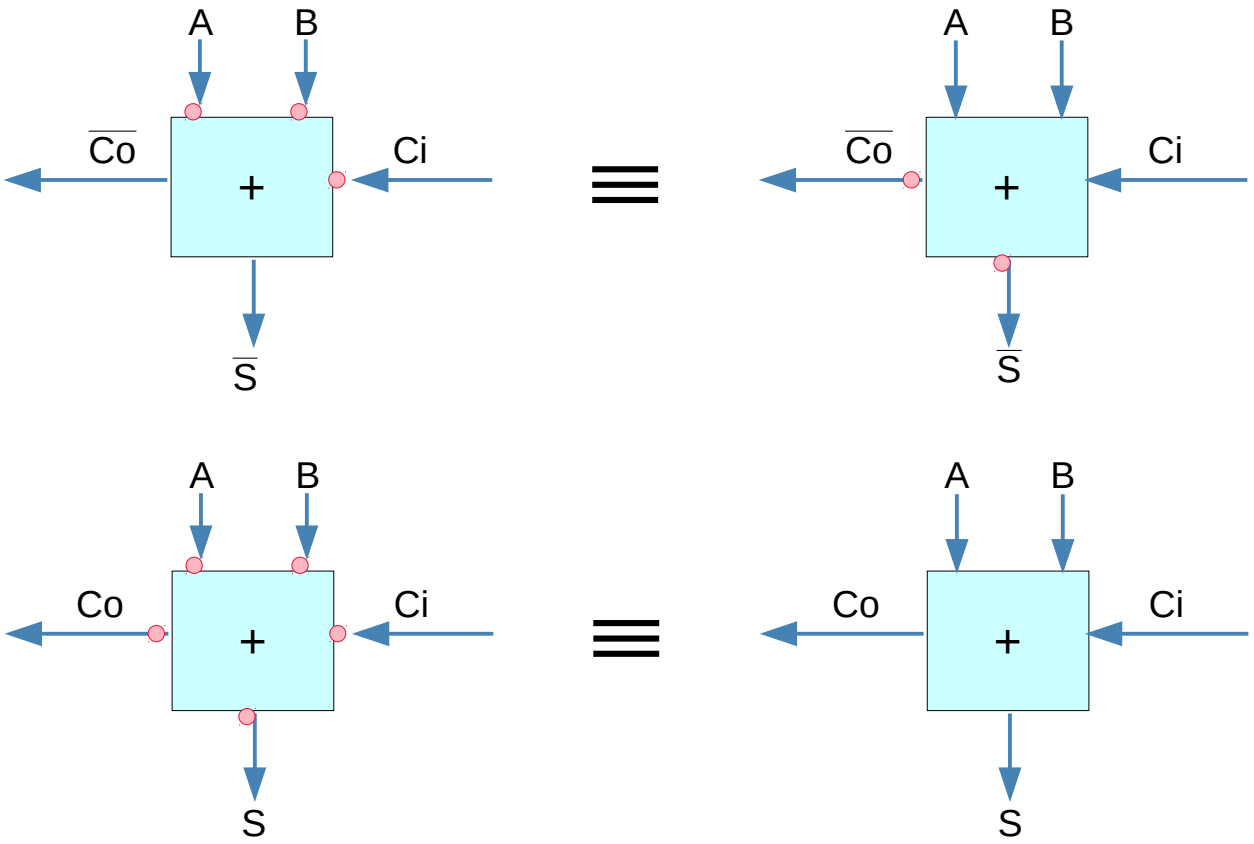


Inverting all inputs to a FA
Results in inverted values for all outputs

$$S(\overline{A},\overline{B},\overline{C_i}) = \overline{S(A,B,C_i)}$$

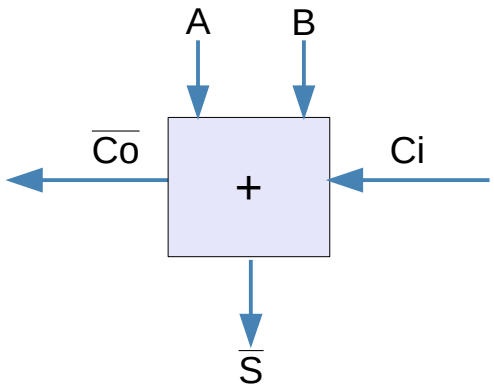
$$C_o(\overline{A},\overline{B},\overline{C_i}) = \overline{C_o(A,B,C_i)}$$

Equivalent Relations



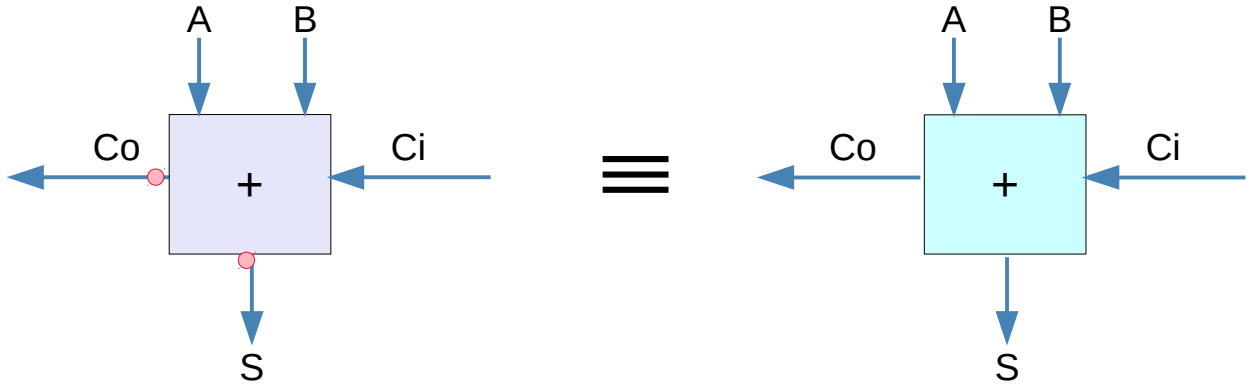
http://www.ece.ucdavis.edu/acsel, Oklobdzija originally from Rabaey

Inverted FA Outputs



Most CMOS transistor level FAs (full adders) have inverted outputs $\overline{Co}$ and $\overline{S}$ by default

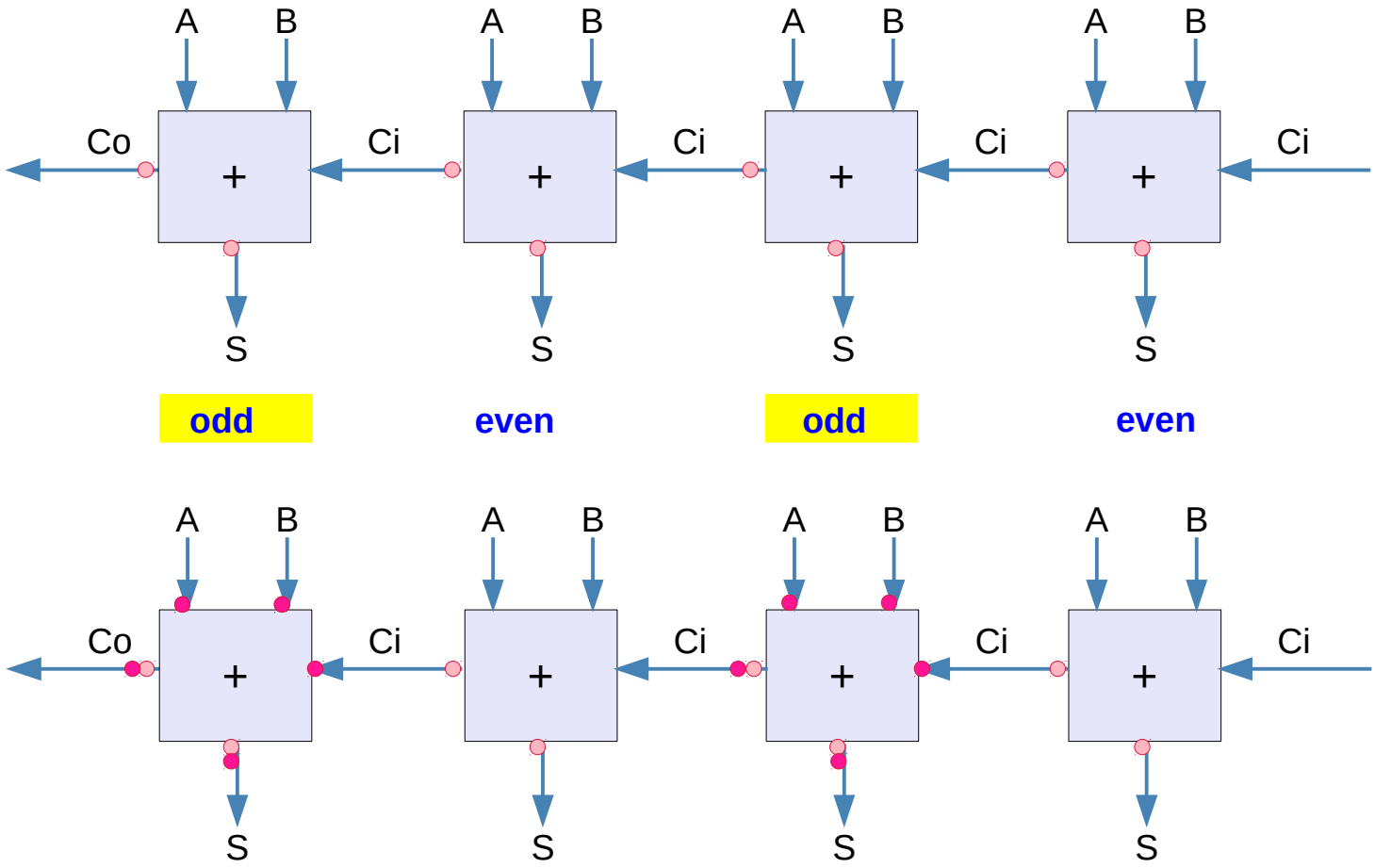
Need inverter to get normal output



http://www.ece.ucdavis.edu/acsel, Oklobdzija originally from Rabaey

Applying Inversion Property

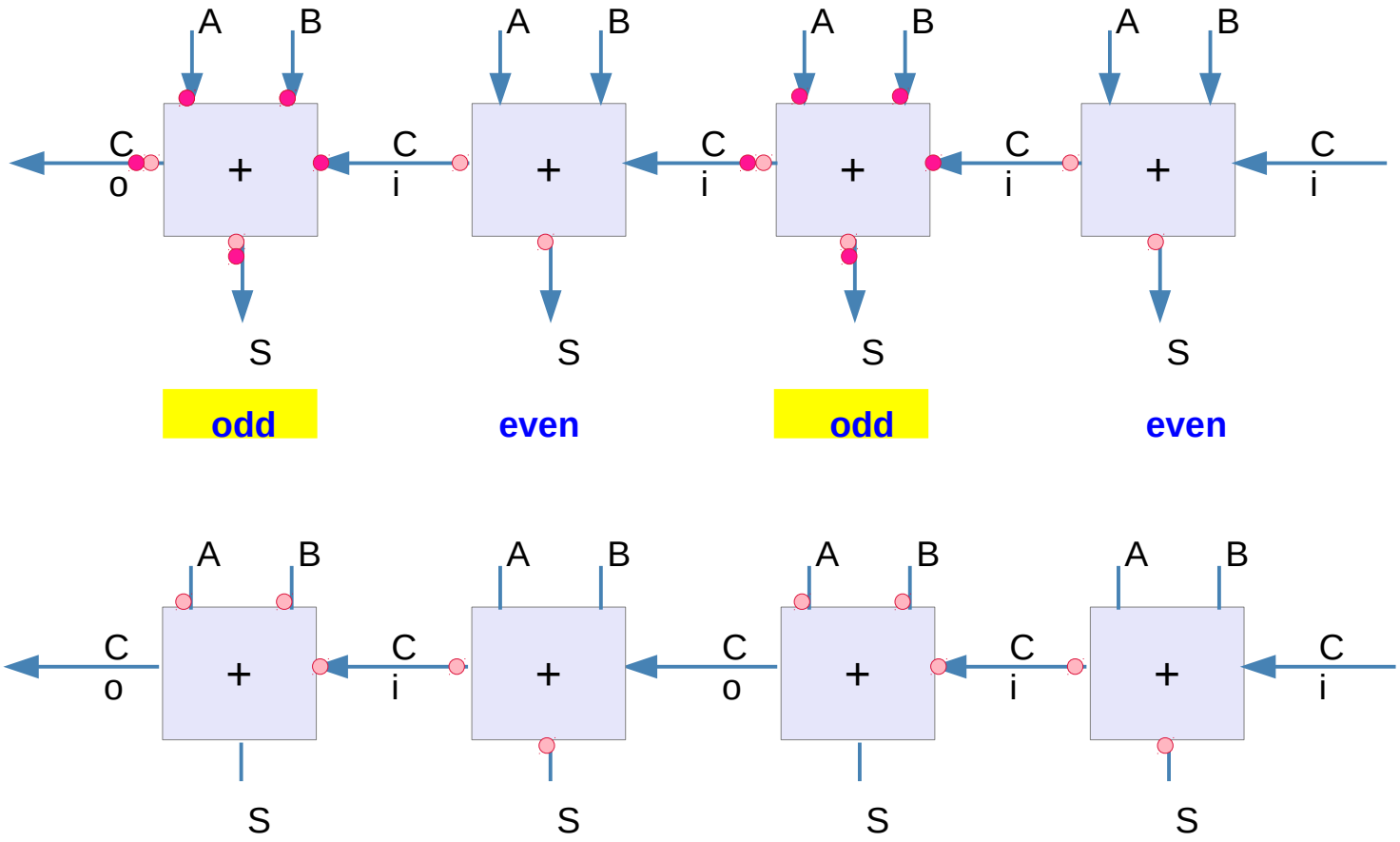
FA with inverted outputs



http://www.ece.ucdavis.edu/acsel, Oklobdzija originally from Rabaey

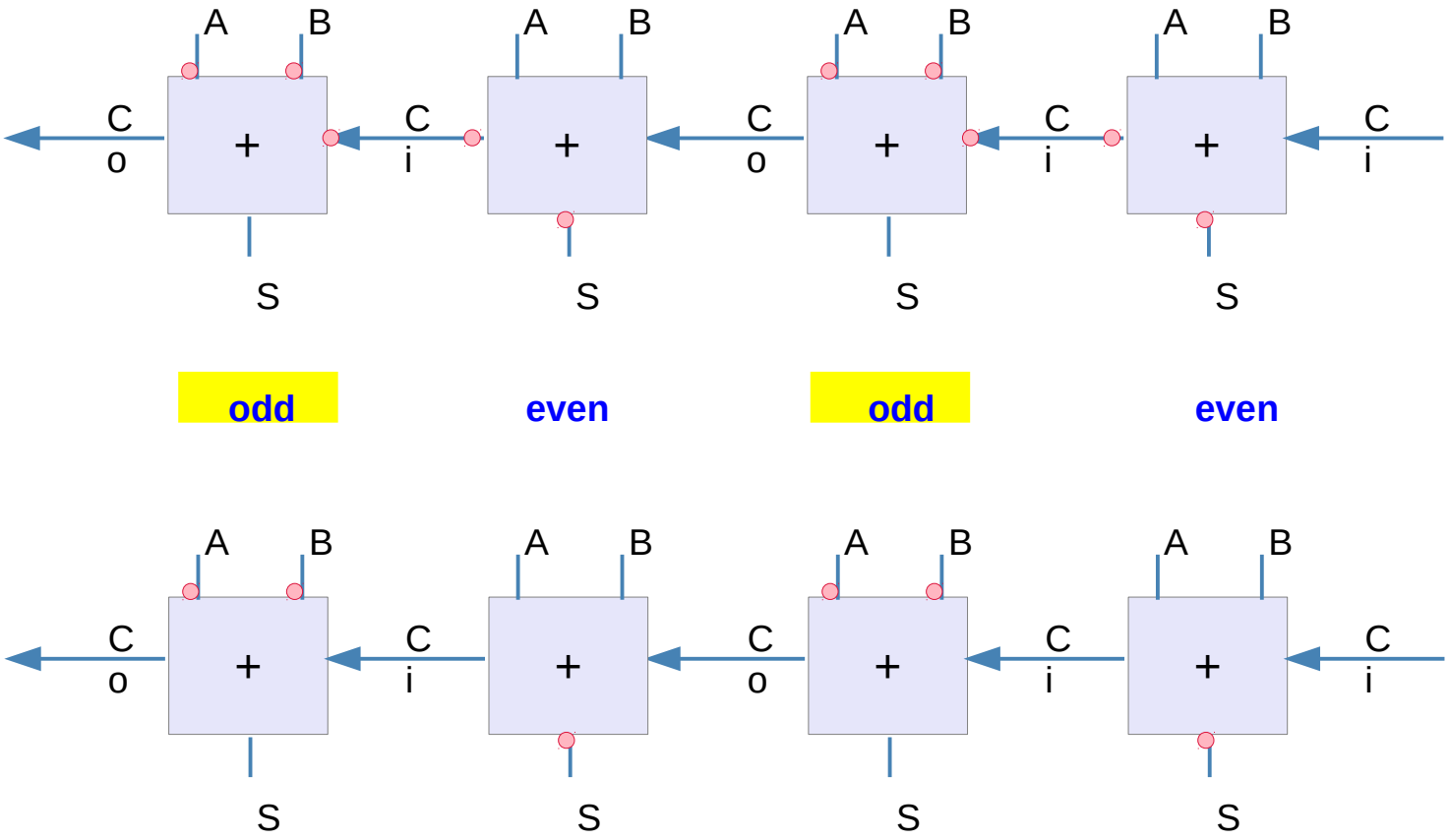
Applying Inversion Property

FA with inverted outputs – inversion property applied



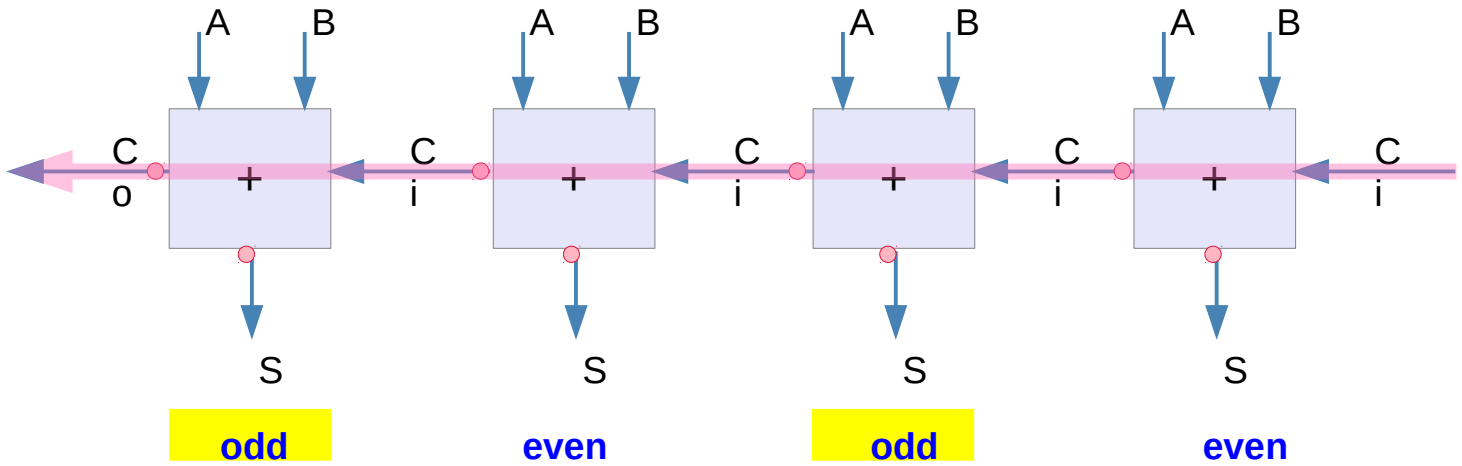
Removing redundant inverters

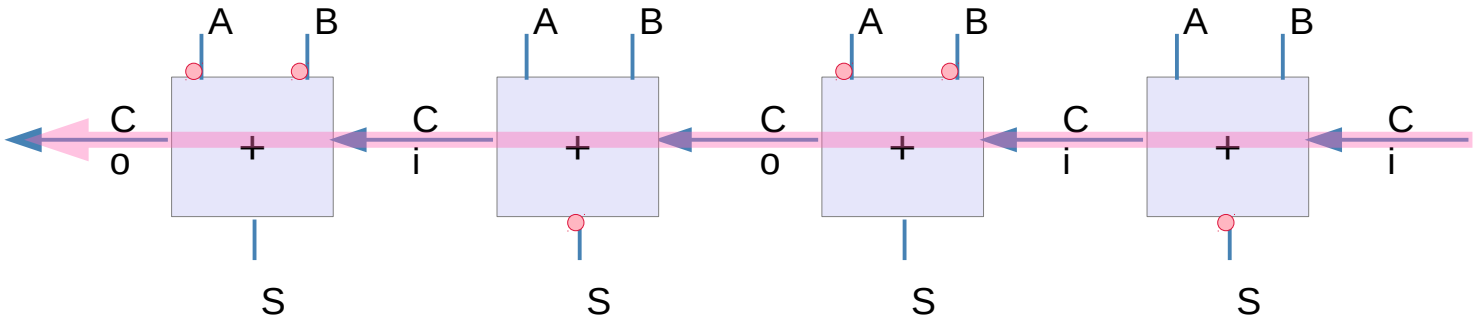
FA with inverted outputs – inversion property applied, redundant inverters removed



Inverters on the critical path

4 inverters on the critical path

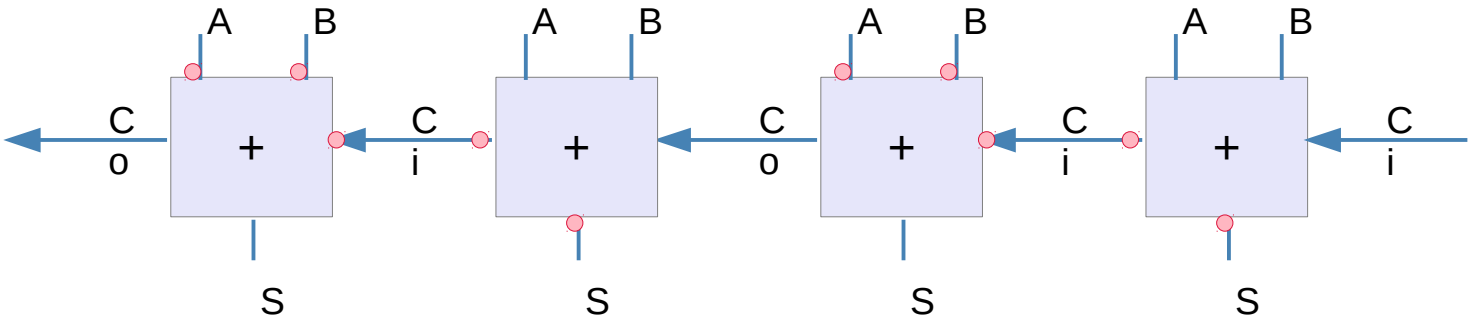




0 inverters on the critical path

http://www.ece.ucdavis.edu/acsel, Oklobdzija originally from Rabaey

Minimize the critical paths



Minimizes the critical paths (the carry chain)
by eliminating inverters between the FAs
(will need to increase the transistor sizing)

References

[1] en.wikipedia.org
[2] D.M. Harris, S. L. Harris, “Digital Design and Computer Architecture”
[3] http://www.aoki.ecei.tohoku.ac.jp/arith/mg/algorithm.html