

Sequential Gates (3B)

Transistor Level Design

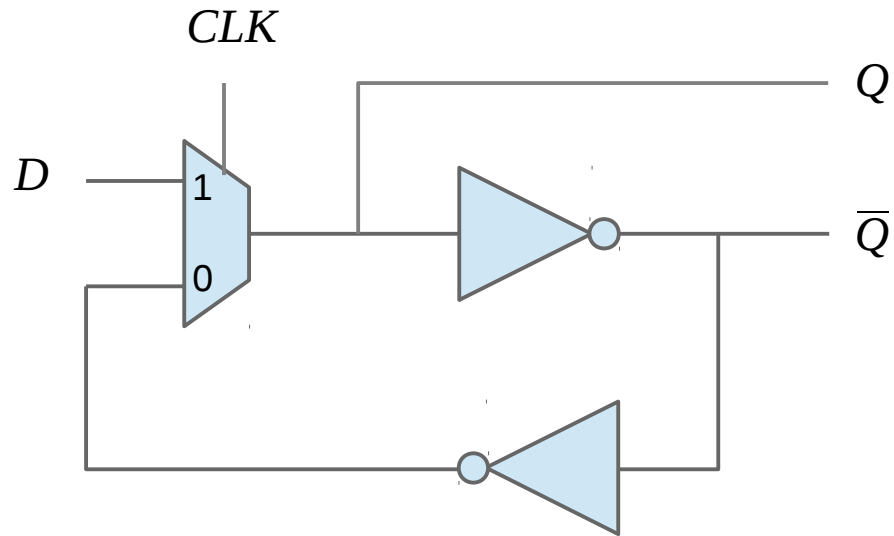
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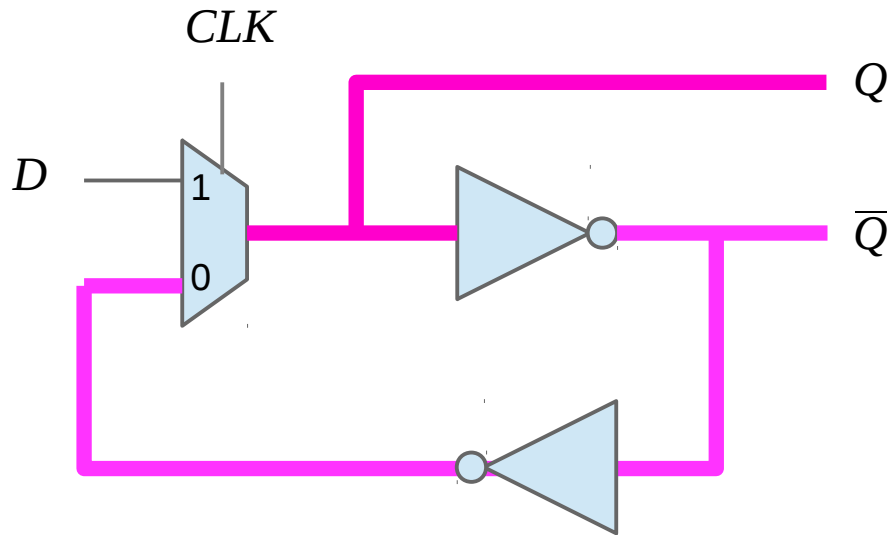
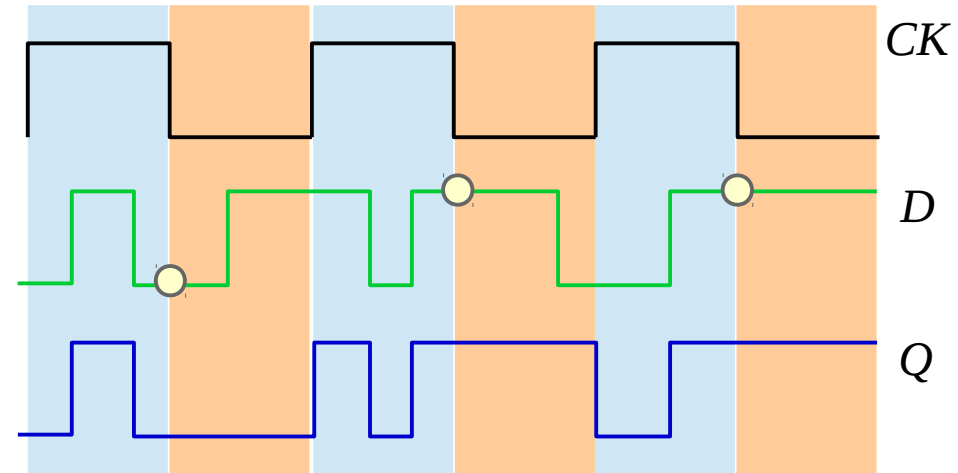
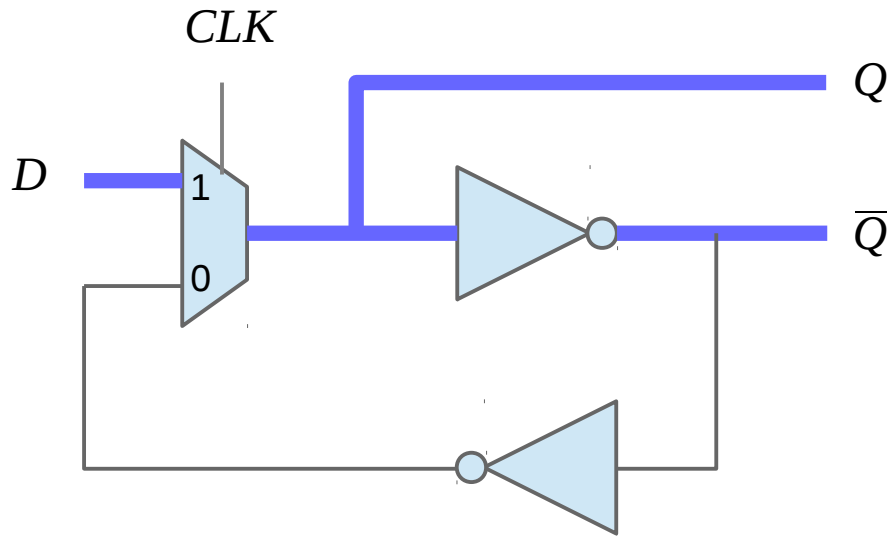
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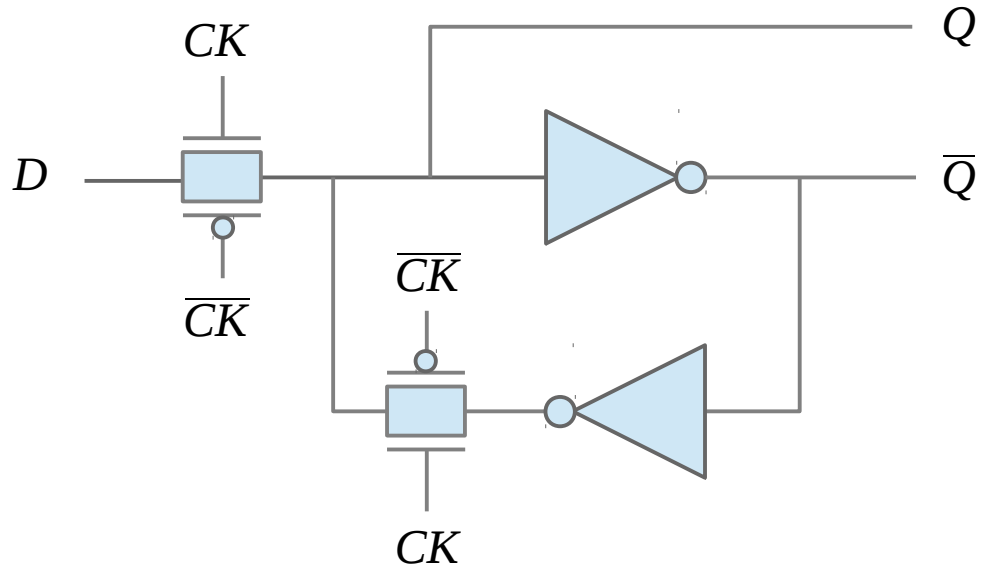
D Latch with Mux (1)



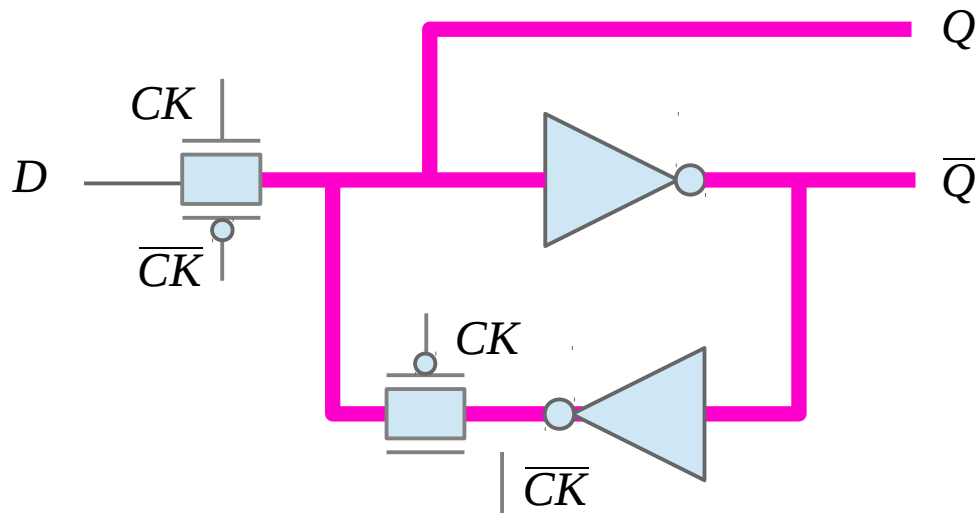
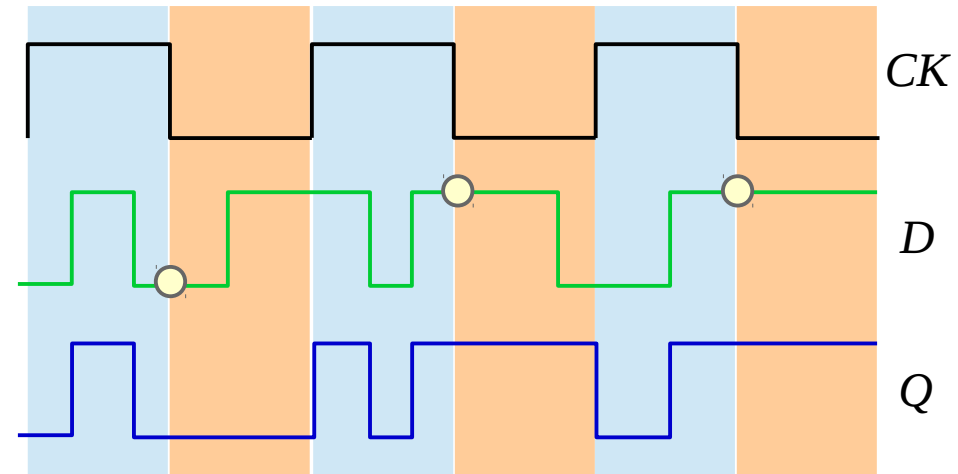
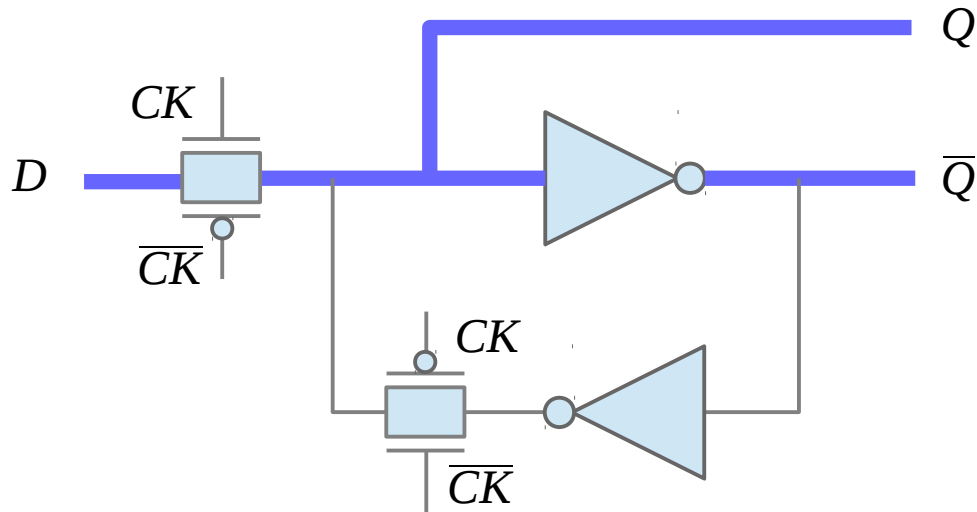
D Latch with Mux (2)



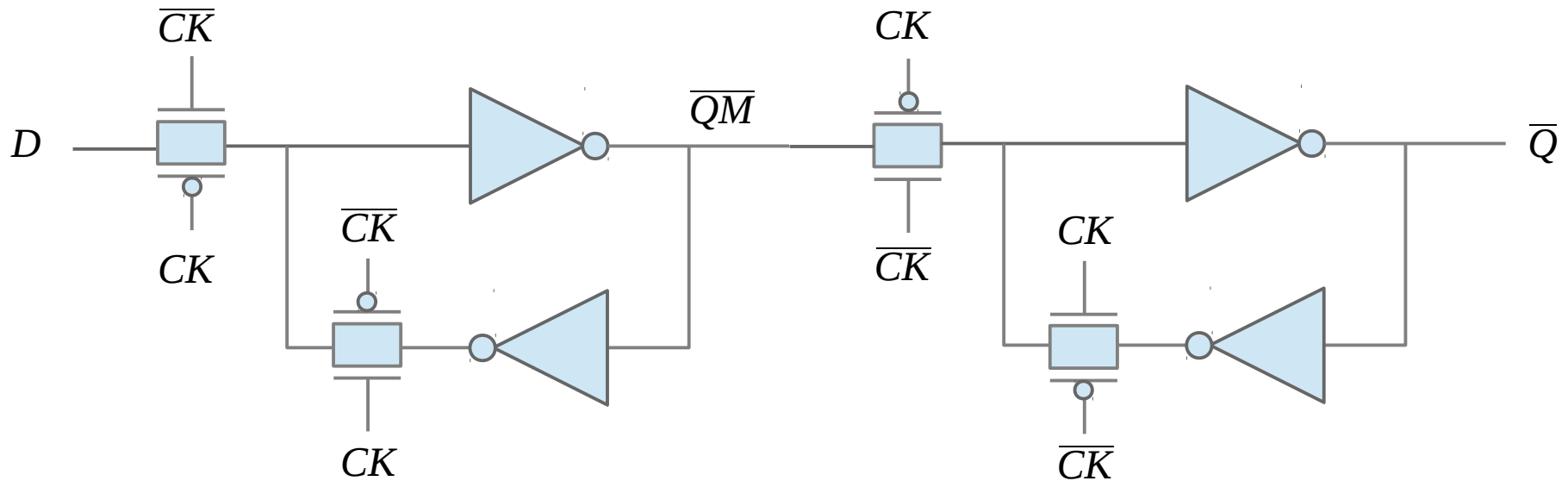
D Latch with Pass Gate (1)



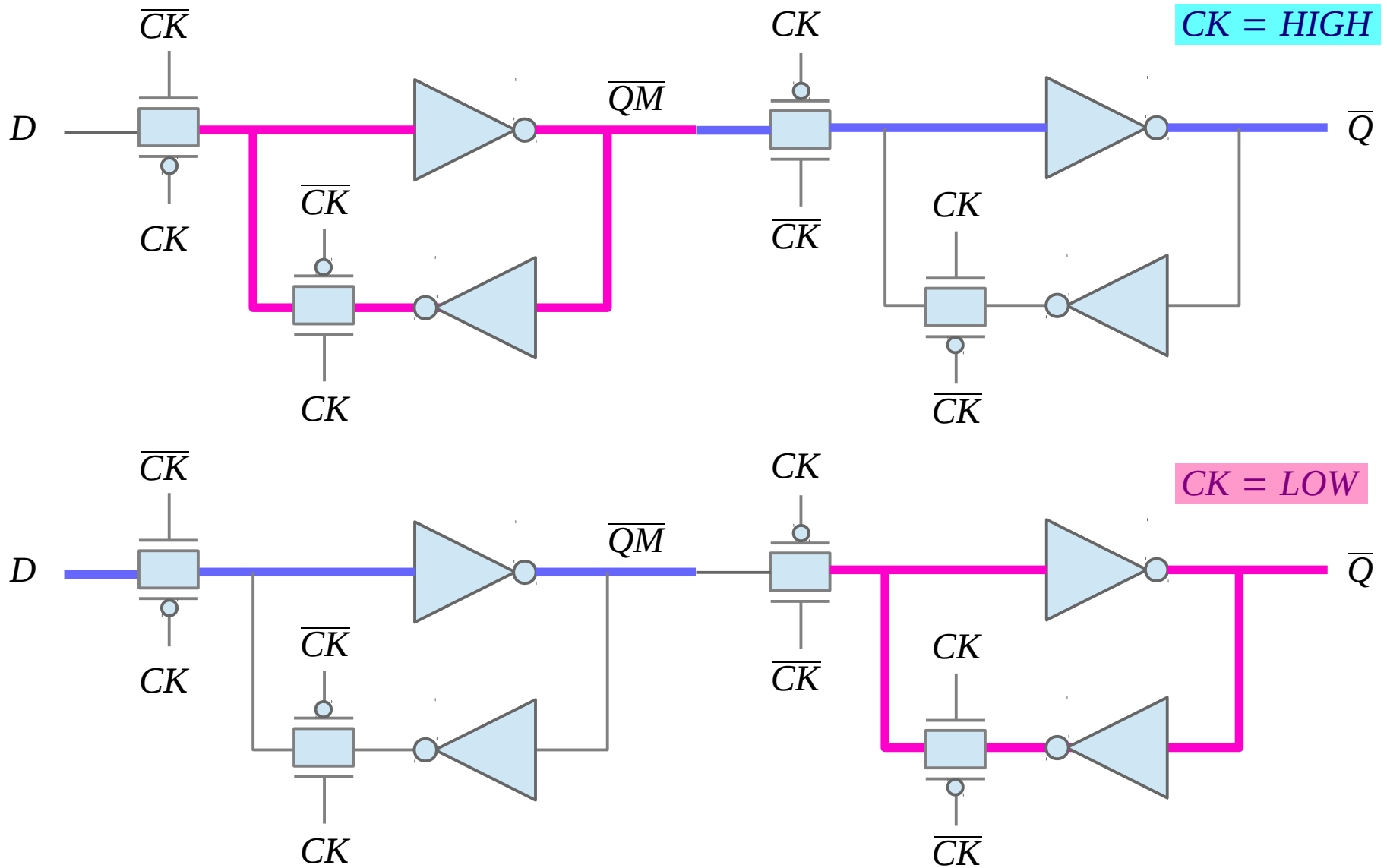
D Latch with Pass Gate (2)



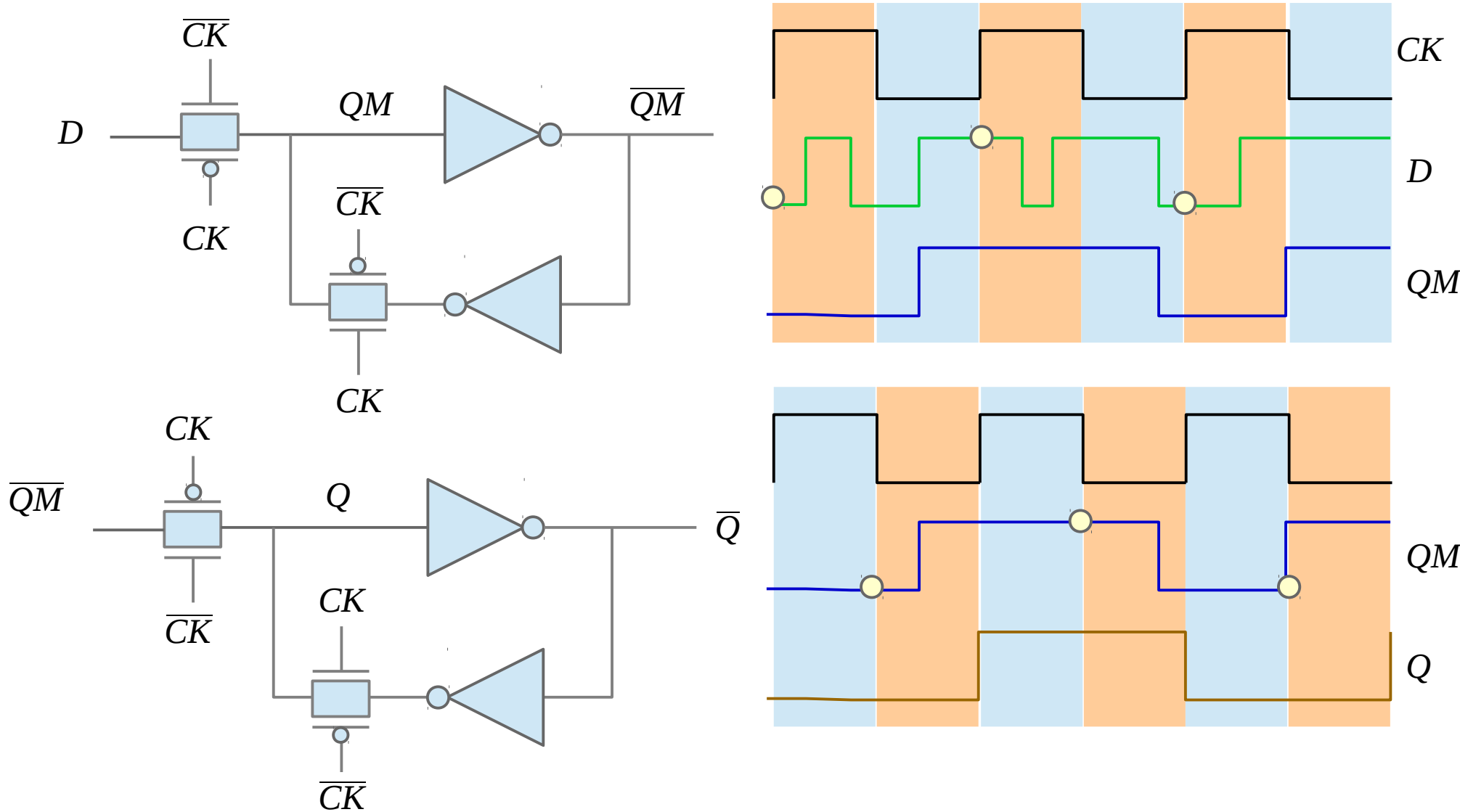
D Flip Flop with Pass Gate (1)



D Flip Flop with Pass Gate (1)



D Latch with Pass Gate (2)



Sequential Element Types

- CMOS Latches
- CMOS FlipFlops
- Pulsed Latches
- Latches and FlipFlops with a Reset
- Latches and FlipFlops with an Enable

References

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