

# BJT Amplifier Common Collector Amp (H.12)

20170630

Copyright (c) 2016 - 2017 Young W. Lim.

Permission is granted to copy, distribute and/or modify this document under the terms of the GNU Free Documentation License, Version 1.2 or any later version published by the Free Software Foundation; with no Invariant Sections, no Front-Cover Texts, and no Back-Cover Texts. A copy of the license is included in the section entitled "GNU Free Documentation License".

# References

Based

[1] Floyd, Electronic Devices 7th ed

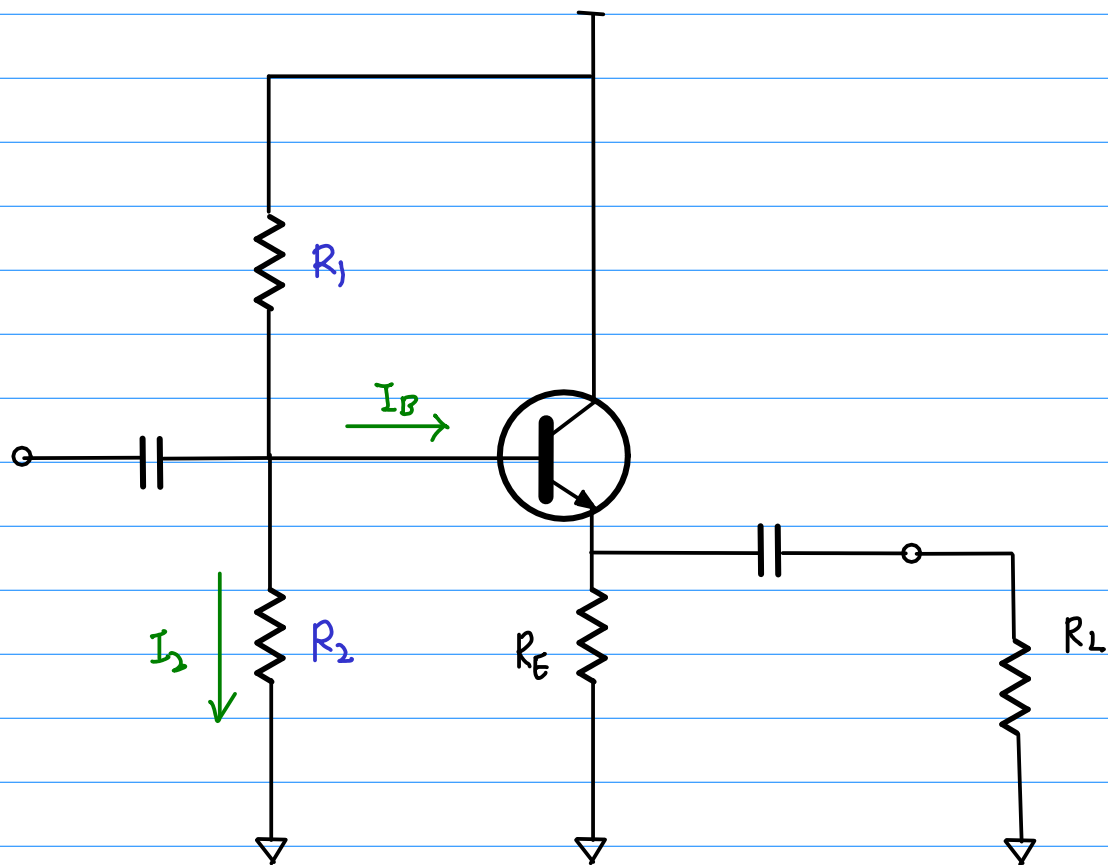
[2] Cook,

[2] [en.wikipedia.org](http://en.wikipedia.org)

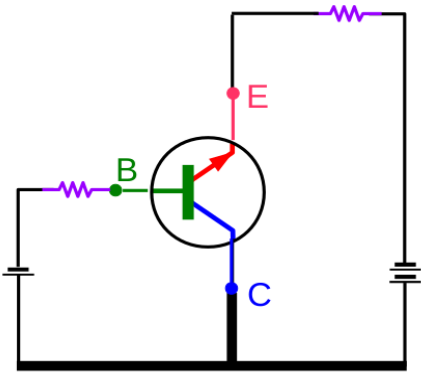
**Common Base****Common Emitter****Common Collector**

$Z_{in}$	CB : low $r_e \parallel R_E \approx r_e$	CE : med $R_1 \parallel R_2 \parallel \beta r_e$	CC : high $R_1 \parallel R_2 \parallel \beta(r_e + R_E)$
$Z_{out}$	CB : high $R_C$	CE : med $R_C$	CC : low $(r_e + \frac{R_s}{\beta}) \parallel R_E = \frac{R_s}{\beta} \parallel R_E$
$A_v$	CB : high $\frac{R_C}{r_e}, \frac{R_C \parallel R_L}{r_e}$	CE : med $\frac{R_C}{r_e}, \frac{R_C \parallel R_L}{r_e}$	CC : unity $\frac{R_E}{(r_e + R_E)} \approx 1$
$A_i$	CB : unity	CE : med	CC : high

**VDB**

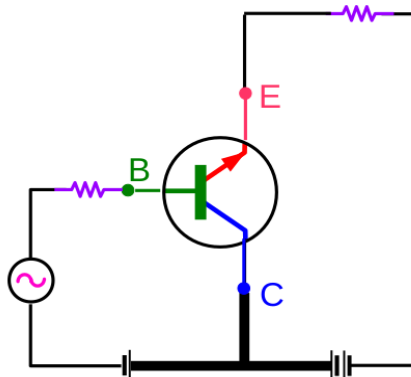


# Common Collector Configuration



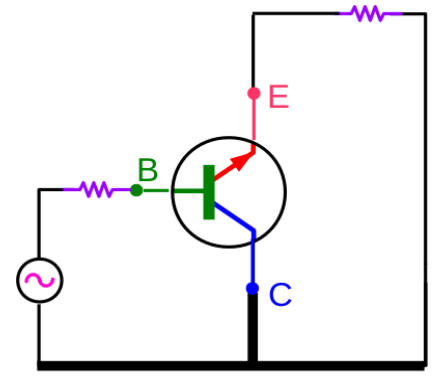
Common Collector

DC Bias



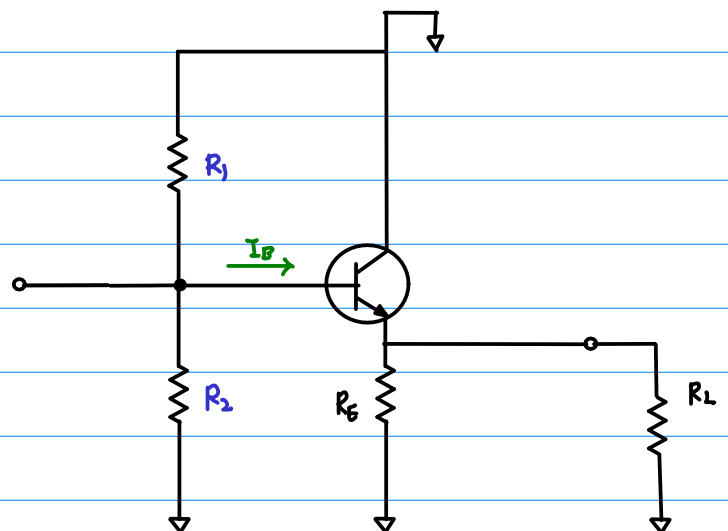
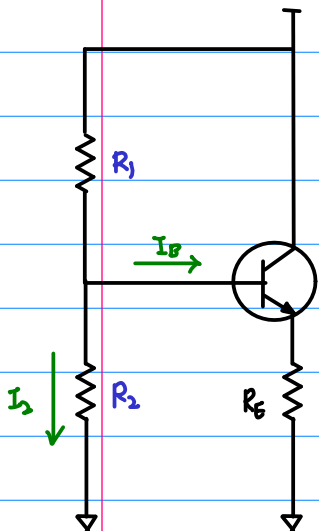
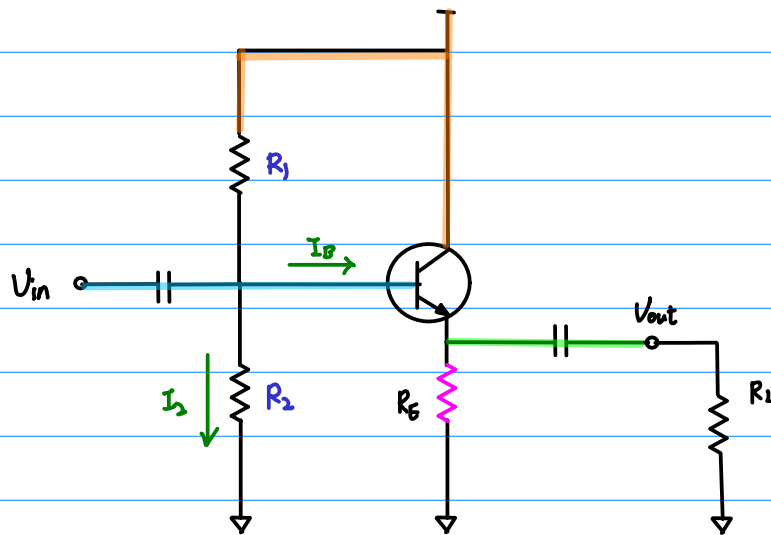
Common Collector

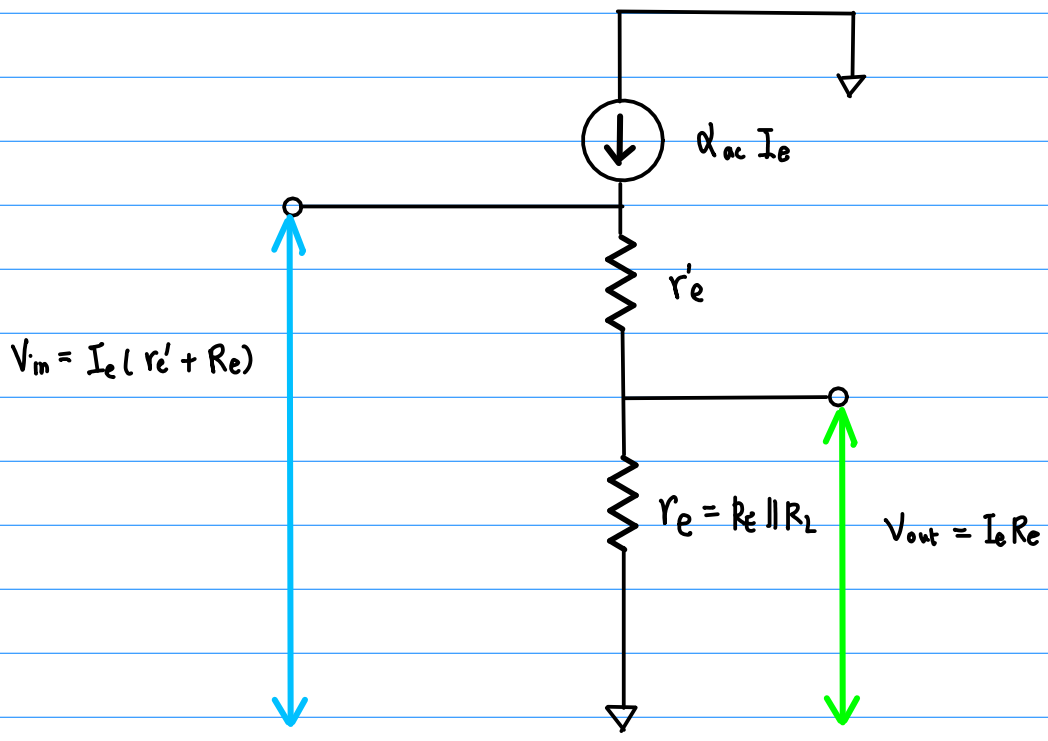
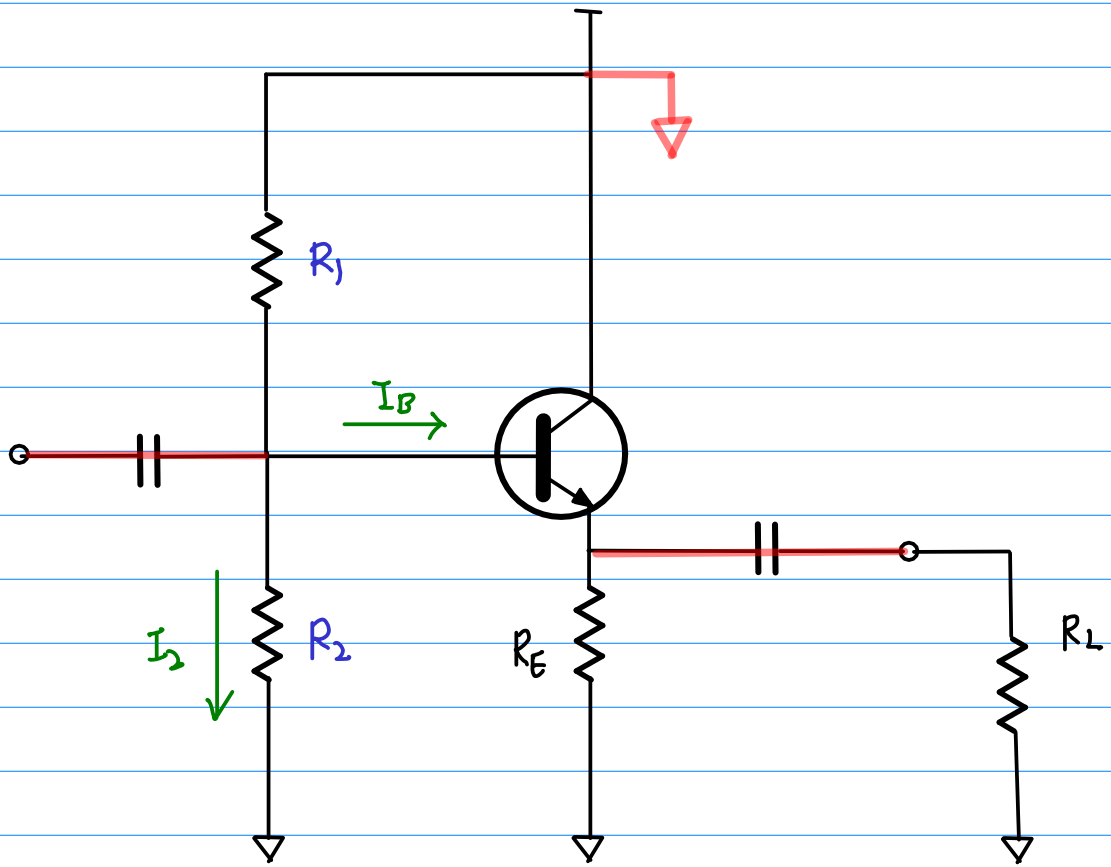
DC Bias + AC Signal



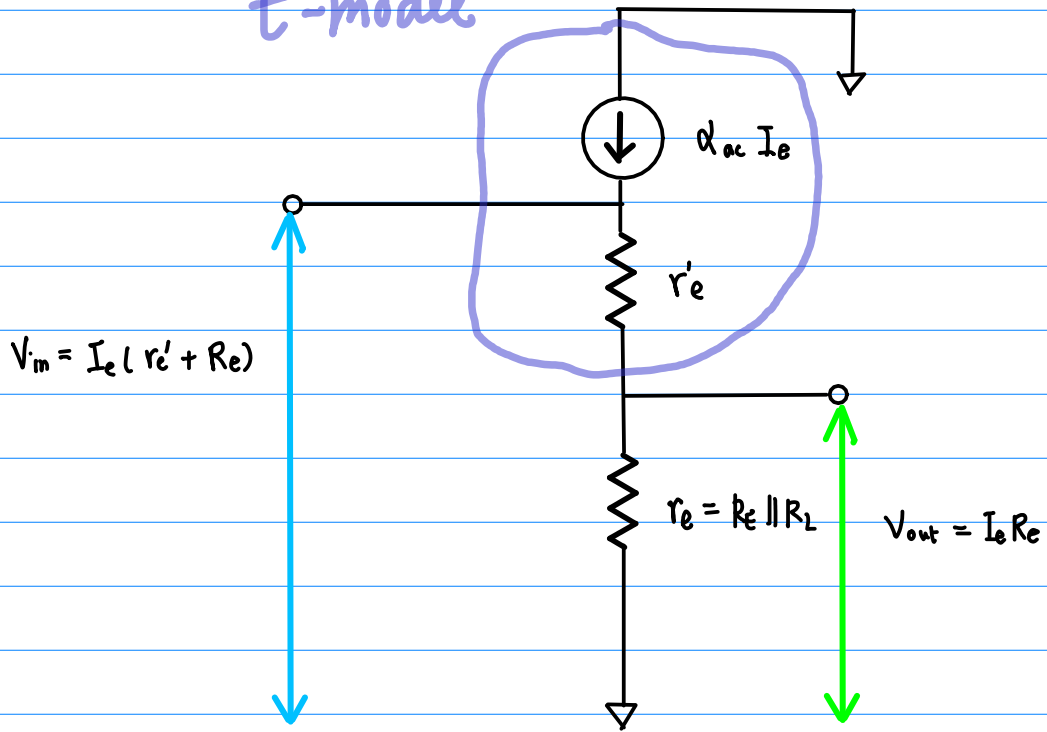
Common Collector

AC Signal

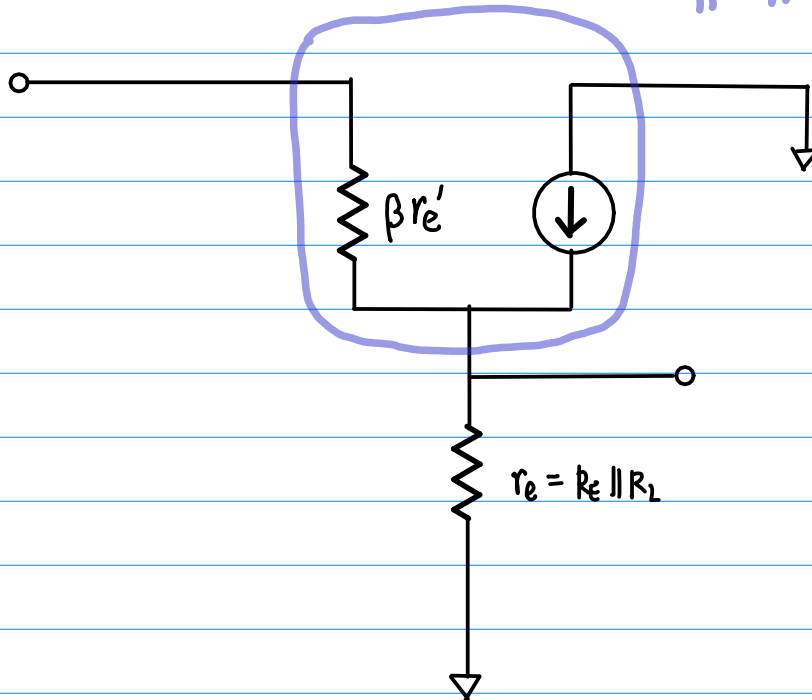


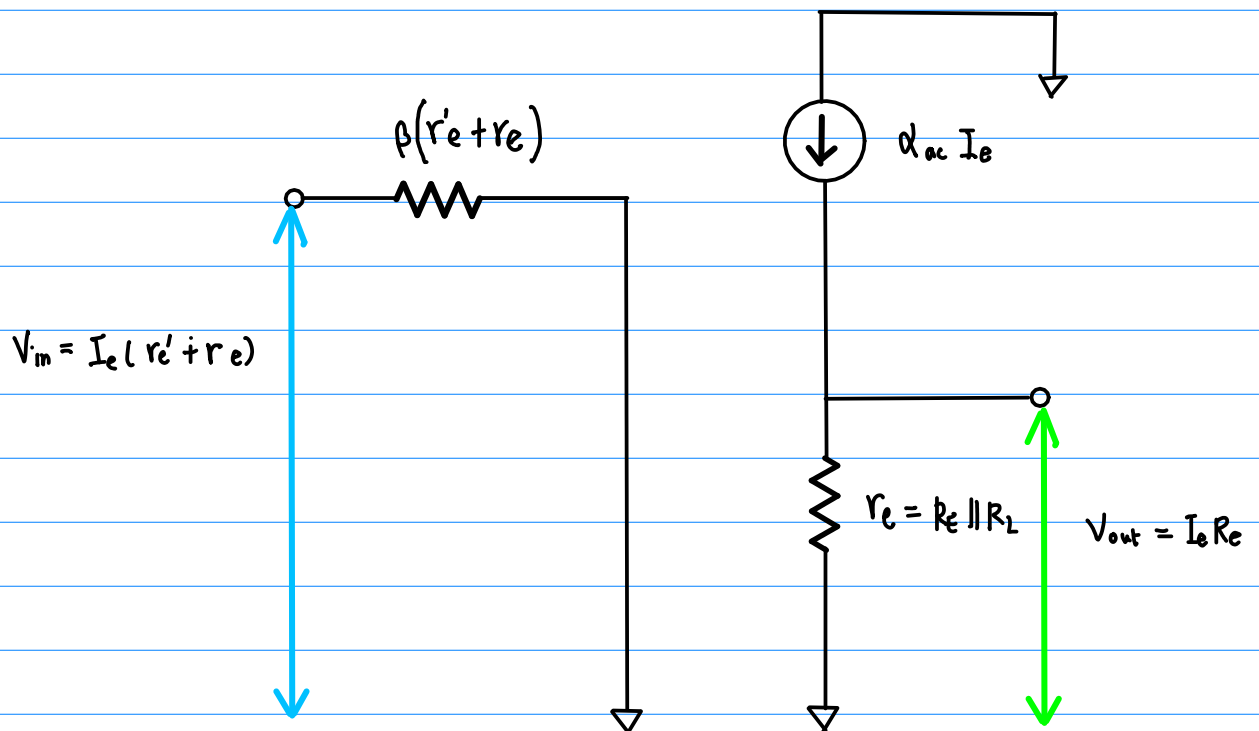
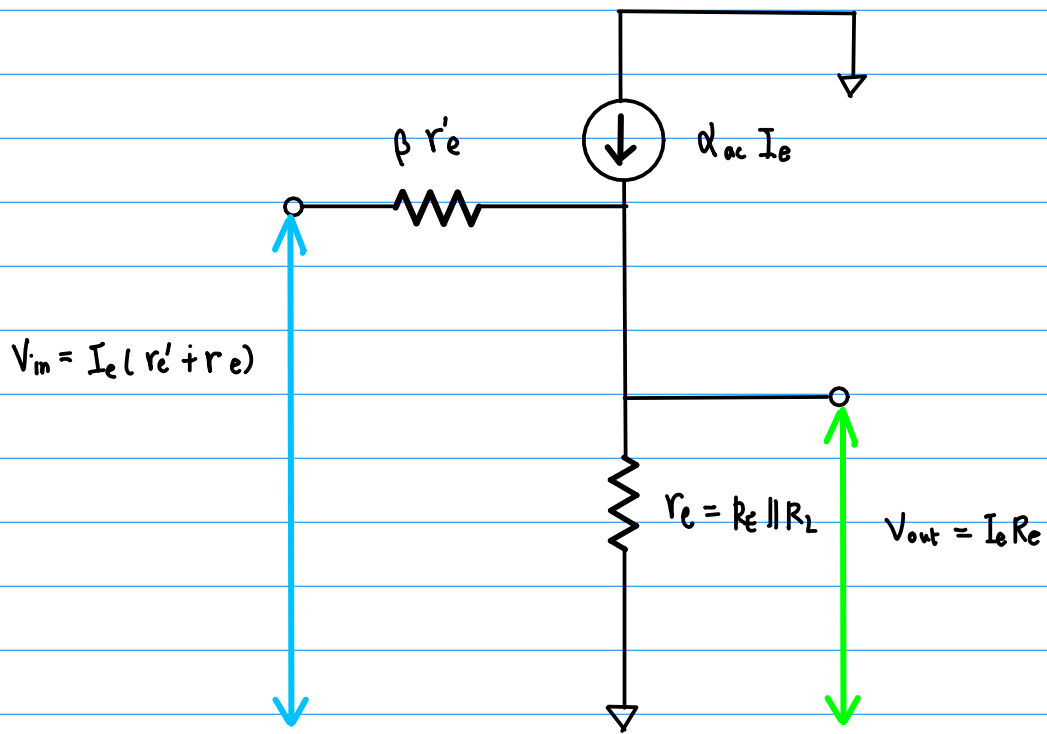


t-model



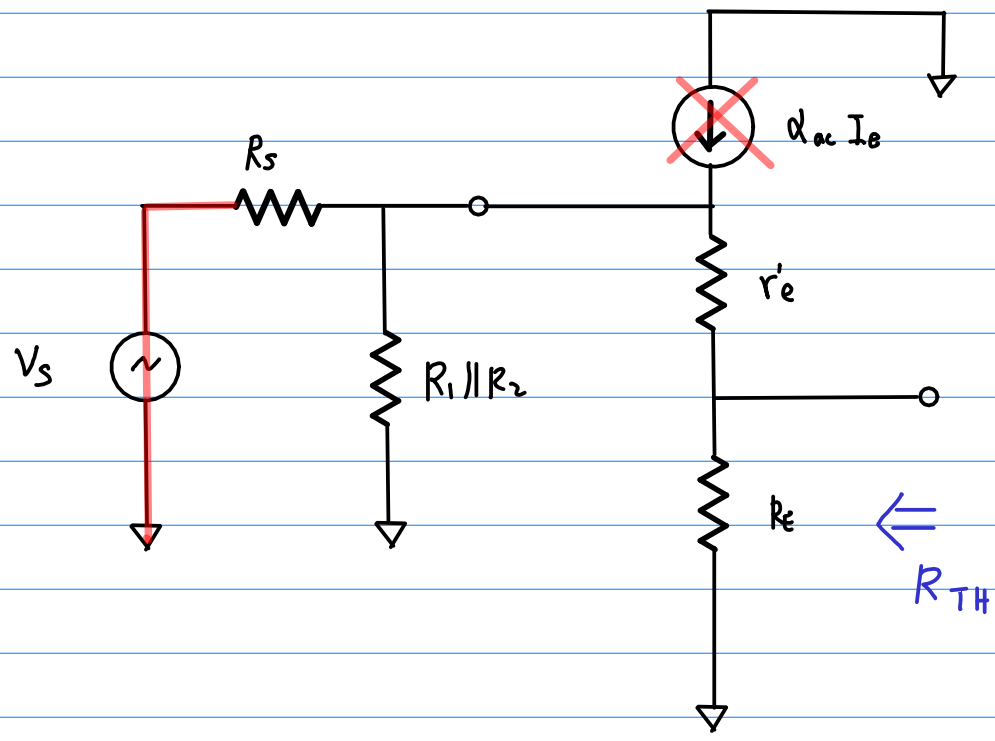
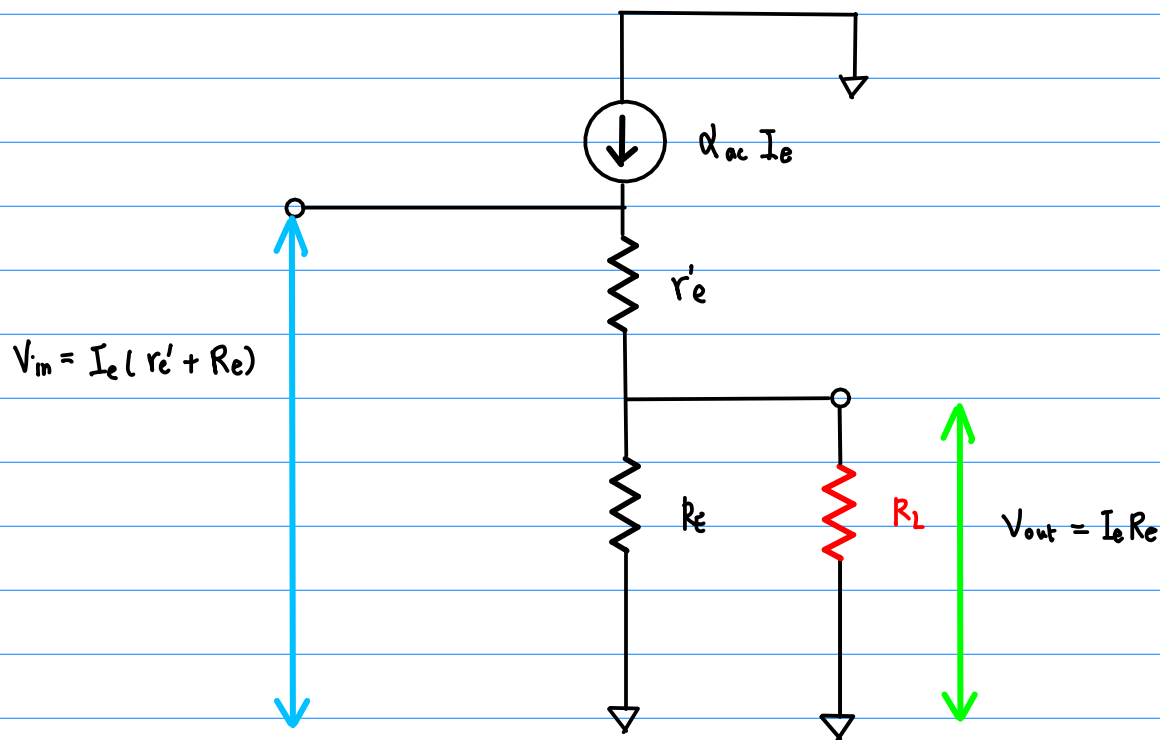
$\pi$ -model

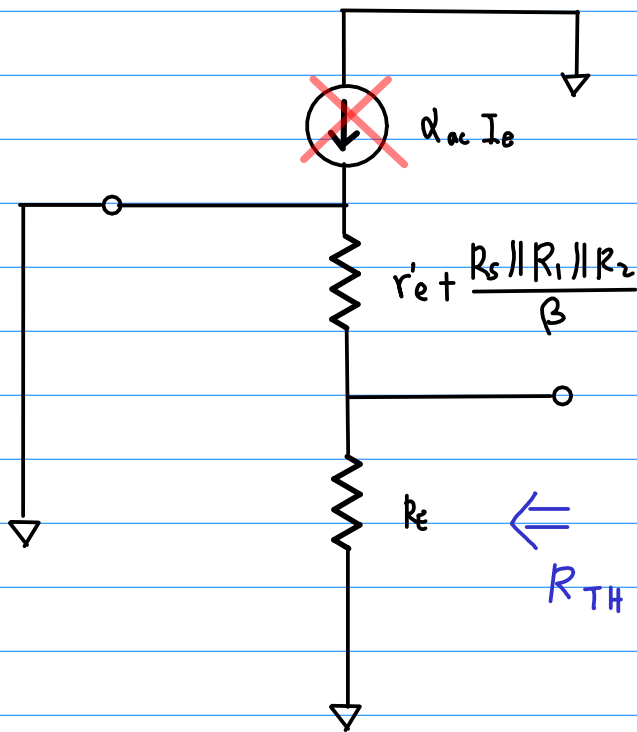
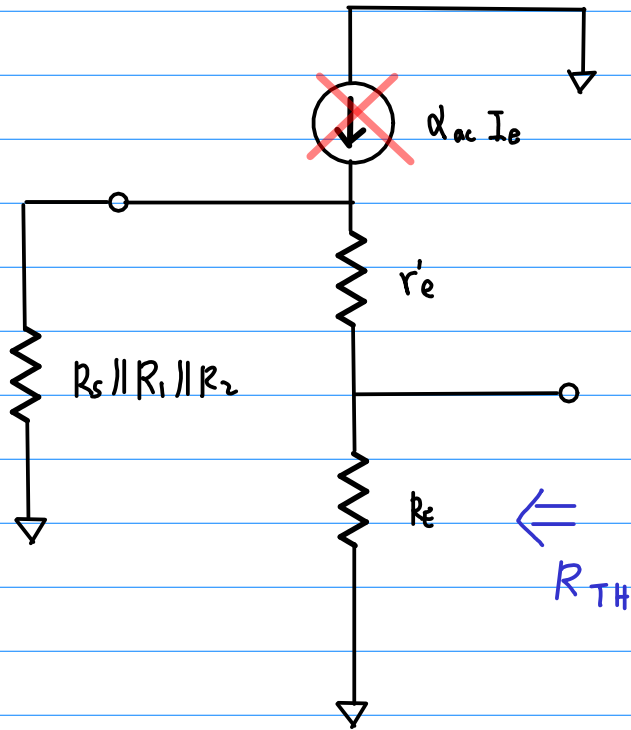




$$Z_{in}(\text{base}) = \beta (r'_e + r_e)$$







$$Z_{out} = R_E \parallel \left( r_e + \frac{R_s \parallel R_1 \parallel R_2}{\beta} \right)$$

# $A_v$

$$V_{out} = I_e R_e$$

$$V_{in} = I_e (r_e' + R_c)$$

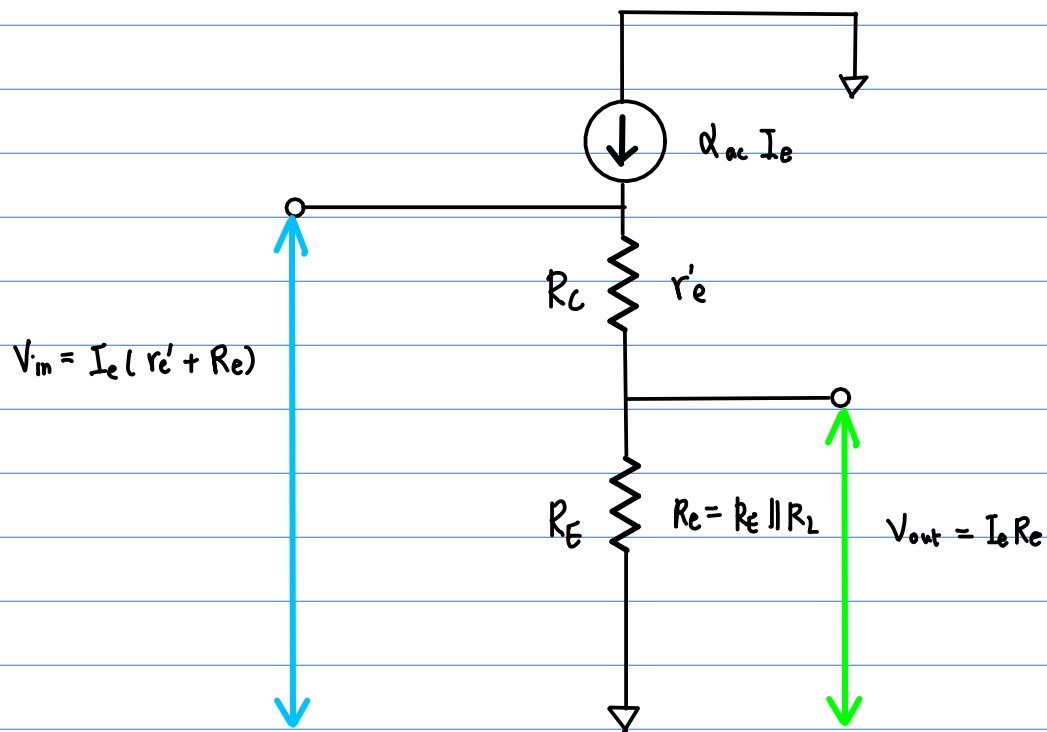
$$A_v = \frac{I_e R_e}{I_e (r_e' + R_c)} = \frac{R_e}{(r_e' + R_c)}$$

$$R_e = R_E \parallel R_L$$

$$R_e = R_E \quad \text{no load}$$

$A_v < 1$  always

$$\text{if } R_c \gg r_e' \Rightarrow A_v = 1$$



$Z_i$

$$R_{in(base)} = \frac{V_{in}}{I_{in}} = \frac{V_b}{I_b} = \frac{I_e(r_e' + R_e)}{I_b} = \frac{\beta I_b (r_e' + R_e)}{I_b}$$

$$R_{in(base)} = \beta (r_e' + R_e)$$

$$R_e \gg r_e'$$

$$R_{in(base)} = \beta R_e$$

$$R_{in(total)} = R_1 \parallel R_2 \parallel R_{in(base)} = R_1 \parallel R_2 \parallel \beta R_e$$

$A_i$

$$I_{in} = \frac{V_{in}}{R_{in(total)}}$$

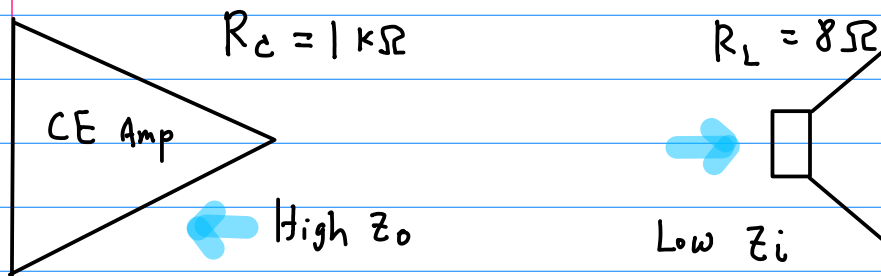
$$A_i = \frac{I_e}{I_{in}}$$

$$R_1, R_2 \gg R_{in(base)}$$

$$R_1 \parallel R_2 \gg \beta R_e$$

$$A_i = \frac{I_e}{I_{in}} = \beta$$

# Driving Low Resistance Load



$$R_c = R_c \parallel R_L = 1000 \parallel 8 = 7.94 \Omega$$

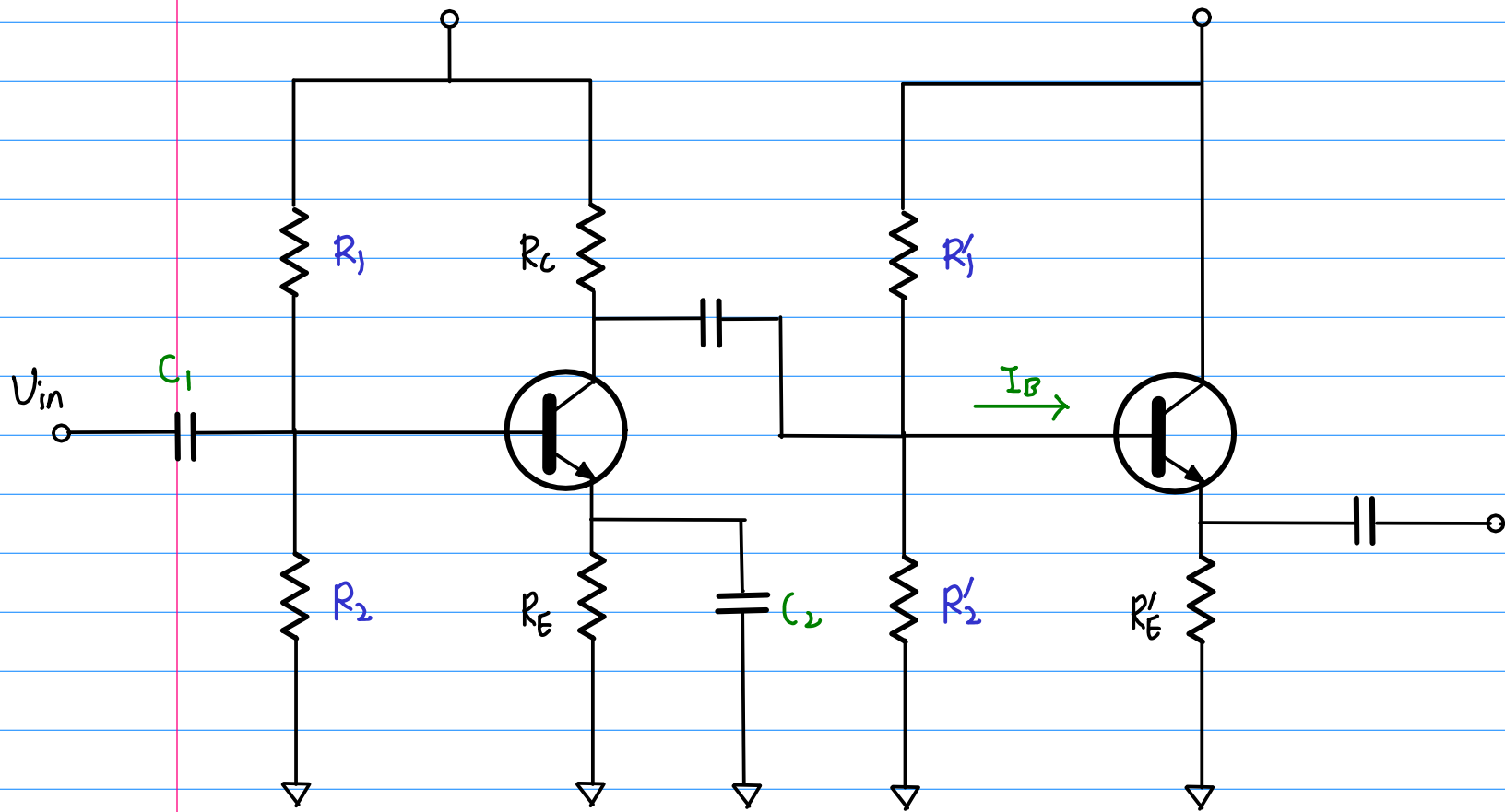
$$A_v = \frac{R_c}{r_{e'}} = \frac{1000}{5} = 200 \quad \text{without load}$$

$$A_v = \frac{R_c}{r_{e'}} = \frac{7.94}{5} = 1.59 \quad \text{with } 8 \Omega \text{ load}$$

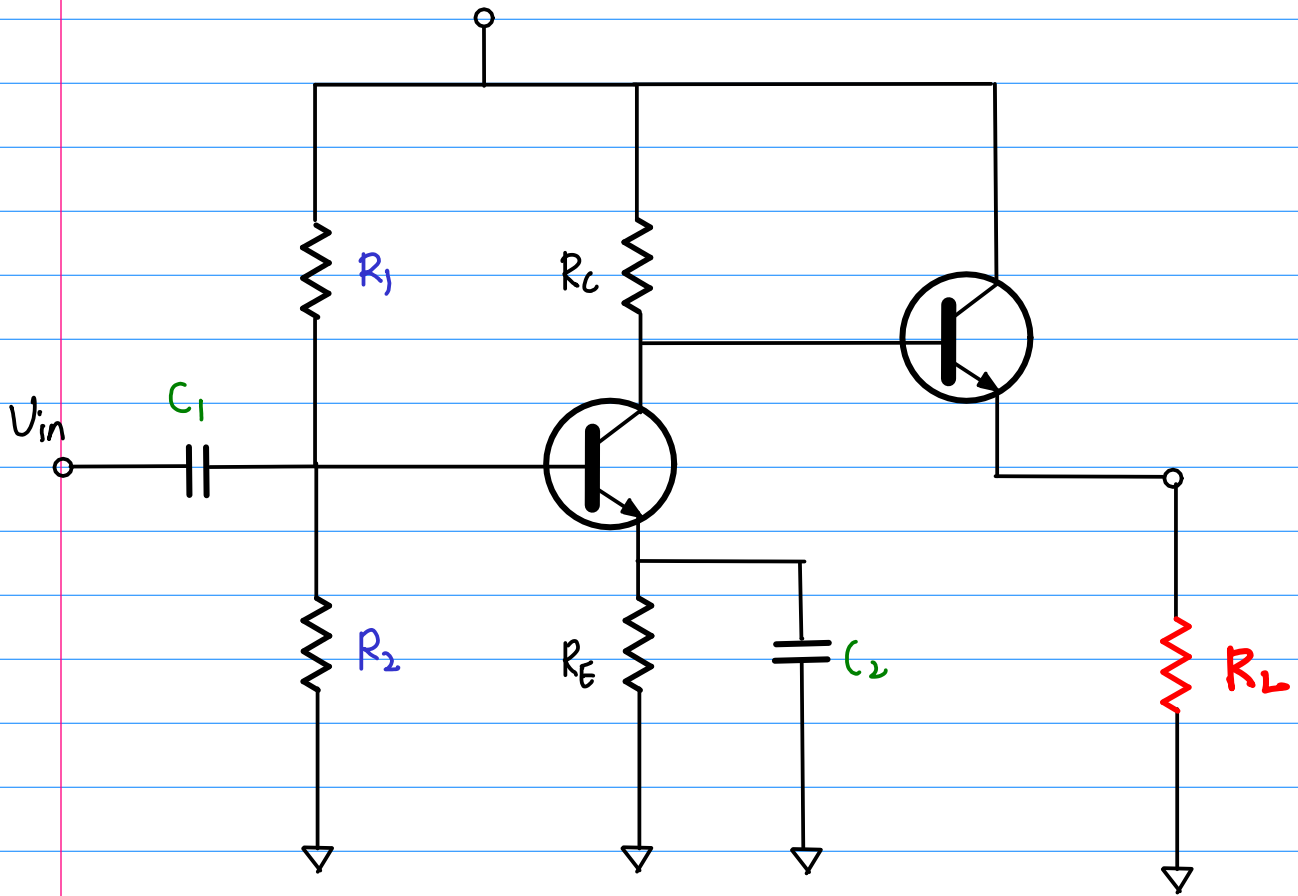
Darlington pair  
interface (buffer)

high output resistance & low resistance load

# CE + CC

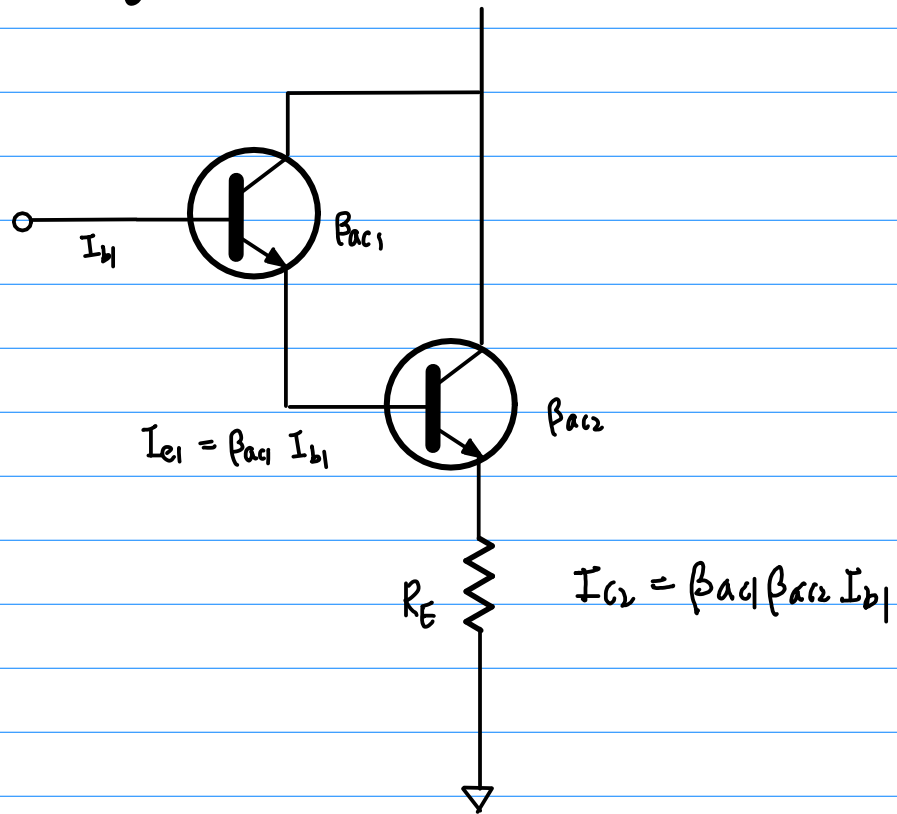


# Direct Coupled Output Stage





# The Darlington Pair



$$\beta_{ac} = \beta_{ac1} \cdot \beta_{ac2}$$

★  $R_{in} = \beta_{ac1} \beta_{ac2} R_E \rightarrow$  high input resistance



