

CMOS Delay-7 (H.8) Delay Model

20170209

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References

Some Figures from the following sites

[1] <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>
Weste & Harris Book Site

[2] en.wikipedia.org

β : Device Transconductance Parameter

k : Process Transconductance Parameter

μ : Electron / Hole Mobility

$$\text{PMOS} \quad \beta_p = k'_p \left(\frac{W}{L}\right)_p \quad k'_p = \mu_p C_{ox} \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$\text{nMOS} \quad \beta_n = k'_n \left(\frac{W}{L}\right)_n \quad k'_n = \mu_n C_{ox} \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$\text{PMOS} \quad \beta_p = \mu_p \frac{\epsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right)_p$$

$$\text{nMOS} \quad \beta_n = \mu_n \frac{\epsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right)_n$$

Saturation Current

$$I_{d_p} = \frac{\beta_p}{2} (V_{GS_n} - |V_{TP}|)^2 \quad V_{TP} < 0$$

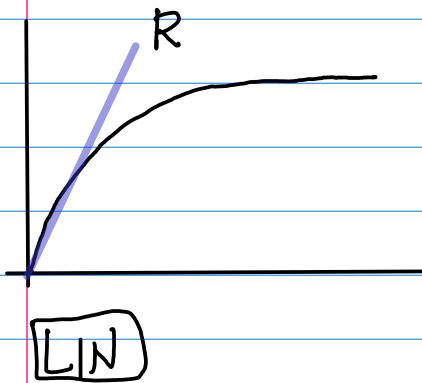
$$I_{d_n} = \frac{\beta_n}{2} (V_{GS_n} - V_{TN})^2 \quad V_{TN} > 0$$

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$

$$\frac{k'_n}{k'_p} = 2 \sim 3$$

$$\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = \gamma$$

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$



$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

$$R_p = \frac{1}{\beta_p (V_{DD} - V_{Tp})}$$

fall time t_f $\tau_n = R_n C_{out}$

rise time t_r $\tau_p = R_p C_{out}$

$$C_{out} = C_{para} + C_L$$

fall time	$t_f = 2.2 \tau_n = \ln 9 \tau_n$	$0.9 V_{DD} \rightarrow 0.1 V_{DD}$
rise time	$t_r = 2.2 \tau_p = \ln 9 \tau_p$	$0.1 V_{DD} \rightarrow 0.9 V_{DD}$
propagation delay time	$t_p = \frac{1}{2} (t_{pf} + t_{pr})$ $= 0.35 (t_{pf} + t_{pr})$	$0.5 V_{DD} \rightarrow 0.5 V_{DD}$
propagation fall time	$t_{pf} = 0.7 \tau_n = \ln 2 \tau_n$	$V_{DD} \rightarrow 0.5 V_{DD}$
propagation rise time	$t_{pr} = 0.7 \tau_p = \ln 2 \tau_p$	$0 \rightarrow 0.5 V_{DD}$

$$\tau_n = R_n (C_{para} + C_L)$$

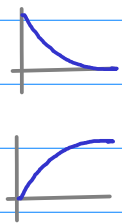
$$\tau_p = R_p (C_{para} + C_L)$$

$$C_{out} = C_{para} + C_L$$

$$\left(\frac{W}{L}\right)_p = r \left(\frac{W}{L}\right)_n$$

$$r = \frac{\mu_n}{\mu_p} = \frac{k'_n}{k'_p} > 1$$

$$R_n = R_p = R = \frac{1}{\beta(V_{DD} - V_T)}$$

$$\begin{cases} V_{out}(t) = V_{DD} (1 - e^{-t/\tau}) \\ V_{out}(t) = V_{DD} e^{-t/\tau} \end{cases}$$


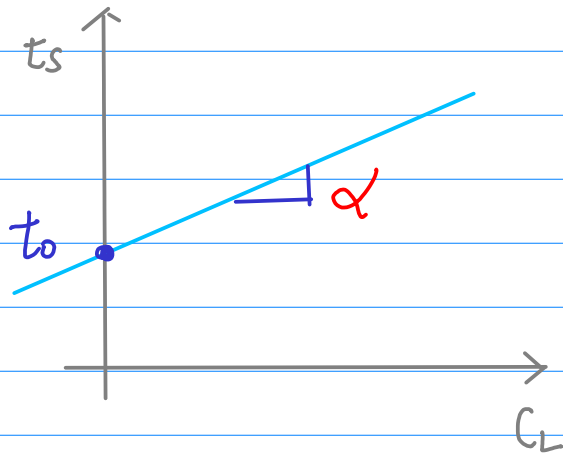
$$\tau = RC_{out} = R(C_{par} + C_L)$$

Generic Switching Delay

$$t_s = t_0 + \alpha C_L \Rightarrow t_s = t_r = t_f$$

Generic Switching Delay

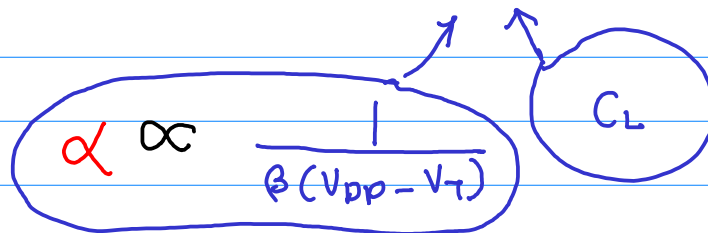
$$t_s = t_0 + \alpha C_L$$

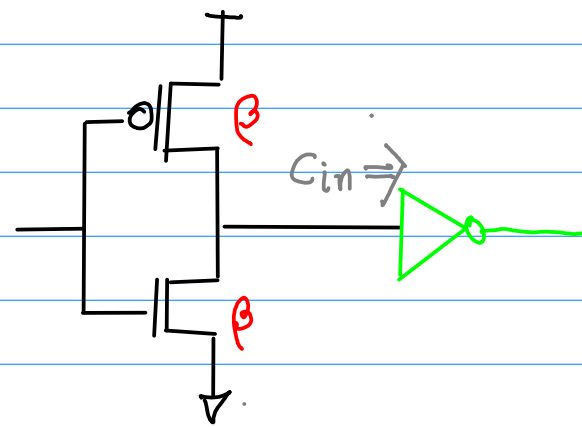
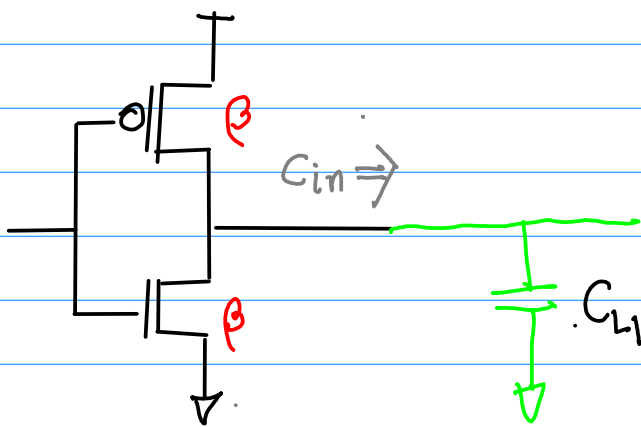
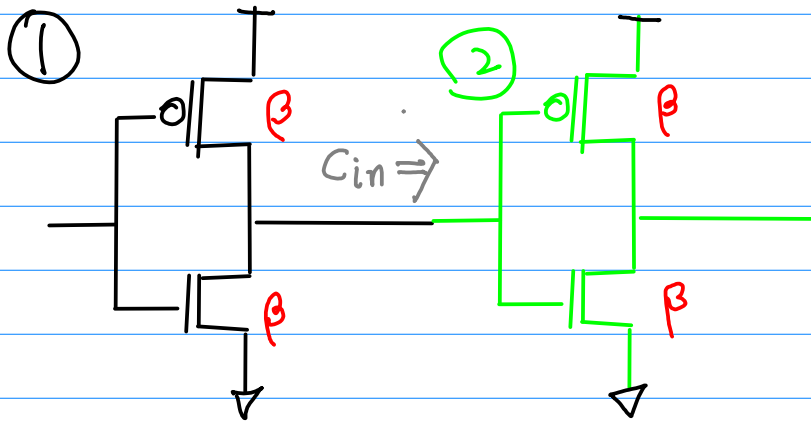


t_0 : zero delay

α : slope

$$\tau \approx RC$$





reference case

$$C_{in} = C_L$$

Generic Switching Delay of ①

$$t_{s1} = t_0 + \alpha C_L$$

$$= t_0 + \alpha C_{in}$$

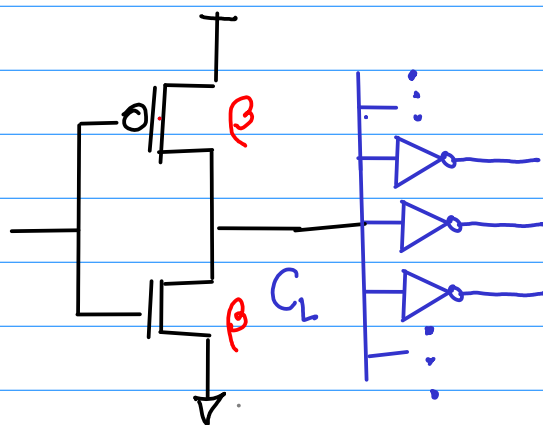
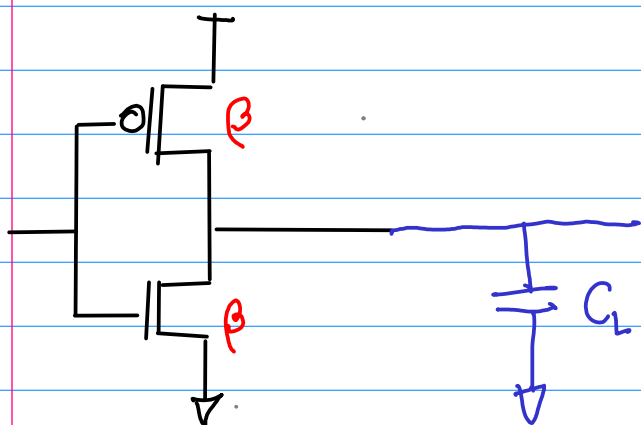
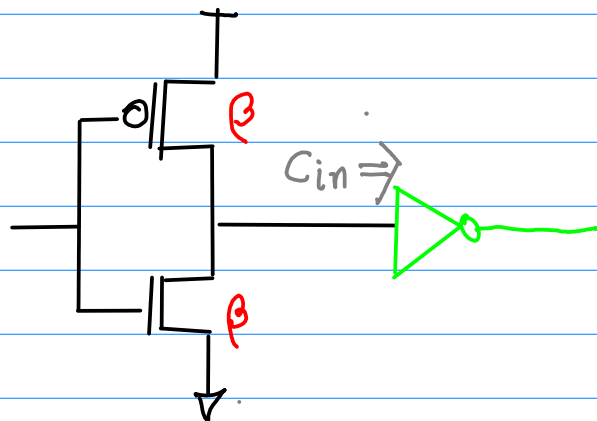
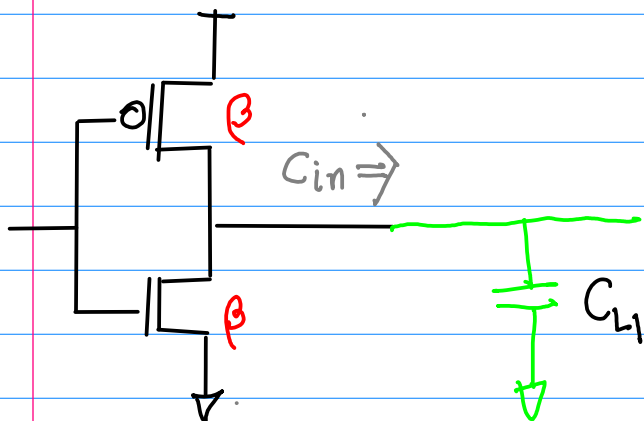
$$\begin{aligned}C_{in} &= C_{gn} + C_{gp} \\ &= C_{ox} (A_{gn} + A_{gp})\end{aligned}$$

A_i : gate area

the channel length L assumed

$$\begin{aligned}C_{in} &= C_{ox} L (W_n + W_p) \\ &= C_{ox} L (W_n + r W_p) \\ &= C_{ox} L W_n \cdot (1 + r) \\ &= C_{gn} (1 + r)\end{aligned}$$

When $C_L \gg C_{in}$



to minimize t_s

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area tradeoff

$$t_s = t_0 + \alpha C_L \quad t \approx RC$$

$$\alpha \propto \frac{1}{\beta(V_{DD} - V_T)}$$

Diagram showing the relationship between α and C_L . The expression $\alpha \propto \frac{1}{\beta(V_{DD} - V_T)}$ is circled in blue. An arrow points from this expression to the α term in the equation above. Another arrow points from a circled C_L to the C_L term in the equation above.

to minimize t_s

$$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow \text{bigger size}$$

Speed v.s. area tradeoff

Scaling Factor S

$$\beta' = S \beta$$

$$R' = \frac{R}{S}$$

$$\alpha' = \frac{\alpha}{S^2}$$

$$t_s = t_0 + \left(\frac{\alpha}{S} \right) C_L$$

Compensation Factor $\left(\frac{1}{S} \right)$

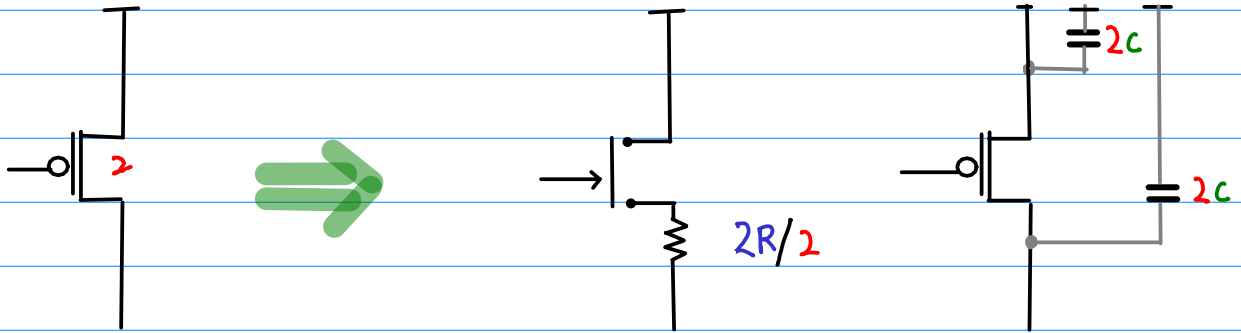
enables a NOT gate drive larger values of C_L

If $C_L = S C_{in}$ (increased by the scaling factor S)

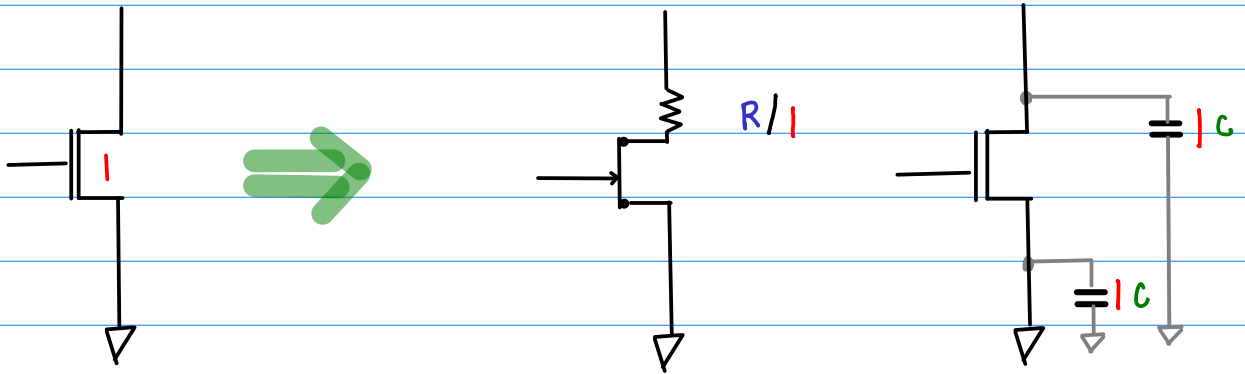
then the switching time is the same

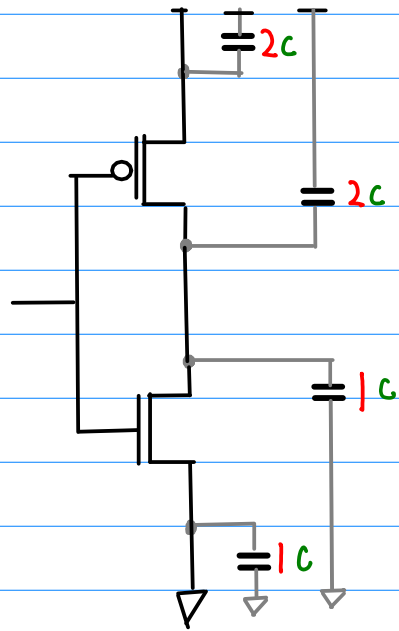
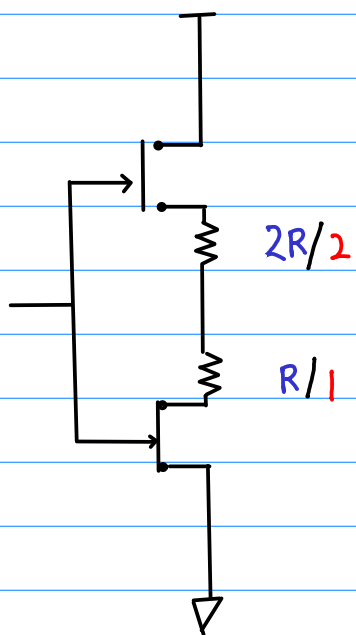
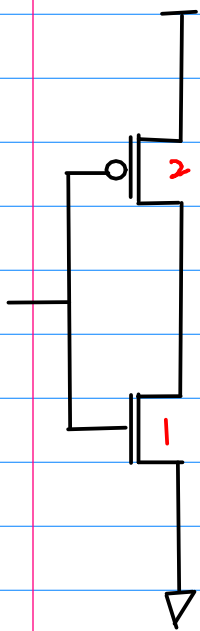
RC Delay Model

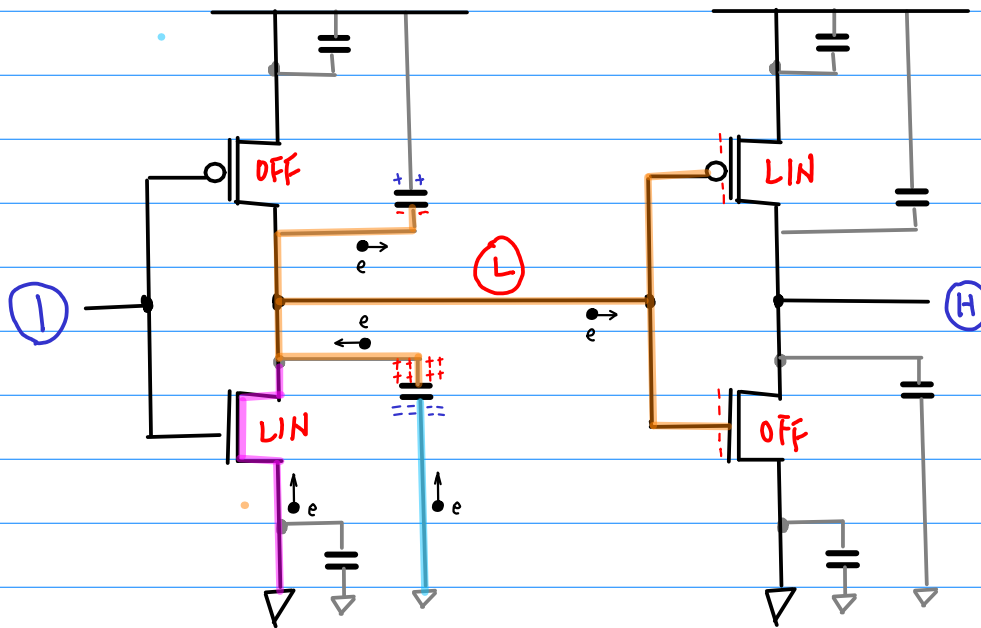
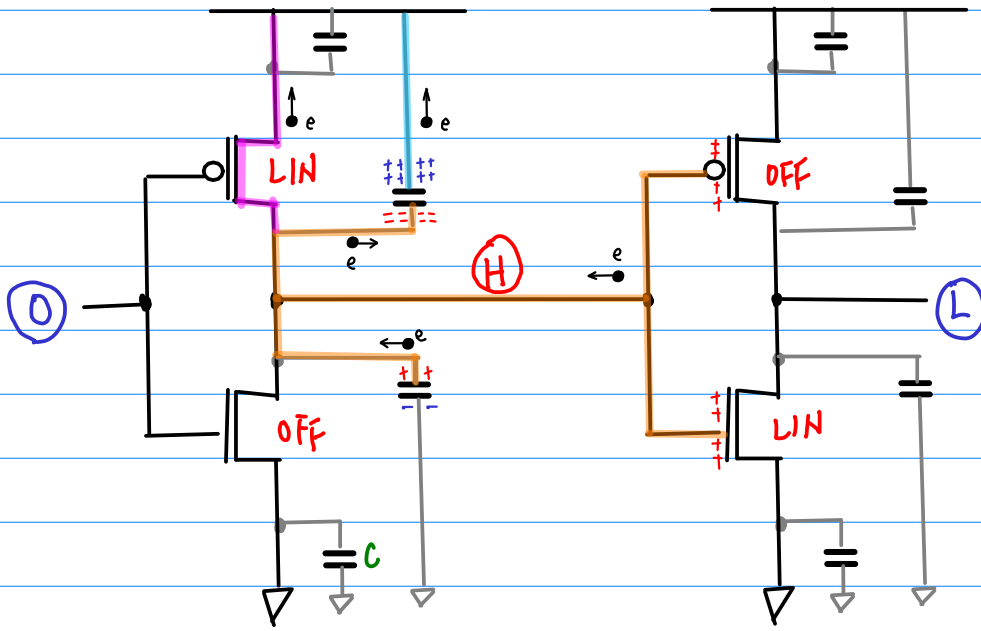
pMOS

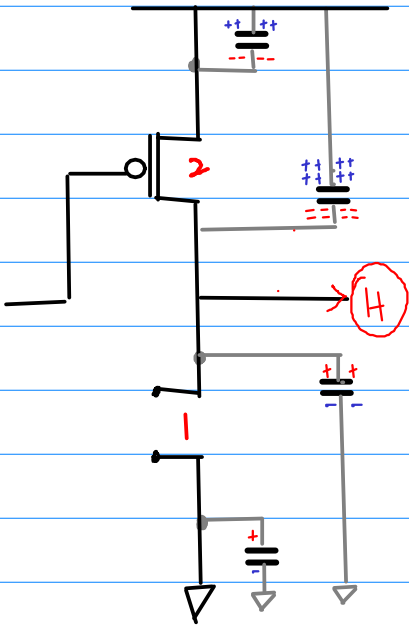


nMOS



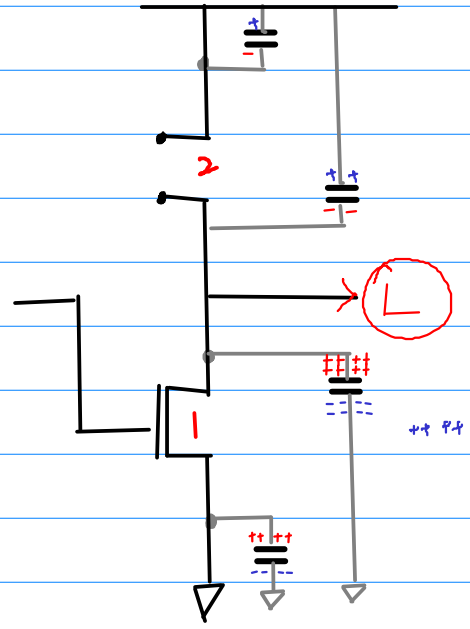


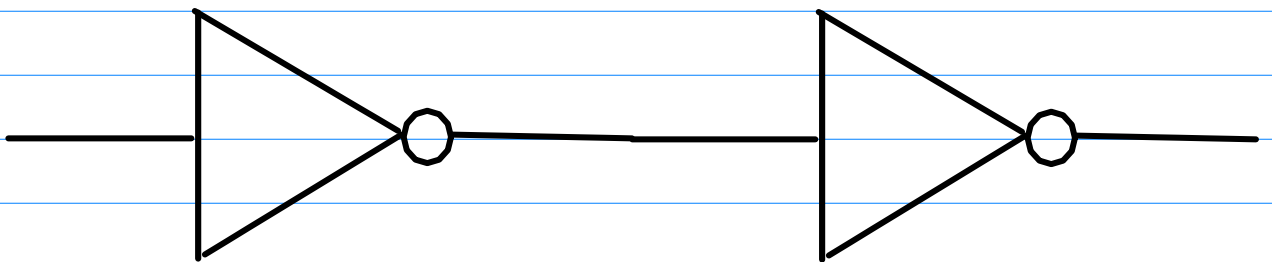
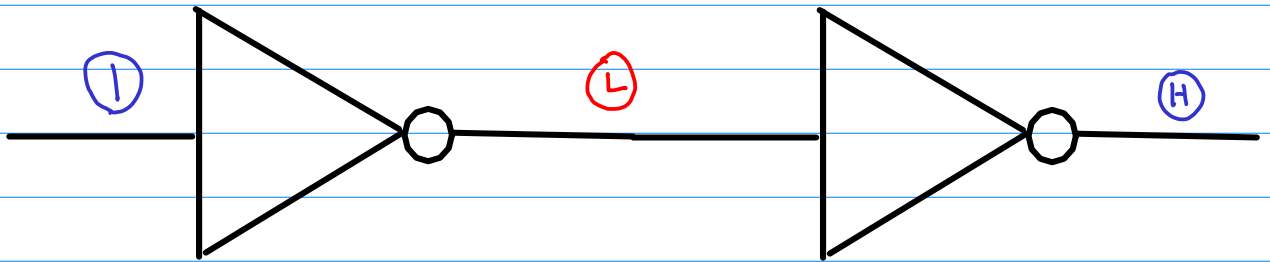
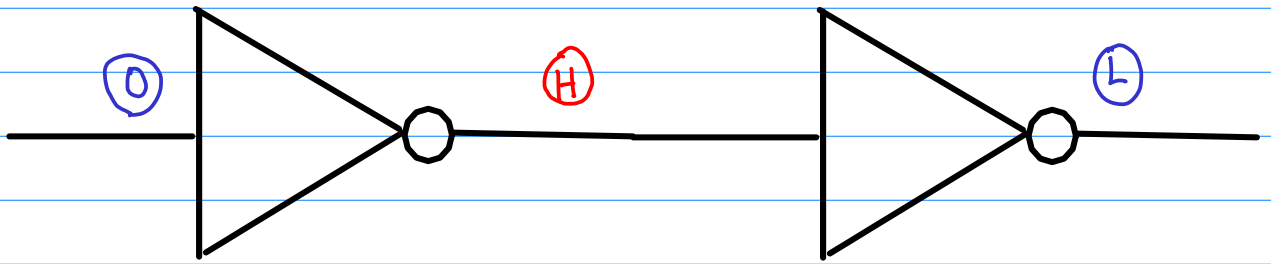


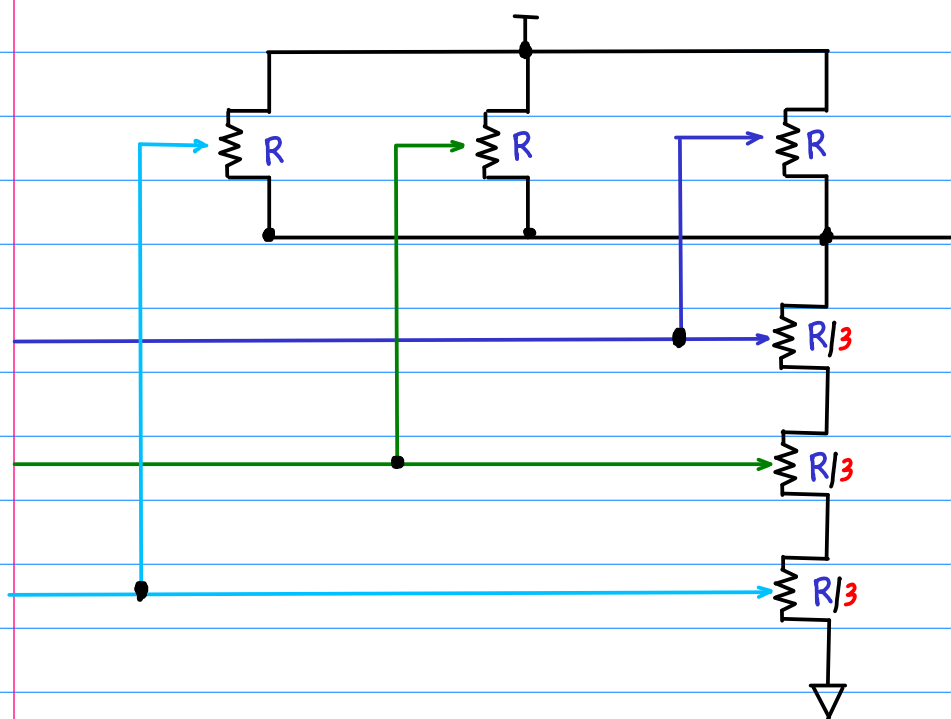
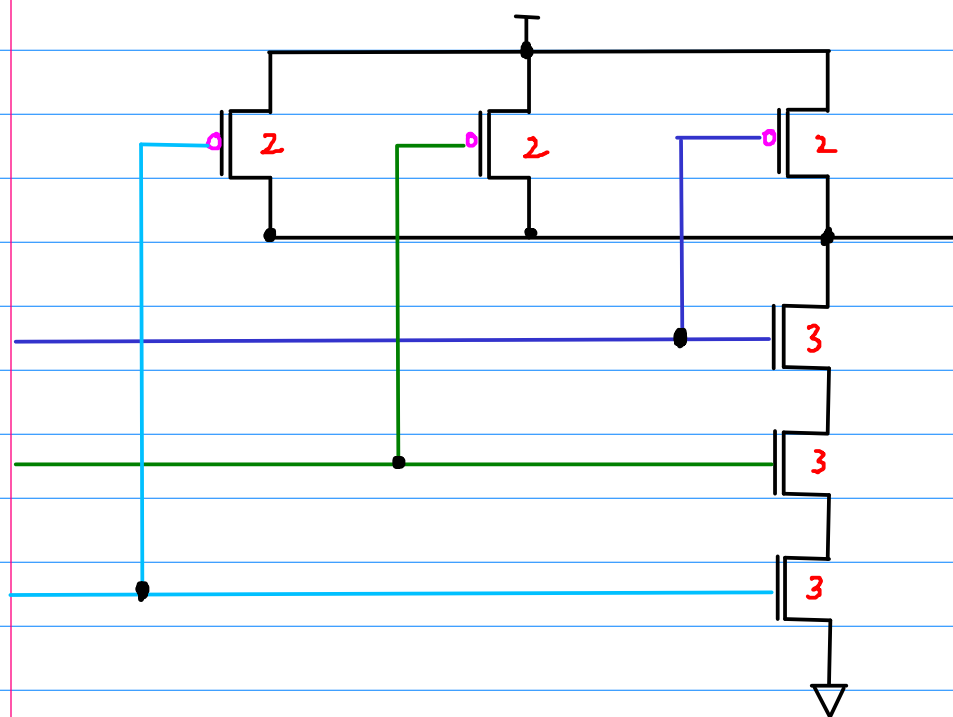


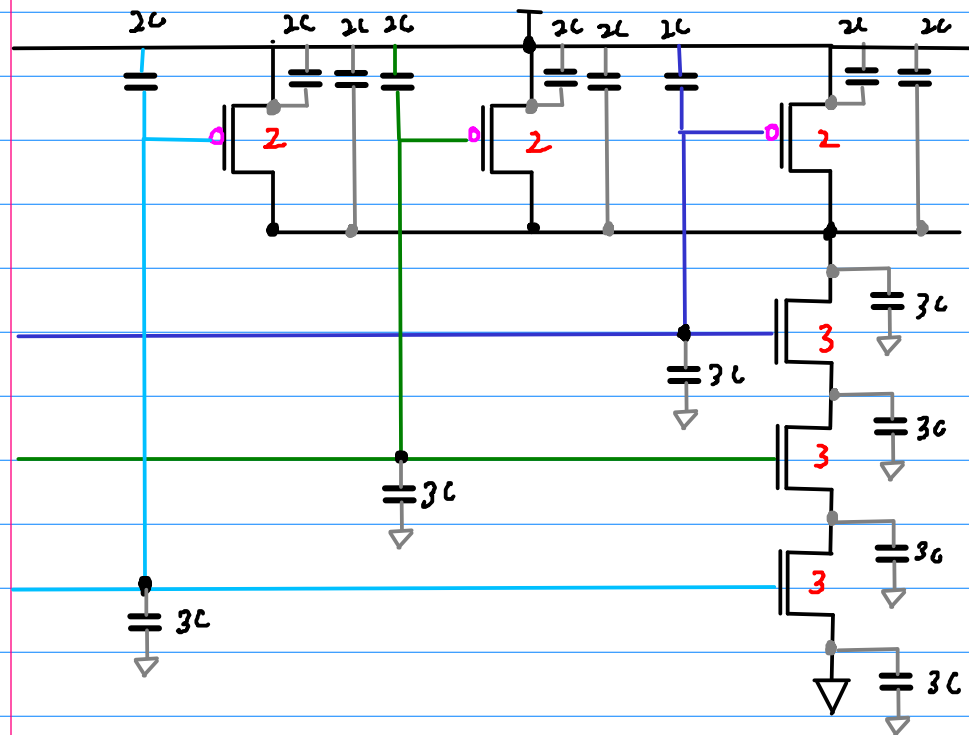
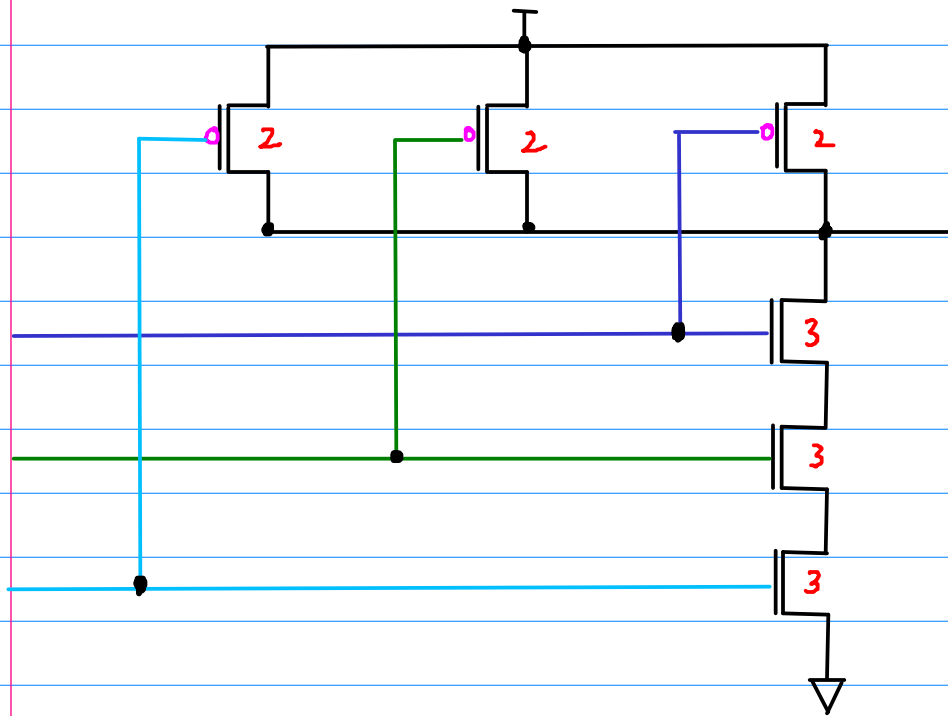
charge +
discharge -

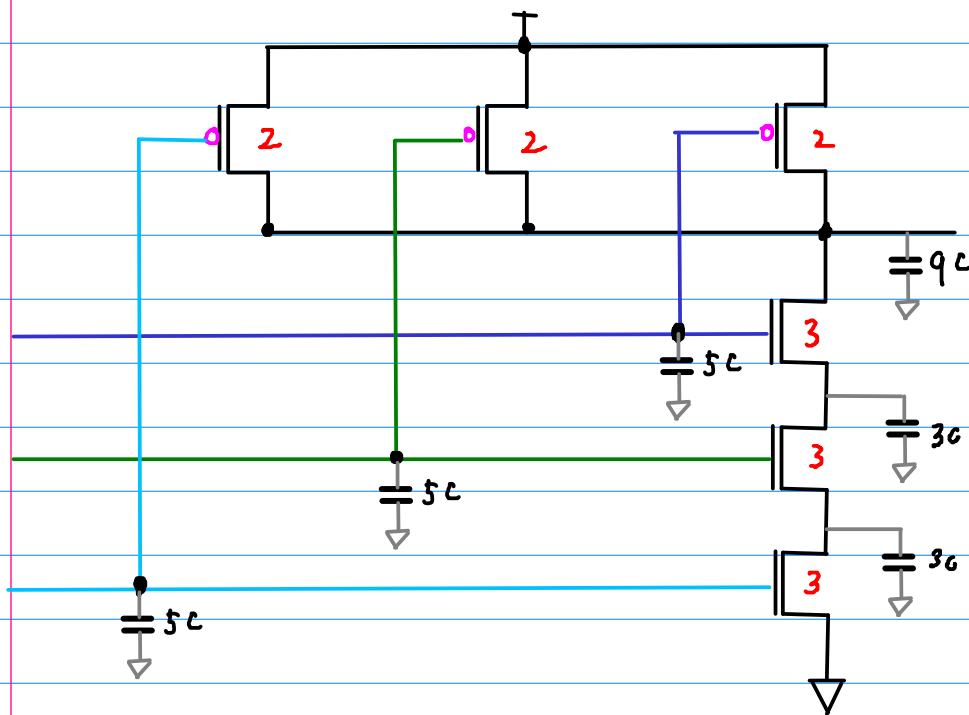
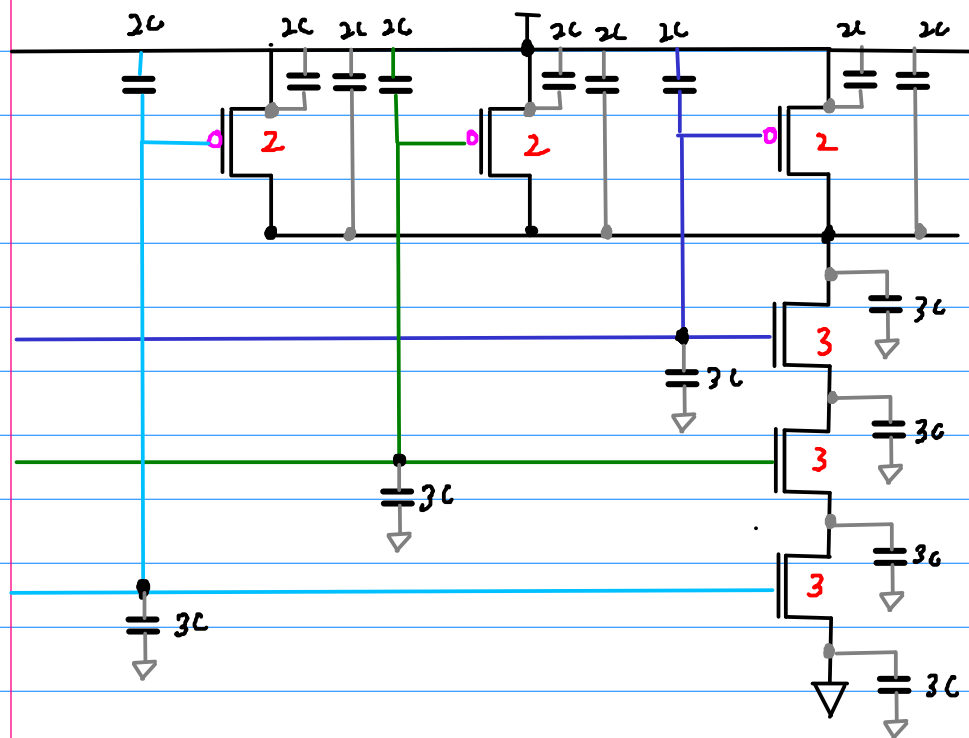
charge +



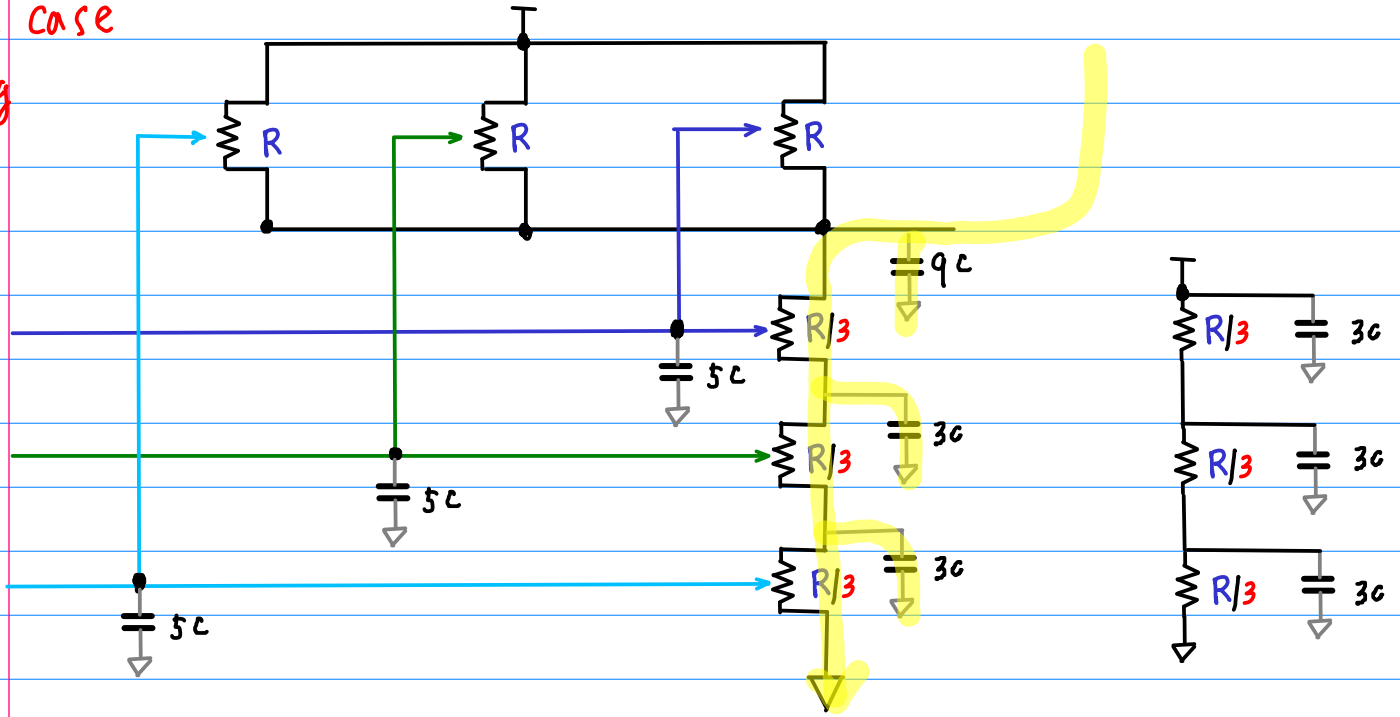




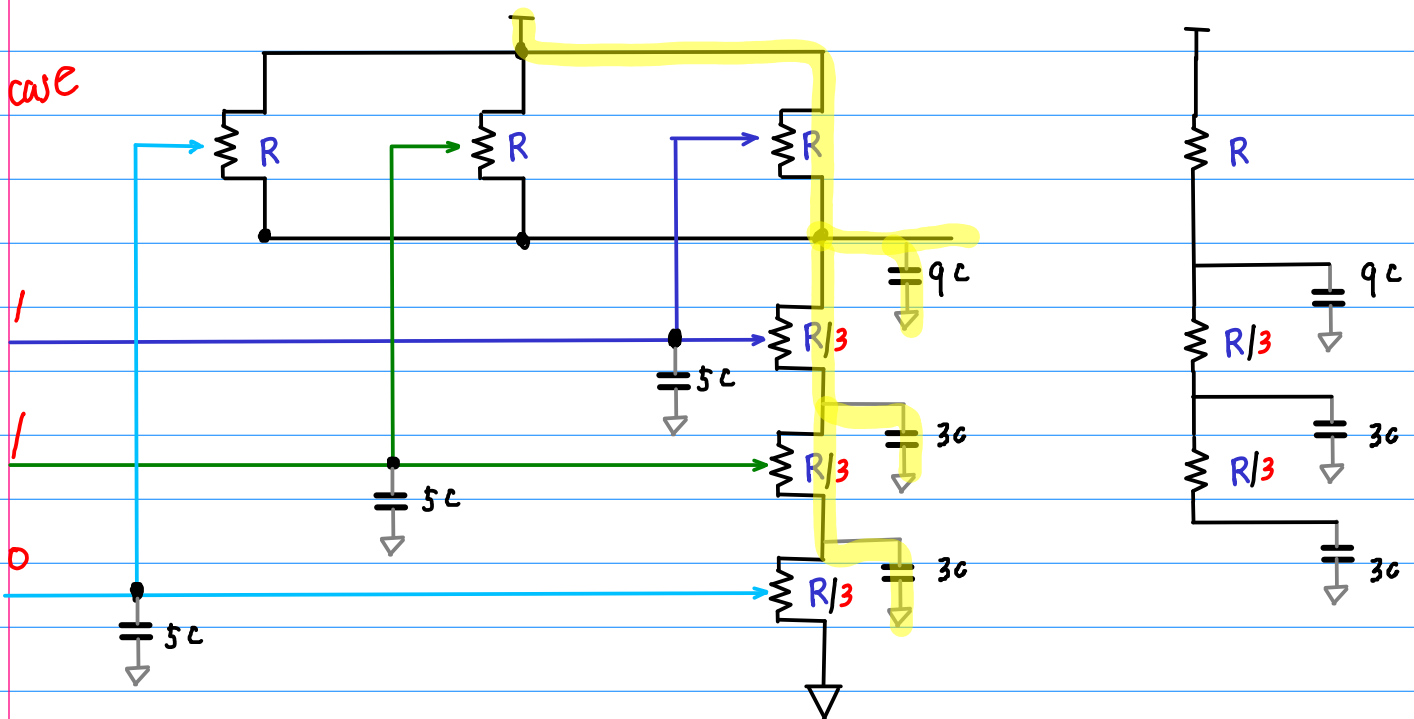




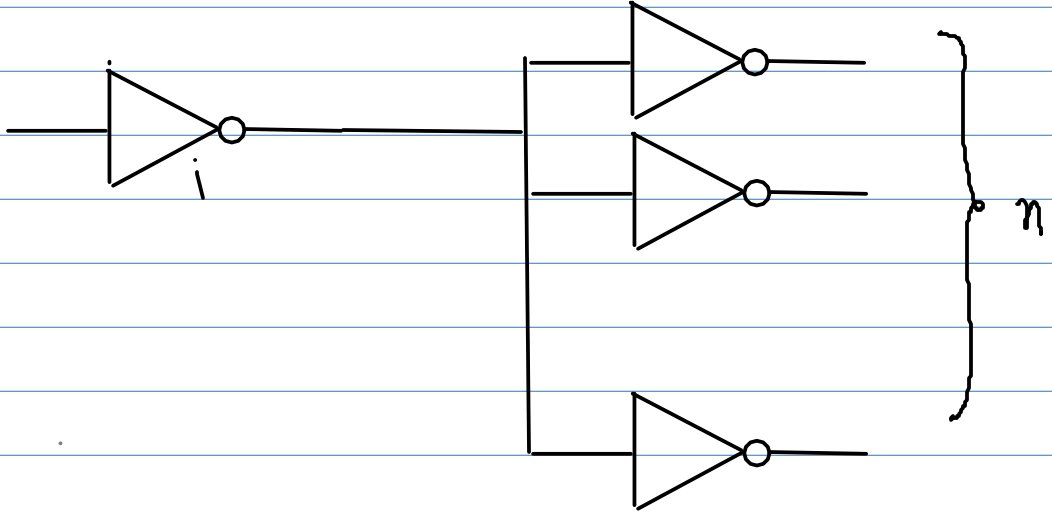
Worst case falling



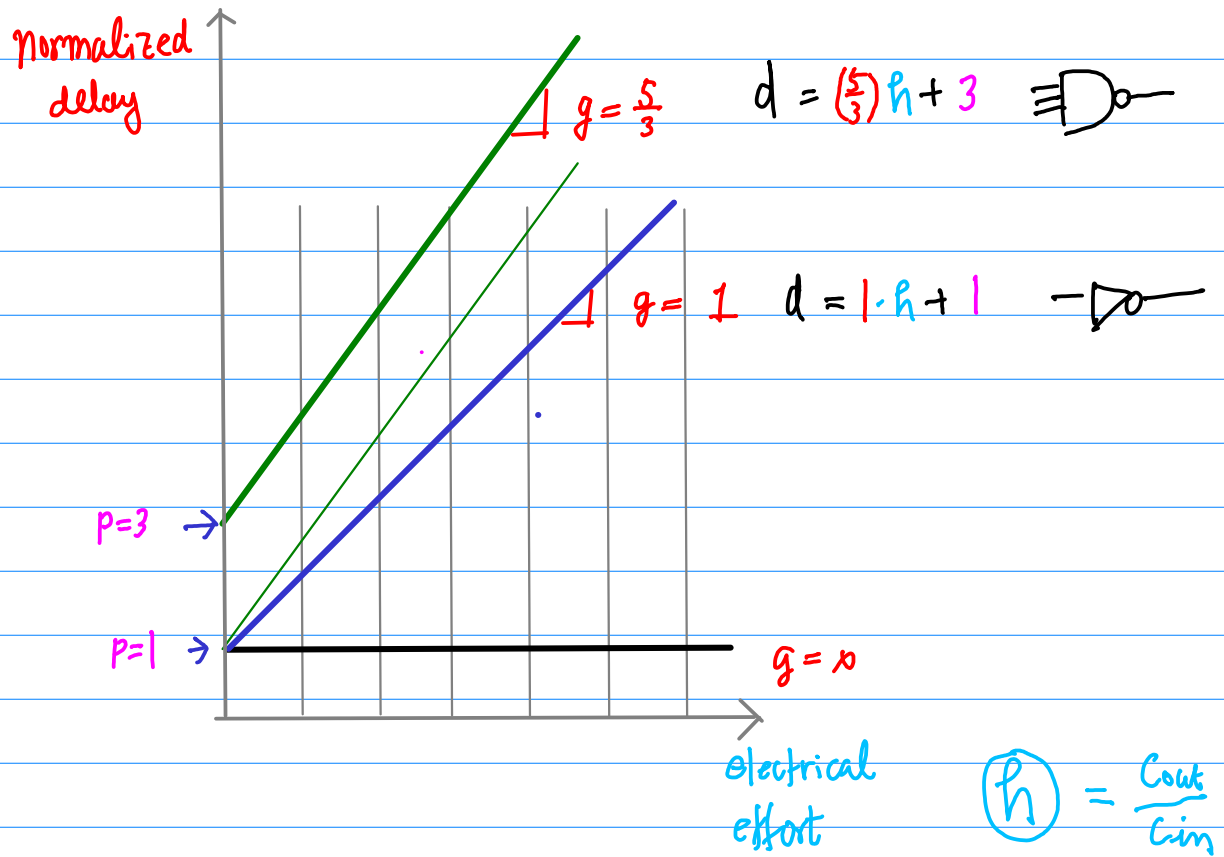
Worst case rising



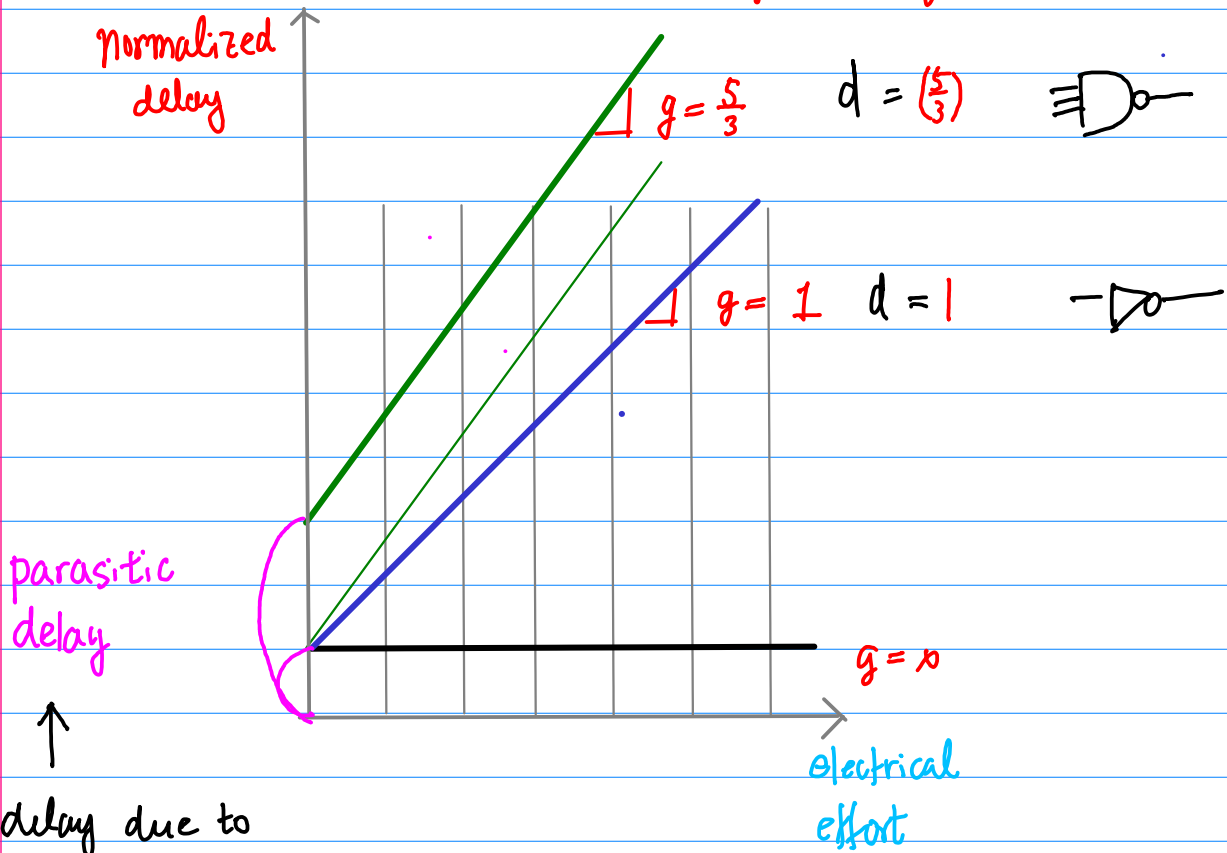
0



Linear Delay Model



Slope : logical effort



↑
delay due to
only internal cap
without external load cap

$$d = g \cdot h + p$$

↑ ↑ ↑
k c c

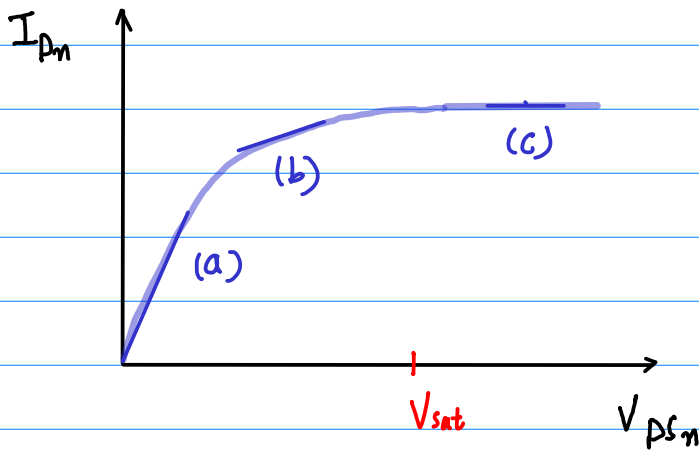


FET RC Model

$$R_n = \frac{V_{DSn}}{I_{Dn}}$$

$$I_{Dn} \cong \beta_n (V_{GSn} - V_{Tn}) V_{DSn}$$

non-saturated	{	$R_n \cong \frac{1}{\beta_n (V_{GSn} - V_{Tn})}$	(a) small V_{DSn}	$V_{DSn}^2 \approx 0$
		$R_n = \frac{2}{\beta_n [2(V_{GSn} - V_{Tn}) - V_{DSn}]}$	(b)	$V_{DS} \neq 0$
saturated	{	$R_n = \frac{2V_{DSn}}{\beta_n (V_{GSn} - V_{Tn})^2}$	(c)	



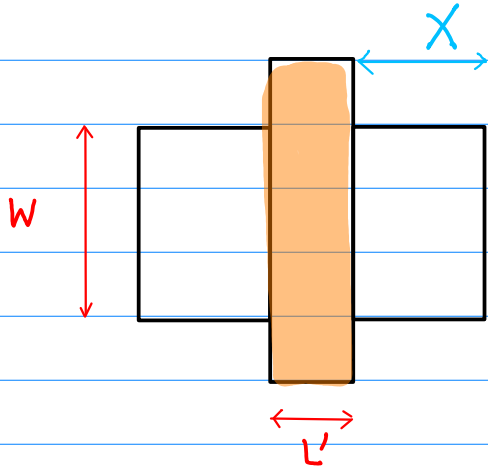
$$R_n \propto \frac{1}{\beta_n} \quad \beta_n = k'_n \left(\frac{W}{L}\right)_n$$

$$R_n = \frac{\eta}{\beta_n (V_{DD} - V_{Tn})} \quad \eta = 1 \sim 6$$

↑
largest possible V_{GSn}

$$\boxed{R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}} \quad \Omega \quad \eta = 1$$

MOS Capacitance



$$C_g = C_{ox} A_g \quad A_g = WL'$$
$$= C_{ox} WL'$$

$$C_{gs} = \frac{1}{2} C_g$$

$$C_{gd} = \frac{1}{2} C_g$$

Junction Capacitance

A_{pn} : area of p-n junction

V_R : the reverse bias voltage

$$C_0 = C_j A_{pn}$$

C_0 : zero-bias capacitance ($V_R=0$)

$$C = \frac{C_0}{\left(1 + \frac{V_R}{\phi_0}\right)^{m_j}}$$

m_j : grading coefficient

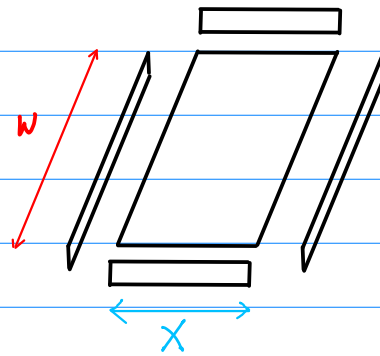
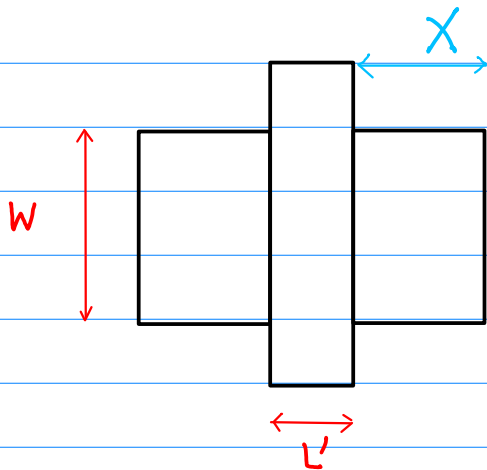
ϕ_0 : built-in potential

$m_j, \phi_0 \leftarrow$ doping characteristics

$$\phi_0 = \left(\frac{kT}{q}\right) \ln \left[\frac{N_d N_a}{n_i^2} \right]$$

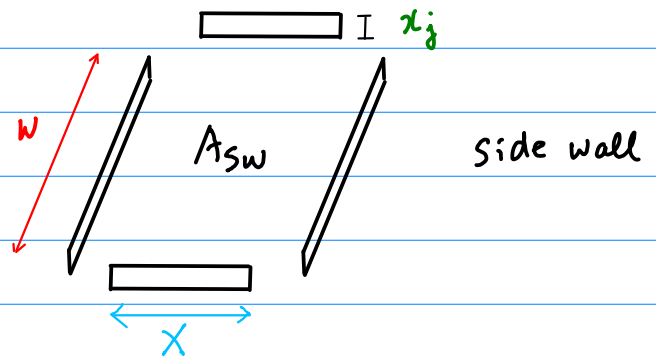
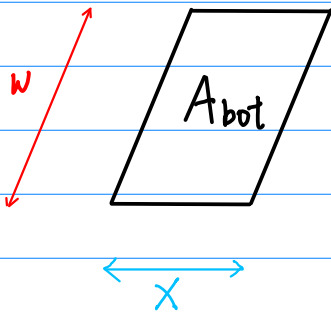
for an abrupt (step) junction

for a linearly graded function



bottom

sidewall



$$A_{bot} = X W$$

$$A_{sw} = 2(W \cdot x_j) + 2(X \cdot x_j)$$

$$= x_j P_{sw} = x_j (2W + 2X)$$

$$C_{bot} = C_j A_{bot}$$

$$C_{sw} = C_j A_{sw}$$

$$= C_j x_j P_{sw}$$

$$= C_{jsw} P_{sw}$$

$$A_{bot} = X W$$

$$A_{sw} = 2(W \cdot x_j) + 2(X \cdot x_j)$$

$$P_{sw} = (2W + 2X)$$

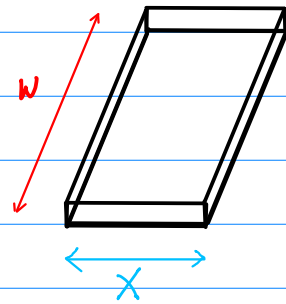
$$C_{jsw} = C_j x_j$$

for overlap $X \leftarrow X + L_o$

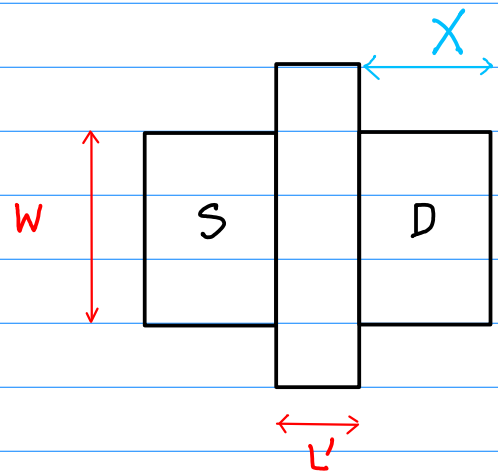
The total zero-bias
capacitance of $n+$ region

$$C_n = C_{bot} + C_{sw}$$

$$= C_j A_{bot} + C_{jsw} P_{sw}$$



$$C_n \Rightarrow C_{SB} \text{ \& \ } C_{DB}$$



$$C_s = C_{gs} + C_{SB}$$

$$C_D = C_{GD} + C_{DB}$$

non-linear version

$$C_n = \frac{C_j A_{bot}}{\left(1 + \frac{V}{\phi_o}\right)^{m_j}} + \frac{C_{jsw} P_{sw}}{\left(1 + \frac{V}{\phi_{osw}}\right)^{m_{jsw}}}$$

V : reverse voltage

m_j : grading coefficients) bottom
 ϕ_o : built-in potential)

m_{jsw} : grading coefficients) sidewalls
 ϕ_{osw} : built-in potential)

$$C_s = C_{gs} + C_{sb}$$

$$C_D = C_{gd} + C_{db}$$

$$C_{gs} = \frac{1}{2} C_g$$

$$C_{sb} = C_n$$

$$C_{gd} = \frac{1}{2} C_g$$

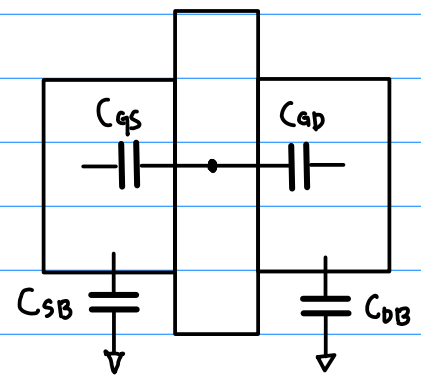
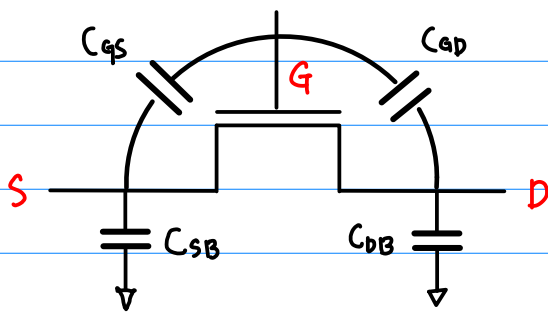
$$C_{db} = C_n$$

$$C_g = C_{ox} W L'$$

$$C_n = C_j \{ X W + 2 X_j (W + X) \}$$

gate cap

junction cap



PFET Characteristics

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$I_{Dp} = \frac{\beta_p}{2} (V_{SGp} - |V_{Tp}|)^2$$

$$\beta_p = K'_p \left(\frac{W}{L}\right)_p$$

$$K'_p = \mu_p C_{ox}$$

$$r = \frac{\mu_n}{\mu_p} = 2 \sim 3$$

$$\beta_n = K'_n \left(\frac{W}{L}\right)_n$$

$$\beta_p = K'_p \left(\frac{W}{L}\right)_p$$

$$V_{sat} = V_{SGp} - |V_{Tp}|$$

$$I_{Dp} = \frac{\beta_p}{2} [2(V_{SGp} - |V_{Tp}|)V_{SDp} - V_{SDp}^2]$$

$$I_{Dp} = \frac{\beta_p}{2} [V_{SGp} - |V_{Tp}|]^2$$

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)}$$

$$R_p \propto \frac{1}{\beta_p} = \frac{1}{K'_p \left(\frac{W}{L}\right)_p}$$

$$C_{gp} = C_{ox} (WL)_p$$

$$C_{gs} = \frac{1}{2} C_{gp} \approx C_{gp}$$

$$C_p = C_j A_{bot} + C_{jsw} P$$

Fall Time Calculation

$$i = -C_{out} \frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$$

$$V_{out}(t) = V_{DD} e^{-t/\tau_n}$$

$$\tau_n = R_n C_{out}$$

$$t = \tau_n \ln \left(\frac{V_{DD}}{V_{out}} \right)$$

$$\begin{aligned} t_f = t_y - t_x &= \tau_n \ln \left(\frac{V_{DD}}{0.1 V_{DD}} \right) - \tau_n \ln \left(\frac{V_{DD}}{0.9 V_{DD}} \right) \\ &= \tau_n \ln(9) \end{aligned}$$

$$t_{HL} = t_f \cong 2.2 \tau_n$$

Rise Time Calculation

$$i = -C_{out} \frac{dV_{out}}{dt} = \frac{V_{DD} - V_{out}}{R_p}$$

$$V_{out}(t) = V_{DD} [1 - e^{-t/\tau_p}]$$

$$\tau_p = R_p C_{out}$$

$$t = \tau_p \ln \left(\frac{V_{DD}}{V_{out}} \right)$$

$$\begin{aligned} t_f = t_r - t_u &= \tau_p \ln \left(\frac{V_{DD}}{0.1 V_{DD}} \right) - \tau_n \ln \left(\frac{V_{DD}}{0.9 V_{DD}} \right) \\ &= \tau_p \ln(9) \end{aligned}$$

$$t_{LH} = t_r \cong 2.2 \tau_p$$

Propagation Delay

$$t_p = \frac{(t_{pf} + t_{pr})}{2}$$

$$t_{pf} = \ln(2) \cdot \tau_n$$

$$t_{pr} = \ln(2) \cdot \tau_p$$

$$t_p \cong 0.35 (\tau_n + \tau_p)$$

$$C_{out} = C_{FET} + C_L$$

$$t_r = 2.2 R_p (C_{FET} + C_L)$$

$$t_f = 2.2 R_n (C_{FET} + C_L)$$

$$t_r = t_{ro} + \alpha_p C_L$$

$$t_f = t_{ro} + \alpha_n C_L$$

$$C_L = 0 \rightarrow t_r = t_{ro} \cong 2.2 R_p C_{FET}$$

$$C_L = 0 \quad t_f = t_{ro} \cong 2.2 R_n C_{FET}$$

$$\alpha_p = 2.2 R_p = \frac{2.2}{\beta_p (V_{DD} - |V_{Tp}|)}$$

$$\alpha_n = 2.2 R_n = \frac{2.2}{\beta_n (V_{DD} - |V_{Tn}|)}$$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$