

Logic Families Dynamic-2 (H.2)

20151215

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References

Some Figures from the following sites

[1] <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>

Weste & Harris Book Site

[2] en.wikipedia.org

[3] Digital Integrated Circuits : A Design Perspective,

Jan M. Rabaey,

(<http://bwrcs.eecs.berkeley.edu/Classes/lcBook/>)

[4] Digital Electronics and Design with VHDL

Pedroni

Other MOS Architectures

Static MOS

Pseudo-nMOS Logic

Transmission-gate Logic

BiCMOS Logic

Dynamic MOS

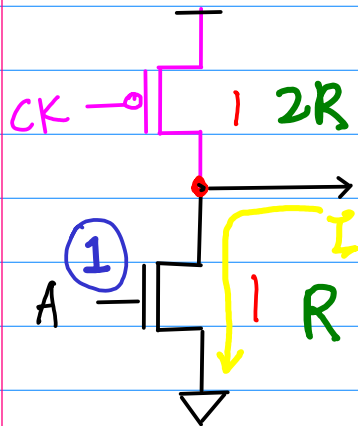
Dynamic Logic

Domino Logic

C2MOS Logic

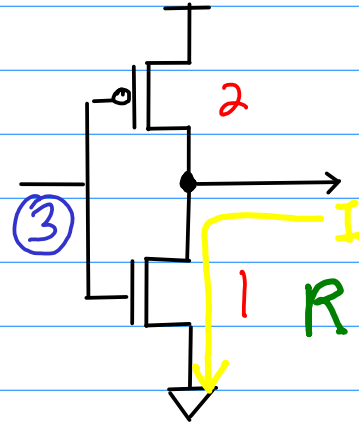
Logical Efforts and Dynamic Logic

Unfooted Inverter



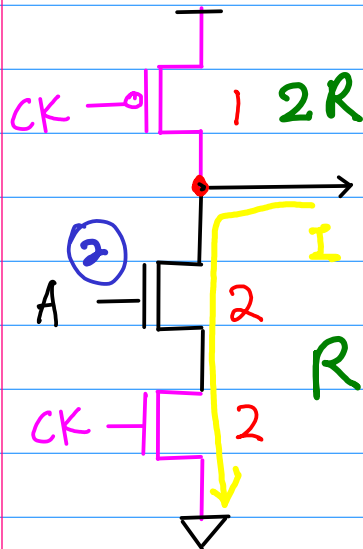
$$g_d = 1/3 < 1$$

Unit Inverter



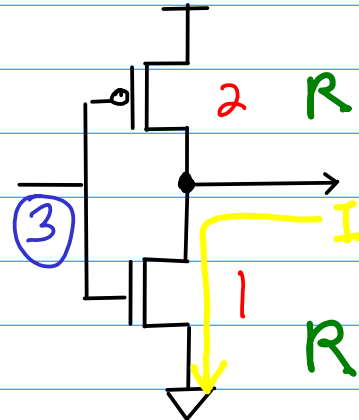
improved down logical effort
faster fall time

Footed Inverter



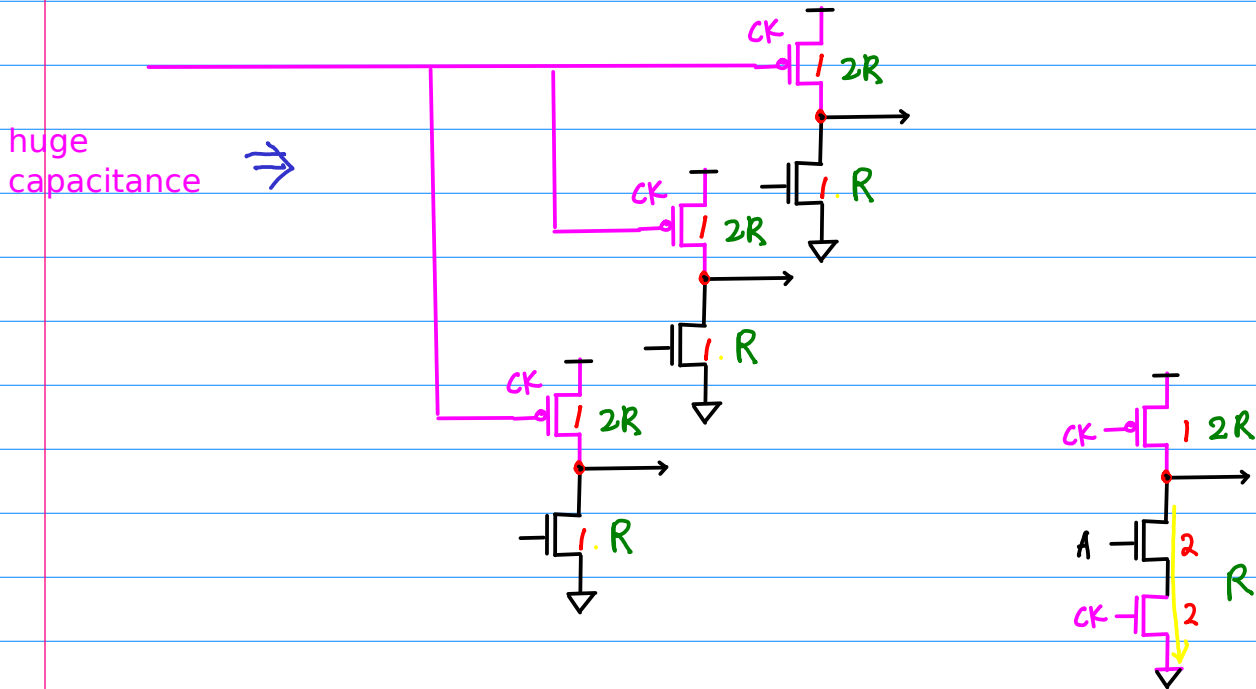
$$g_d = 2/3 < 1$$

Unit Inverter



improved down logical effort
faster fall time

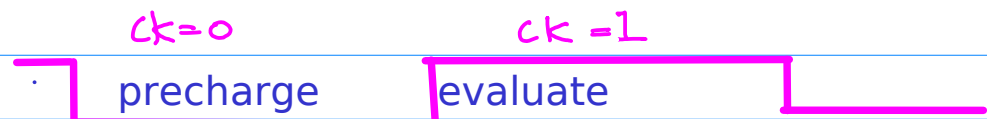
Precharge and Foot Transistors



Unfooted	Footed
$\left(\frac{W}{L}\right)_p \downarrow$ Precharge Transistor	$\left(\frac{W}{L}\right)_n \uparrow$ Foot Transistor
$\star R_p \uparrow$, rise delay \uparrow $\star C \downarrow$	$\star R_n \downarrow$, fall delay \downarrow $\star C \uparrow$

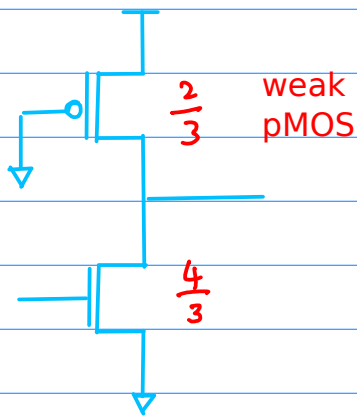
$C \downarrow$ more important because precharge does not require fast rise delay

$R \downarrow$ more important for the fast fall delay during evaluate phase

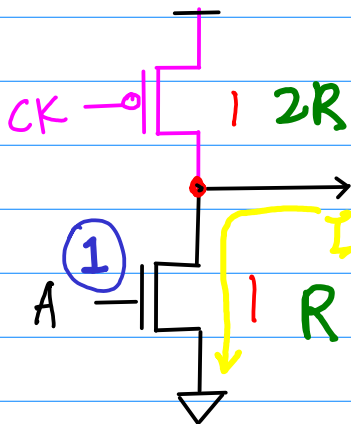


Dynamic Logic and Pseudo-nMOS Logic

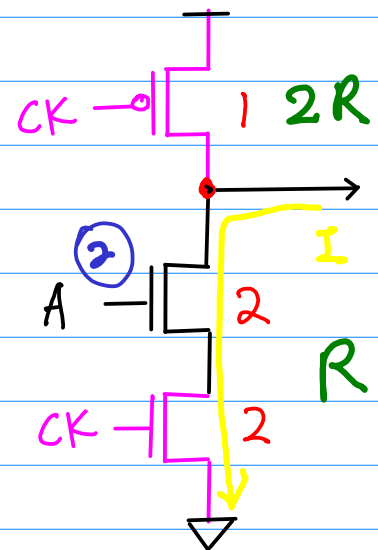
Pseudo-nMOS



Unfooted



Footed



$$\left(\frac{W}{L}\right)_p = \frac{1}{2} \left(\frac{W}{L}\right)_n$$

$$\cdot \frac{1}{4}$$

$$R_p = 4 R_n$$

$$\left(\frac{W}{L}\right)_p = 1 \left(\frac{W}{L}\right)_n$$

$$\cdot \frac{1}{2}$$

$$R_p = 2 R_n$$

$$\left(\frac{W}{L}\right)_p = \frac{1}{2} \left(\frac{W}{L}\right)_n$$

$$\cdot \frac{1}{4}$$

$$R_p = 4 R_n$$

$$\frac{1}{3} \sim \frac{1}{6}$$





