

# Logic Circuit Design

## NAND-1

20170217

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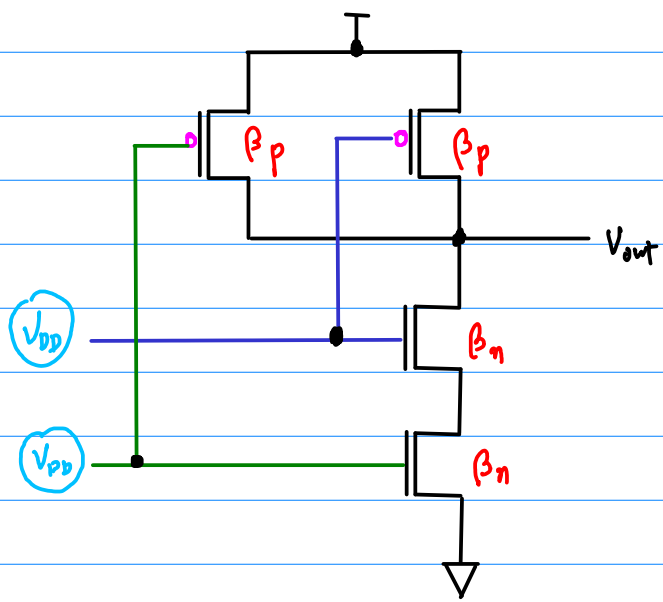
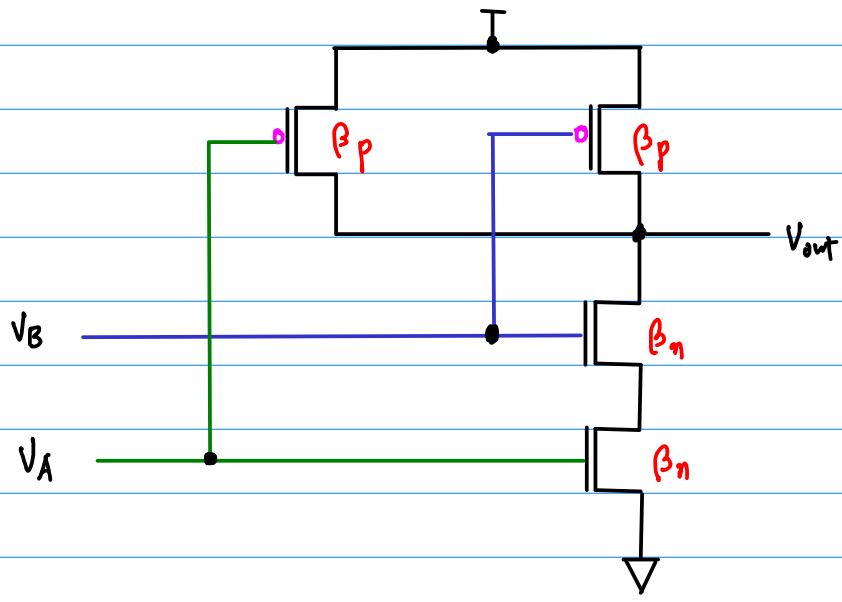
# References

Some Figures from the following sites

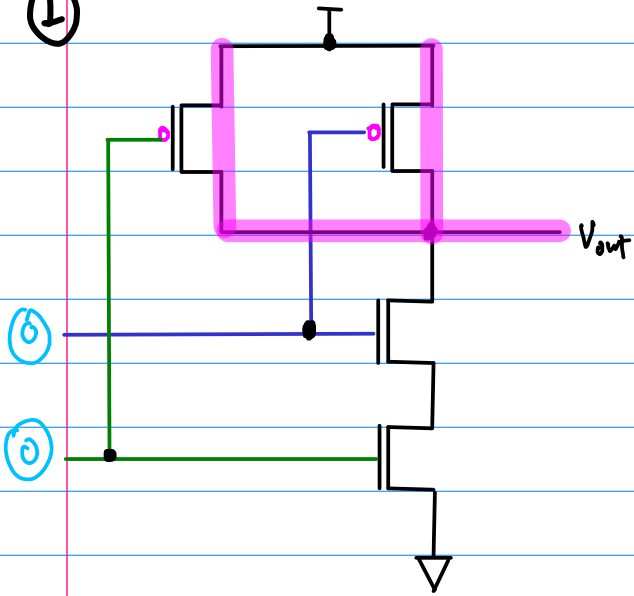
[1] <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>  
Weste & Harris Book Site

[2] Introduction to VLSI Circuits and Systems, Uyemura

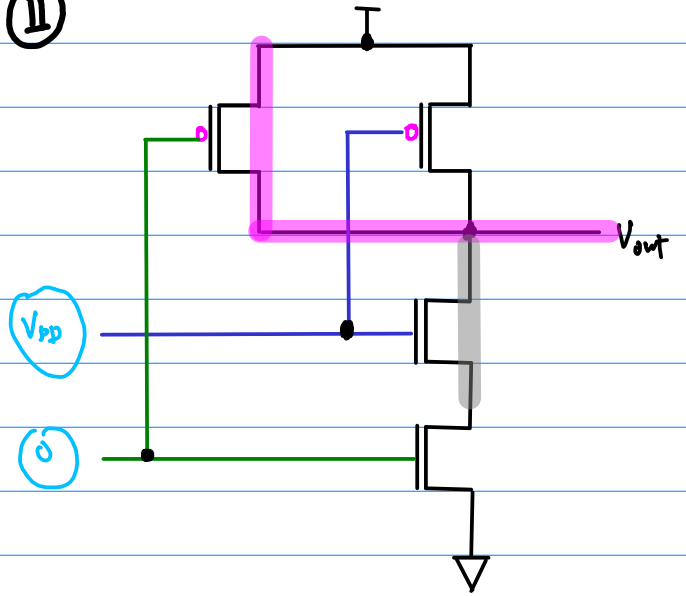
[2] [en.wikipedia.org](http://en.wikipedia.org)



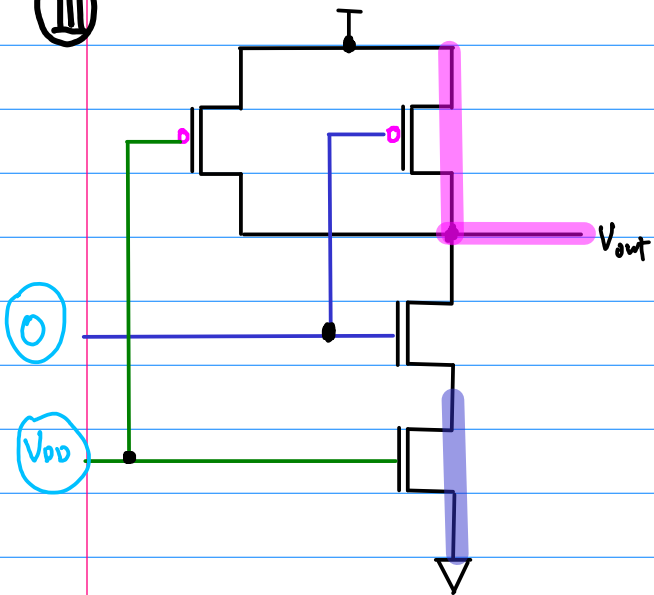
I



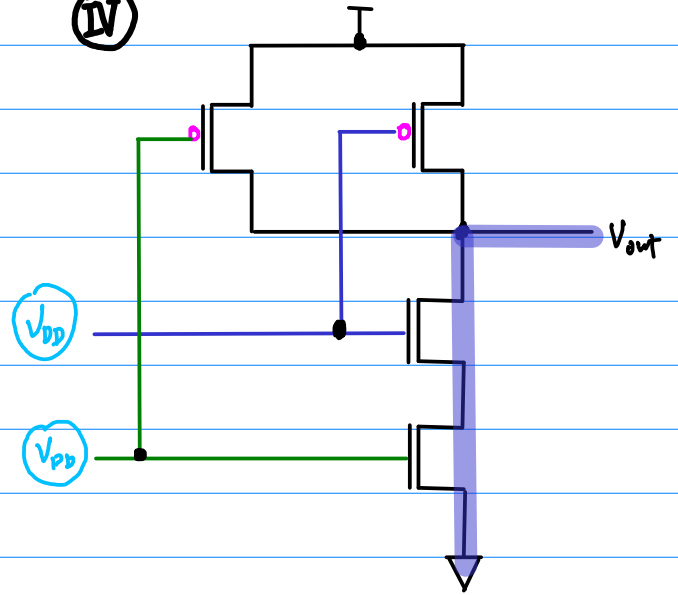
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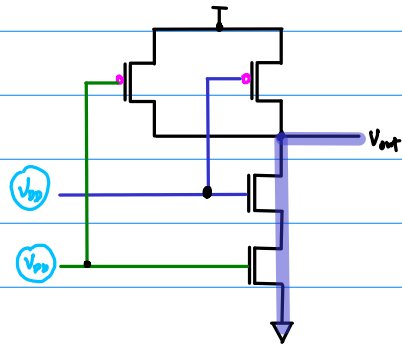
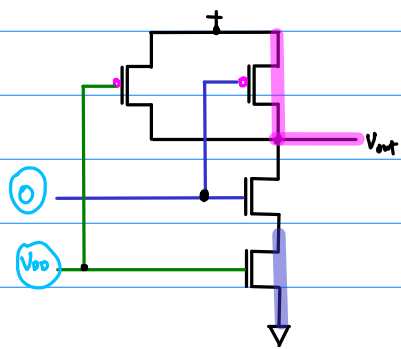
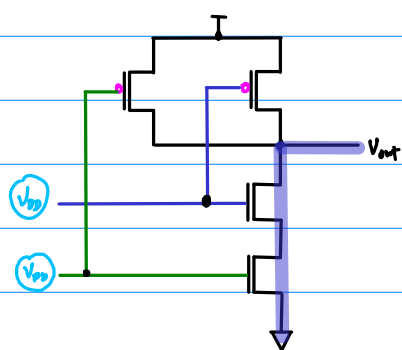
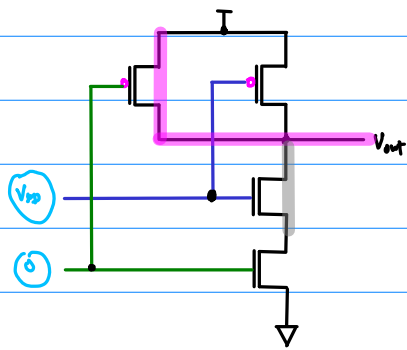
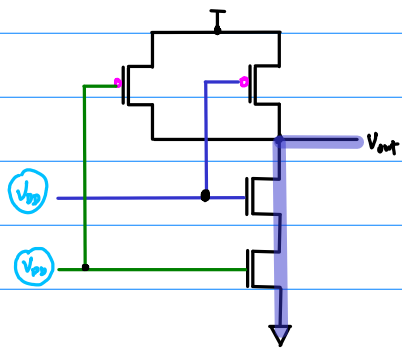
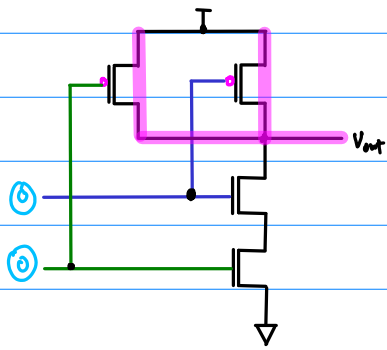


III

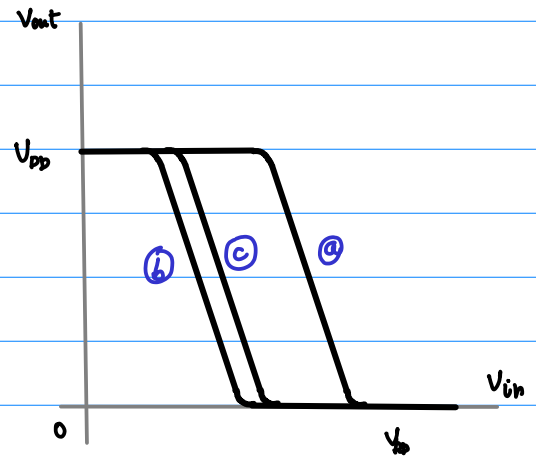


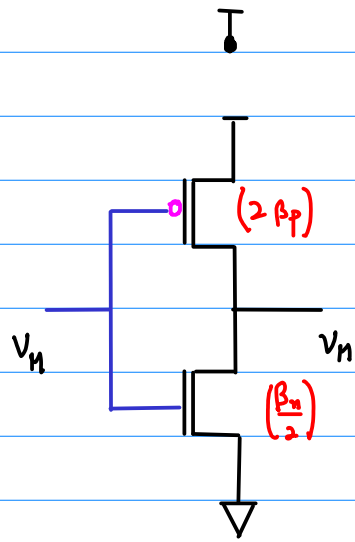
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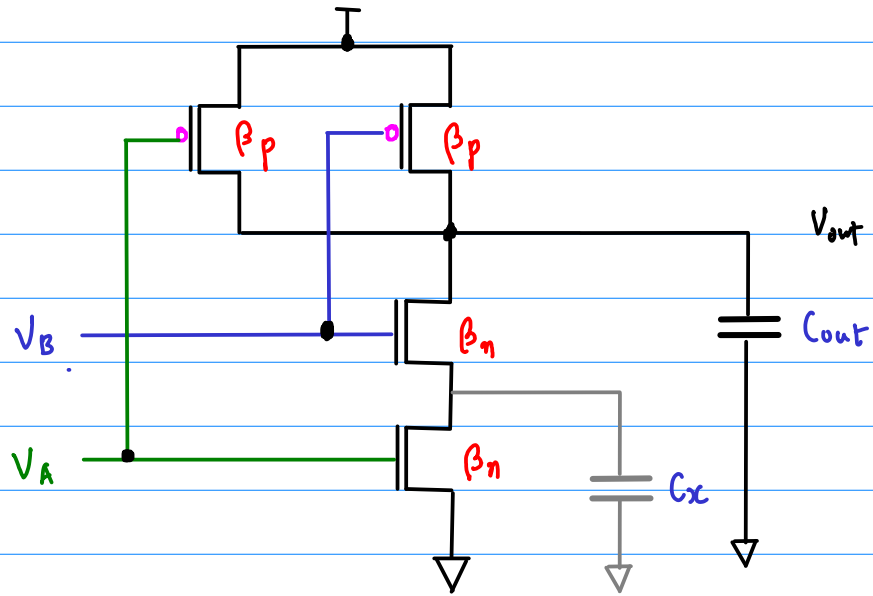




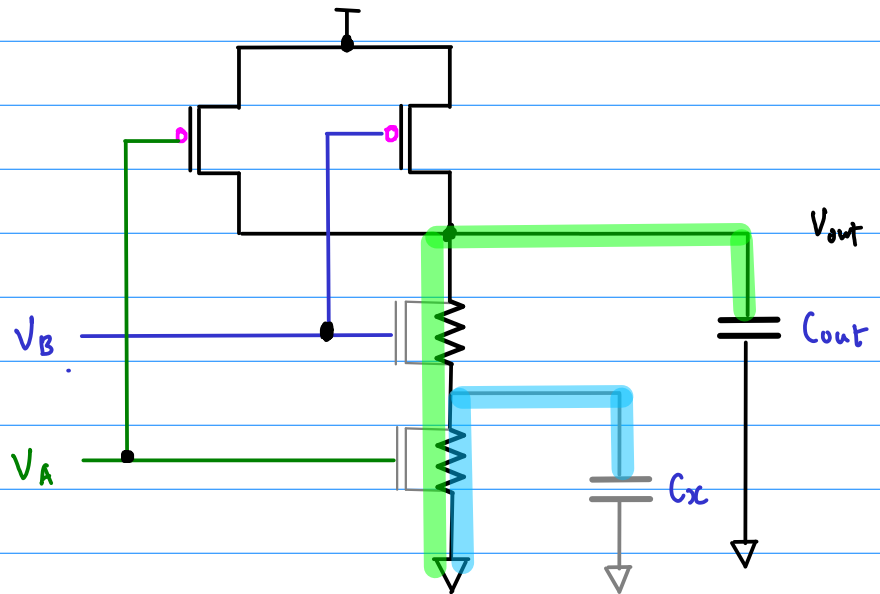
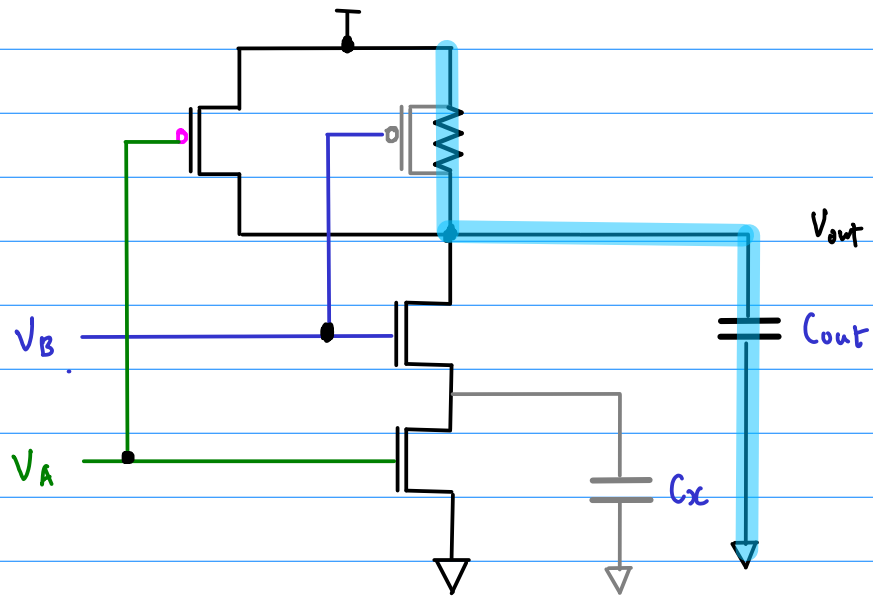
	$V_A$	$V_B$	$V_{out}$
(a)	0	0	$V_{DD}$
(b)	0	$V_{DD}$	$V_{DD}$
(c)	$V_{DD}$	0	$V_{DD}$
	$V_{DD}$	$V_{DD}$	0











$$C_{out} = C_{FET} + C_L$$

$$C_{FG1} = C_{Dn} + 2 C_{Dp}$$

$$R_p = \frac{1}{\beta_p (v_{DD} - |V_{Tp}|)} \quad R_n = \frac{1}{\beta_n (v_{DD} - V_{Tn})}$$

