Logic Circuit Design
NAND-1

20170217

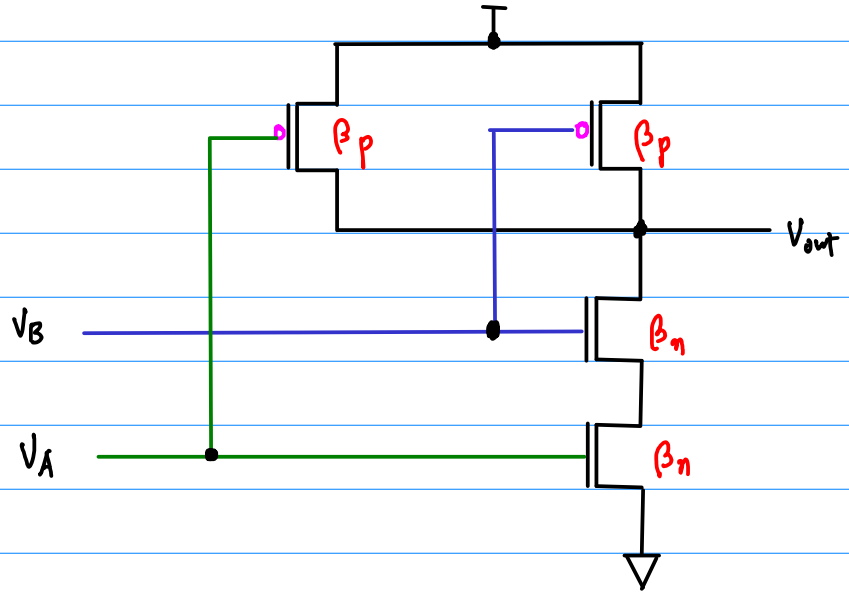
References

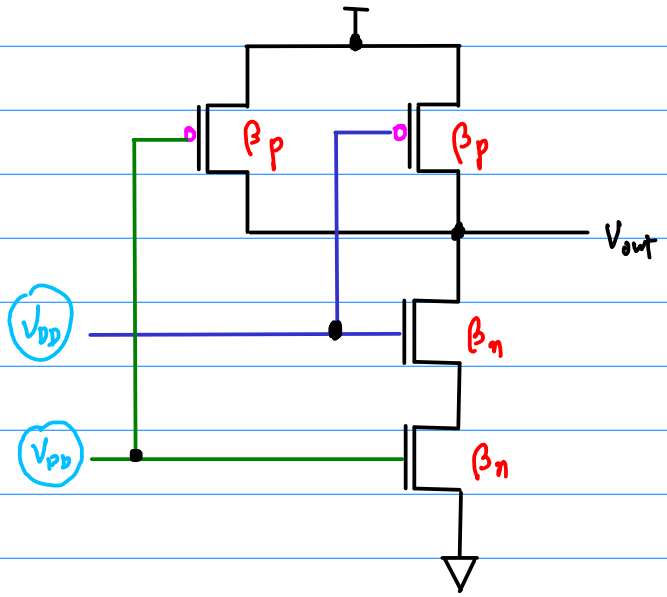
Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

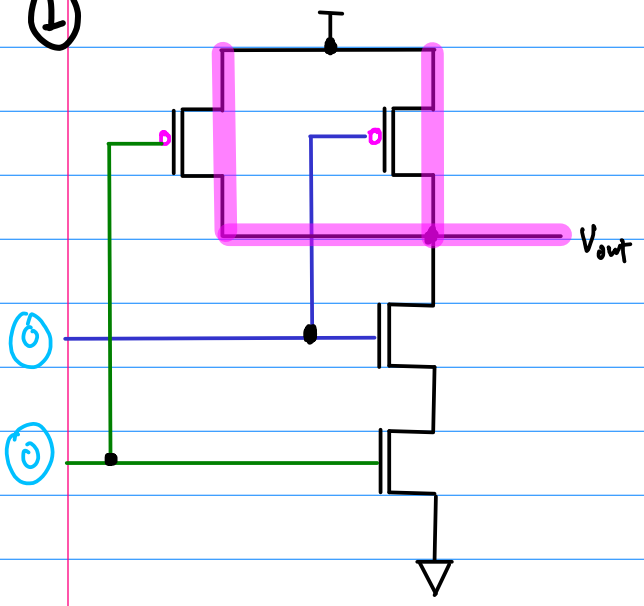
[2] Introduction to VLSI Circuits and Systems, Uyemura

[2] en.wikipedia.org

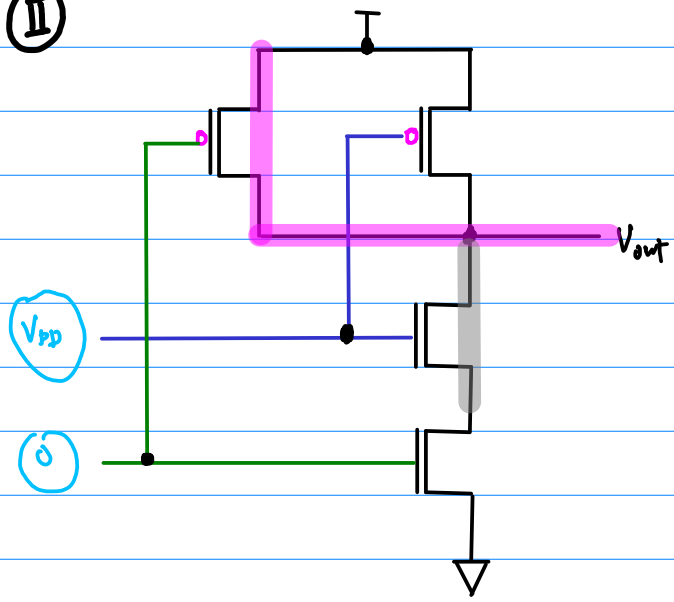

β_p
β_p
V_{out}
V_B
β_n
V_A
β_n


β_p
β_p
V_{out}
V_{DD}
β_n
V_{DD}
β_n

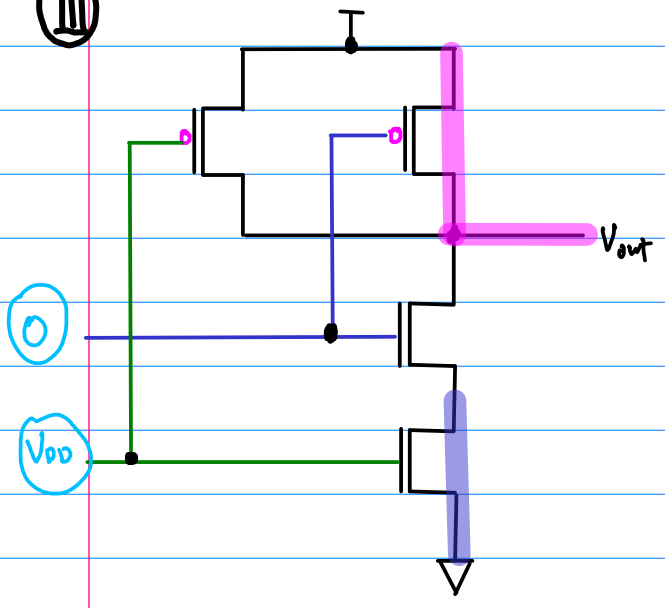
I



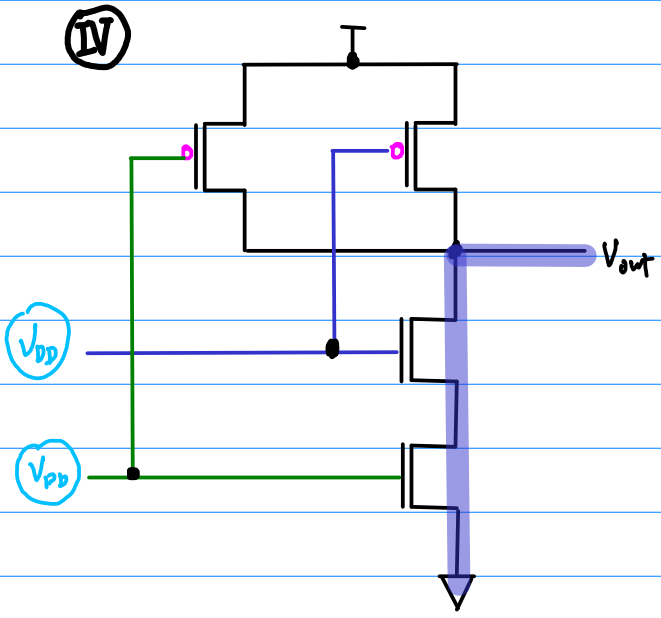
II

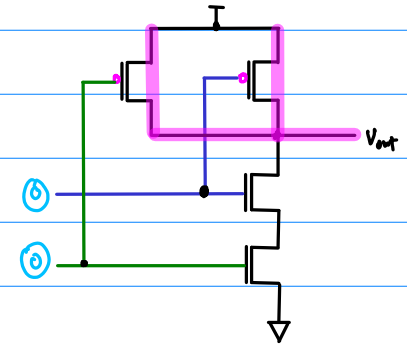


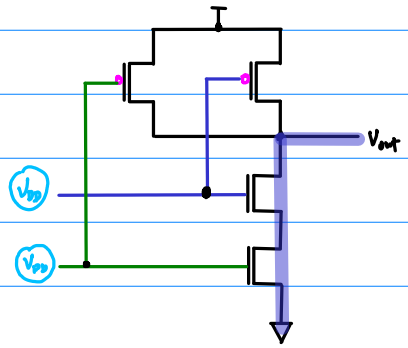
III

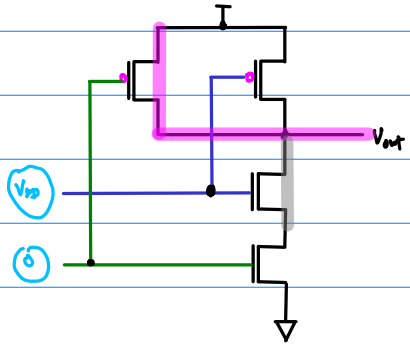


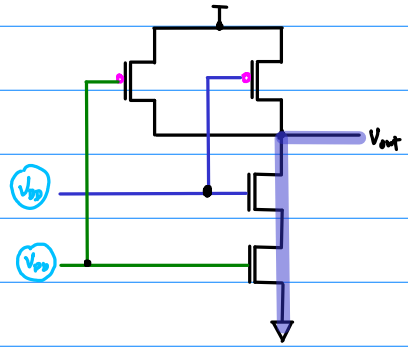
IV

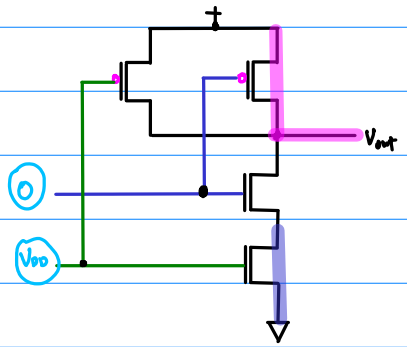


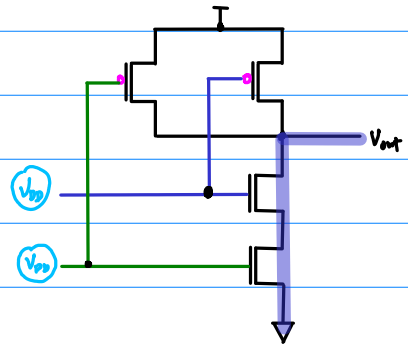

V_{out}
0
0


V_{out}
V_{DD}
V_{DD}

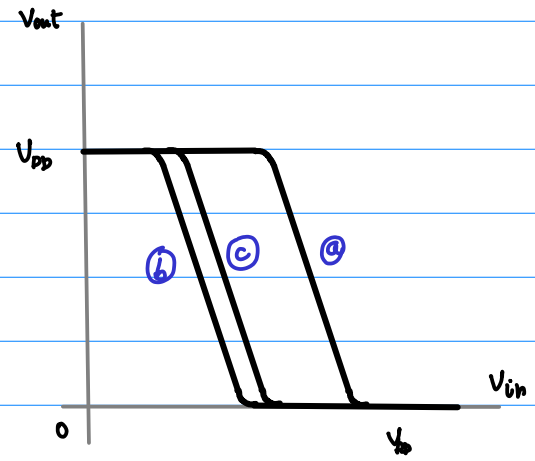

V_{out}
V_{DD}
0

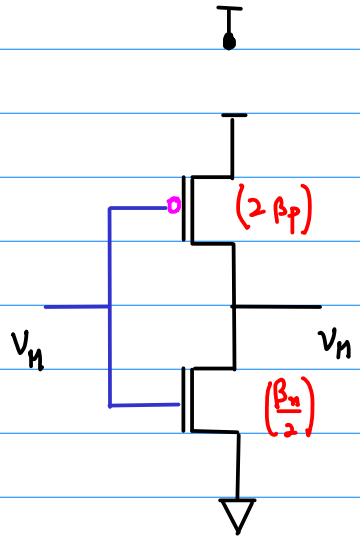

V_{out}
V_{DD}
V_{DD}

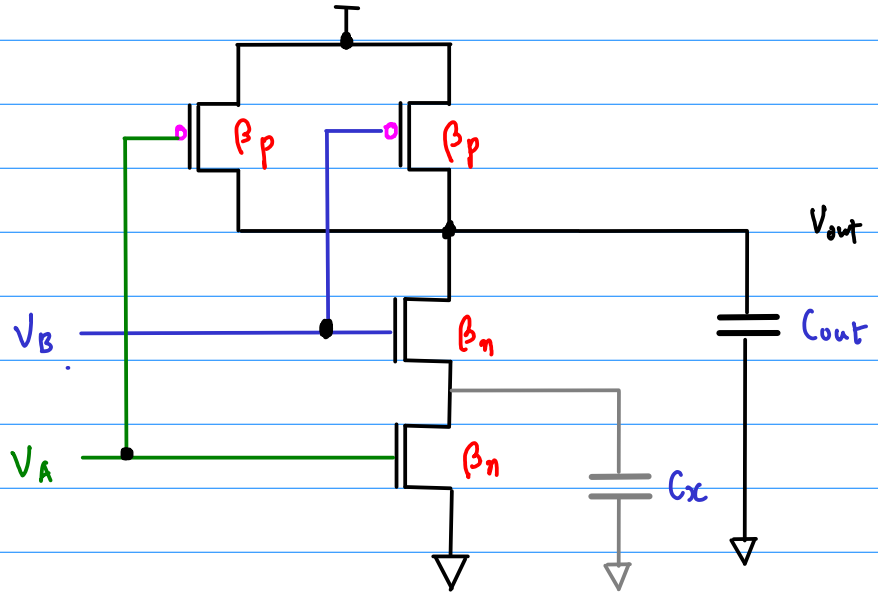

V_{out}
0
V_{DD}

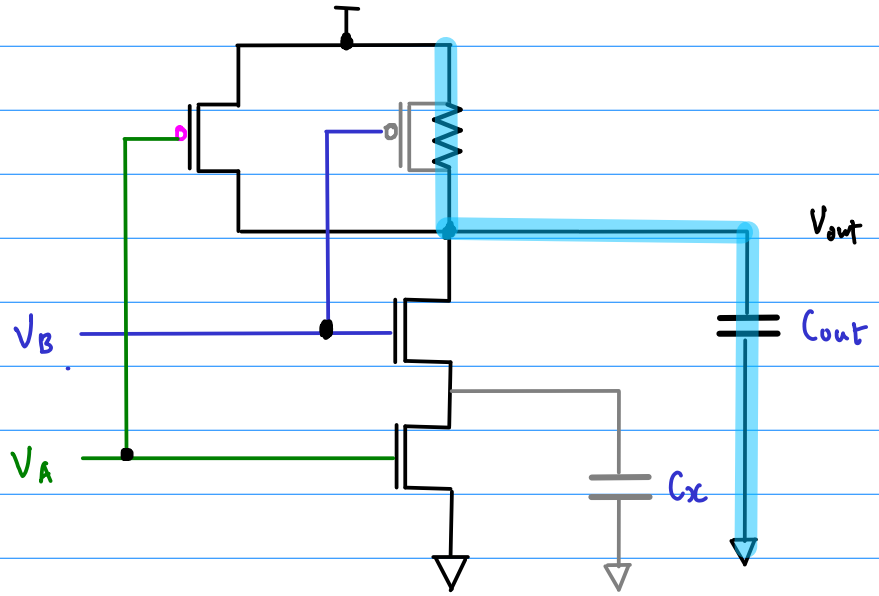

V_{out}
V_{DD}
V_{DD}

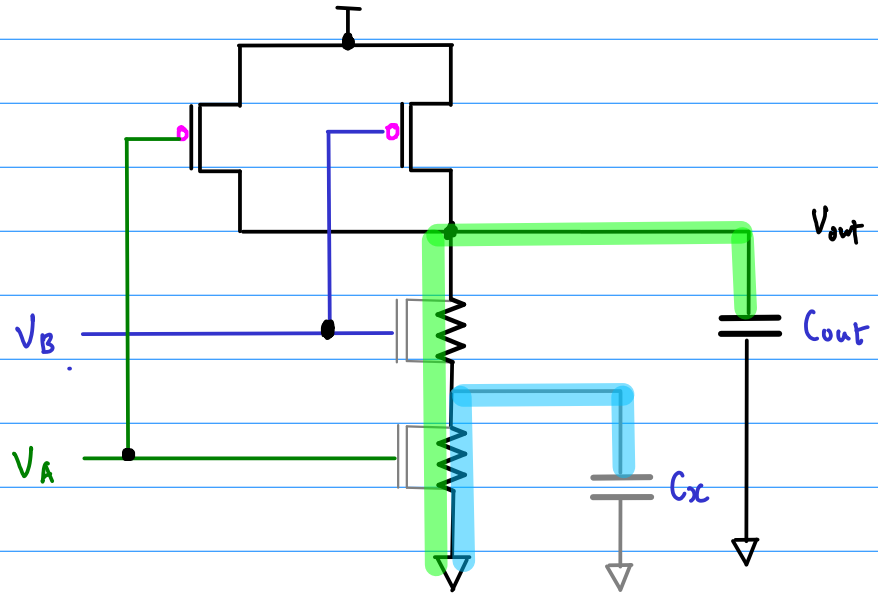
	V_A	V_B	V_{out}
ⓐ	0	0	V_{DD}
ⓑ	0	V_{DD}	V_{DD}
ⓒ	V_{DD}	0	V_{DD}
	V_{DD}	V_{DD}	0




$(2\beta_p)$
V_H
V_n
$\left(\frac{\beta_n}{2}\right)$


β_p
β_p
V_{out}
V_B
β_n
C_{out}
V_A
β_n
C_x


V_{out}
C_{out}
V_B
V_A
C_x


V_{out}
C_{out}
V_B
V_A
C_x

$$C_{out} = C_{FET} + C_L$$

$$C_{FG1} = C_{Dn} + 2C_{Dp}$$

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)} \qquad R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$