Pipelined Architecture (2A)

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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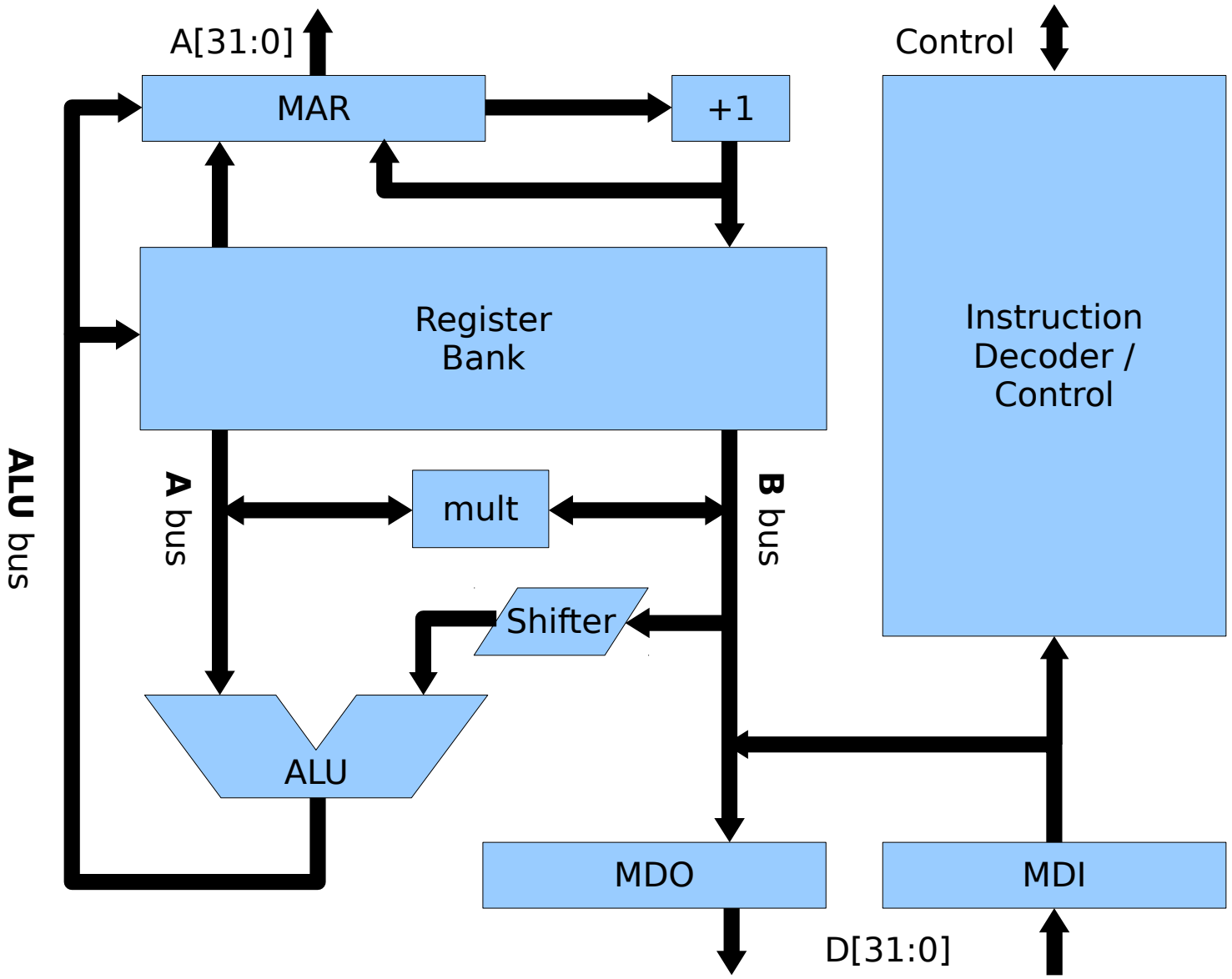
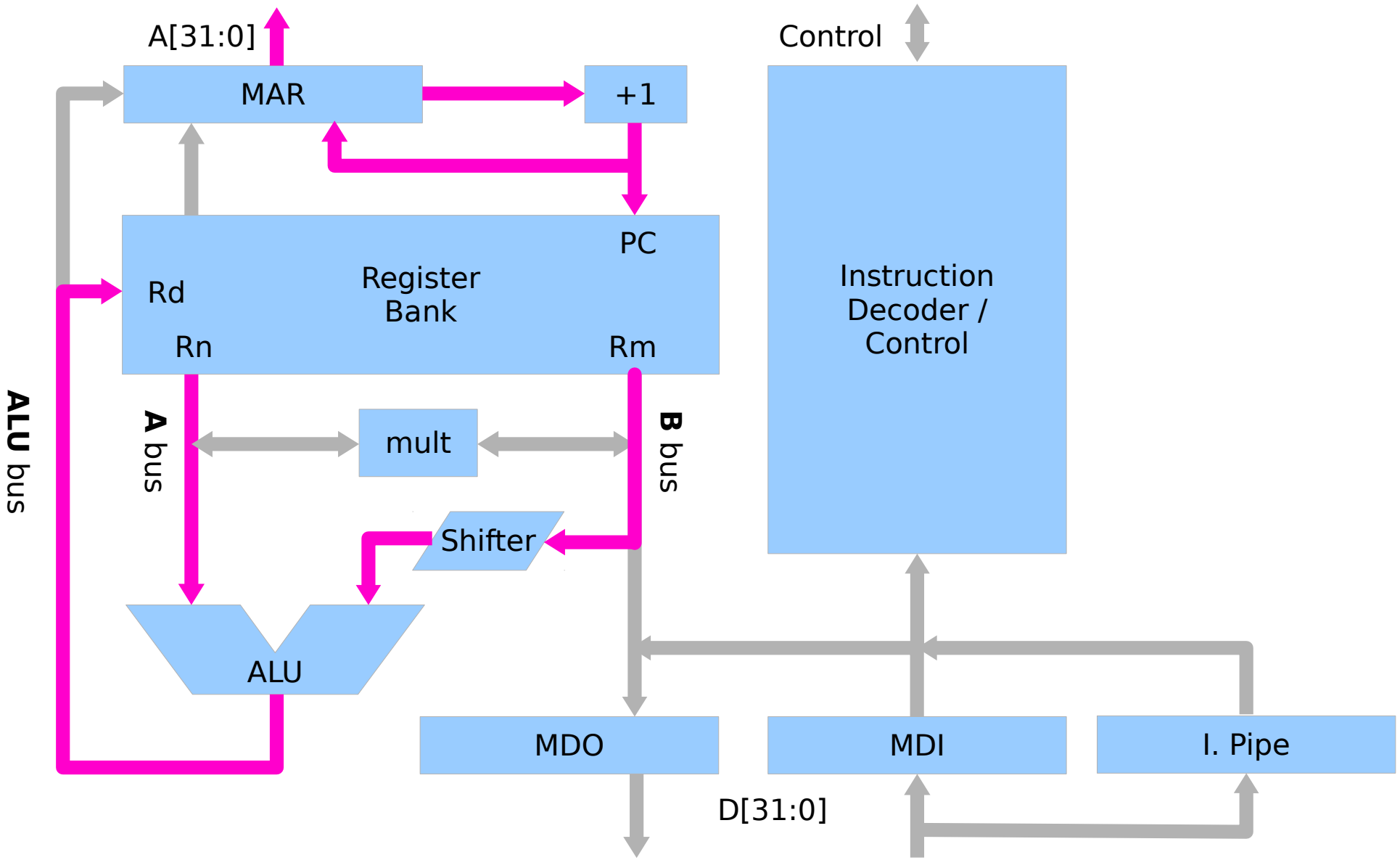
Based on

ARM System-on-Chip Architecture, 2nd ed, Steve Furber

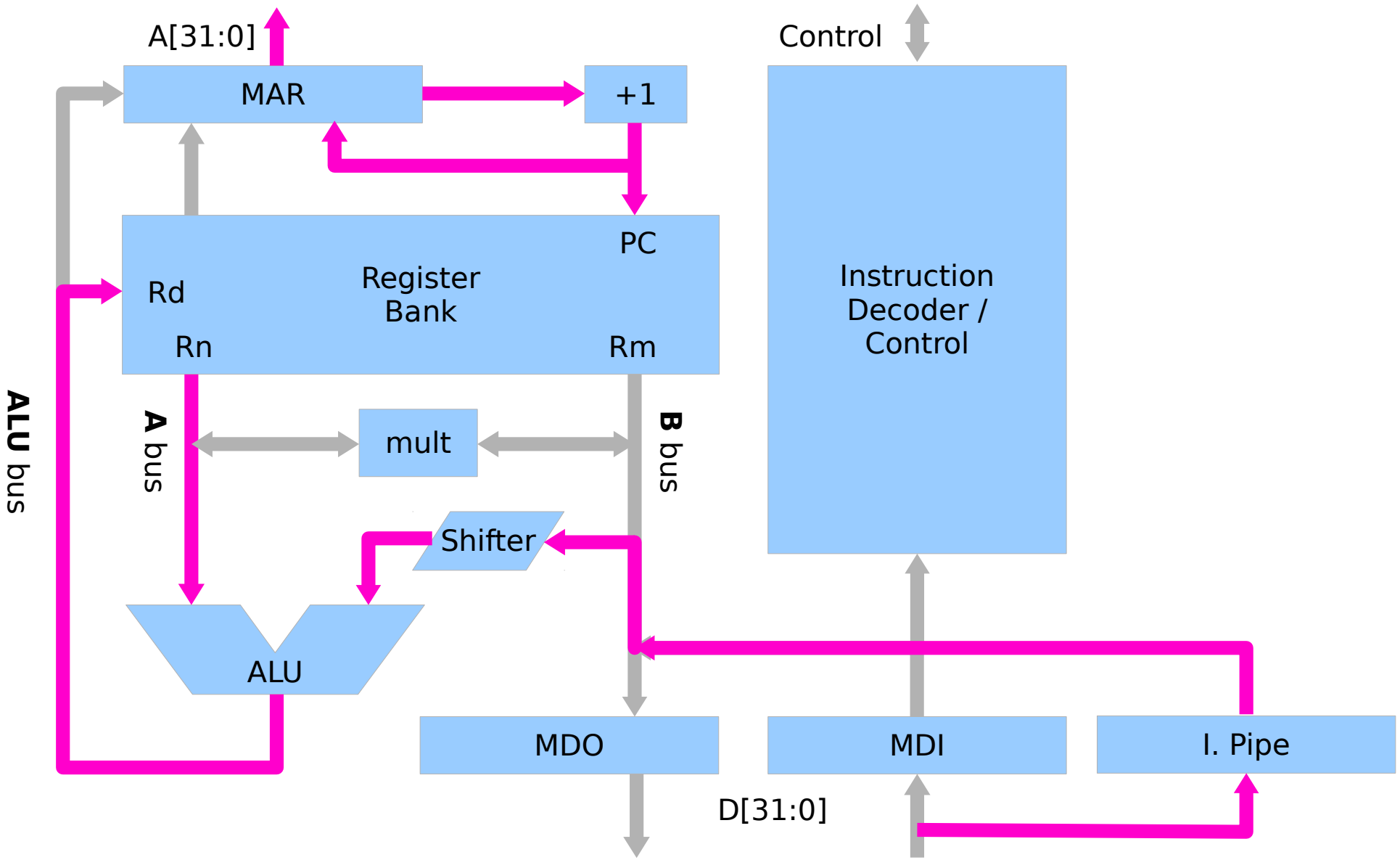
3-stage Pipeline



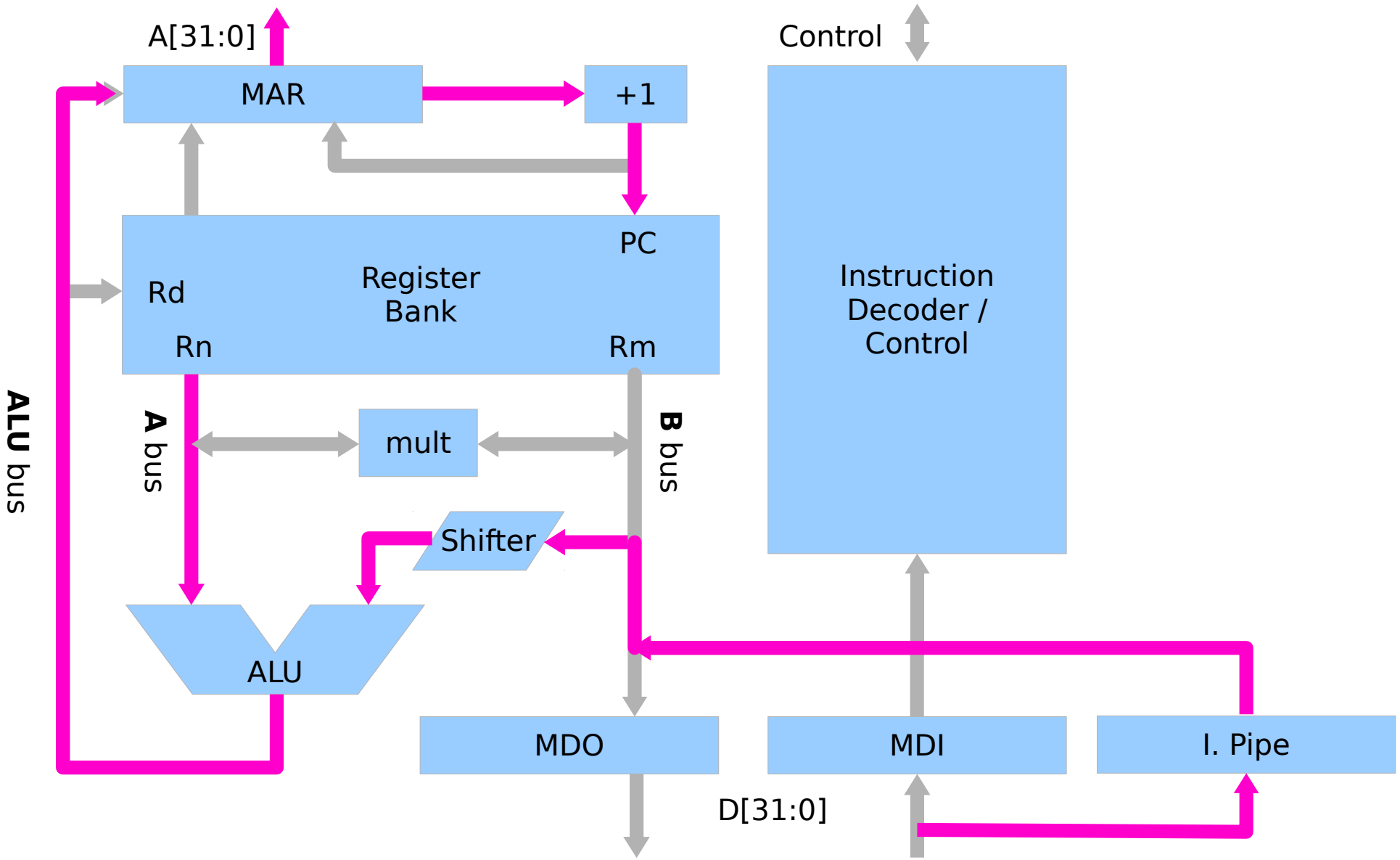
Register-Register Operations



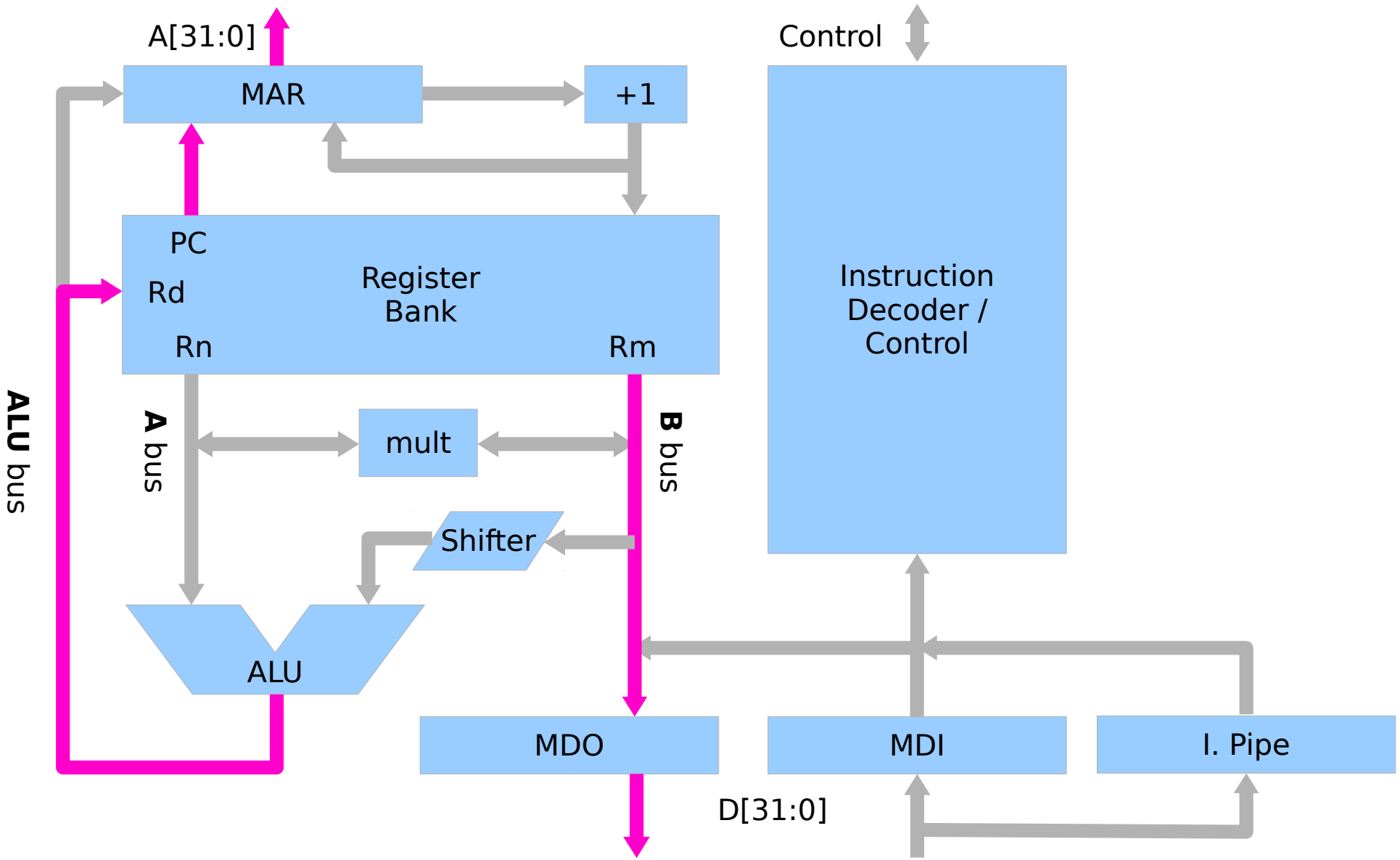
Register-Immediate Operations



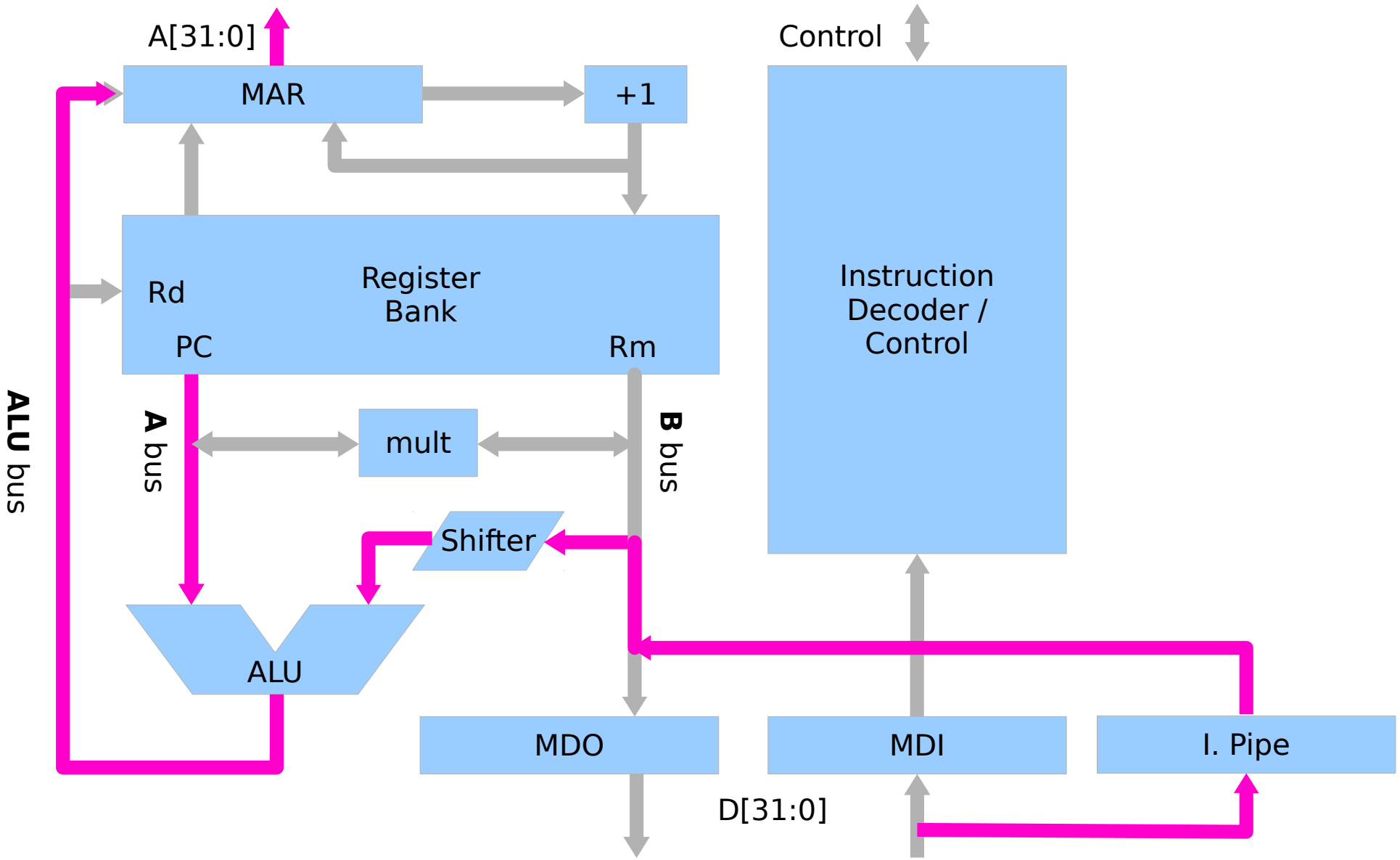
STR - 1st Cycle



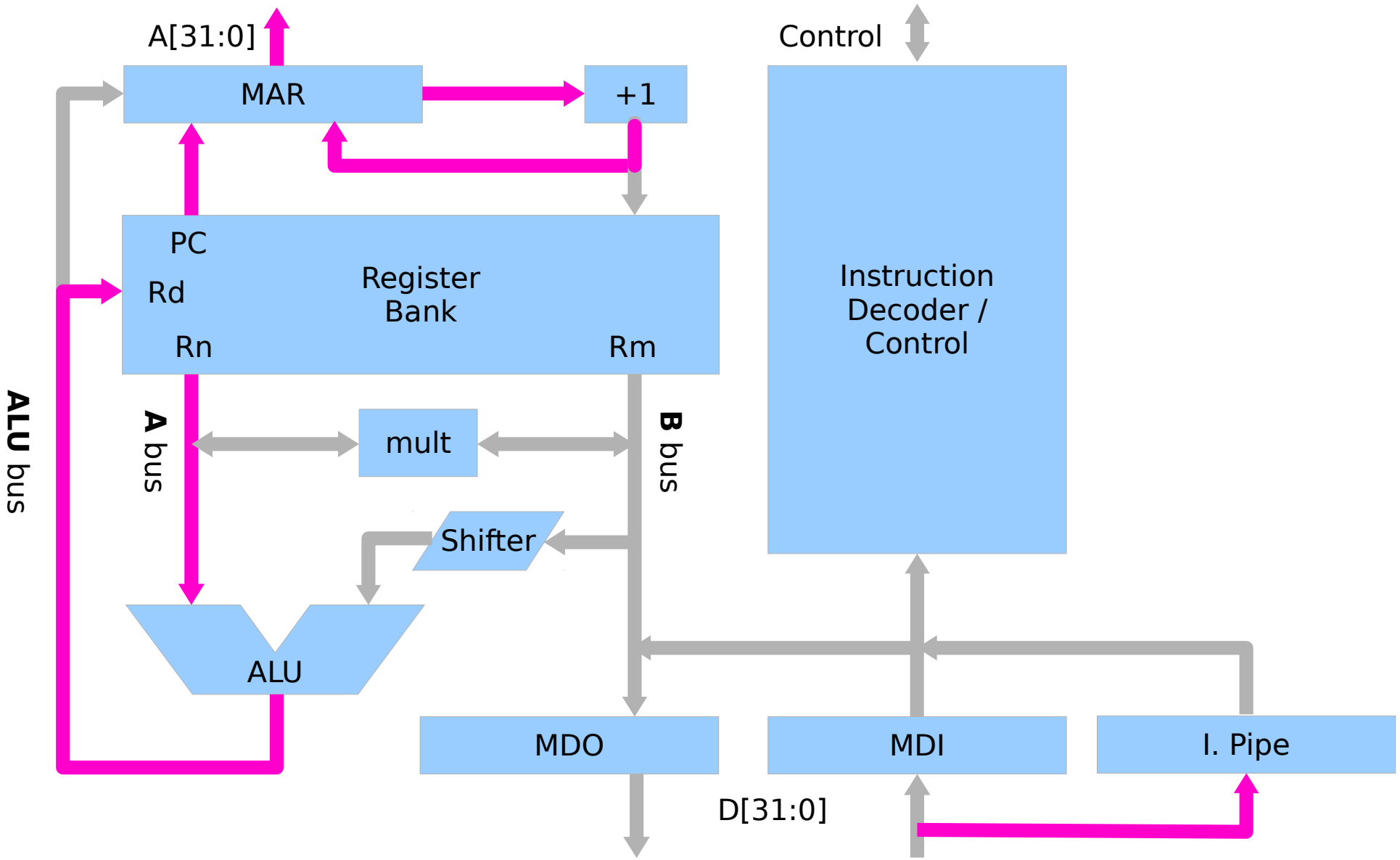
STR - 2nd Cycle



B - 1st Cycle


A[31:0]
MAR
+1
Control
Rd
Register
Bank
PC
Rm
Instruction
Decoder /
Control
ALU bus
A bus
mult
B bus
Shifter
ALU
MDO
MDI
I. Pipe
D[31:0]

B - 2nd Cycle


A[31:0]
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A bus
mult
B bus
Shifter
ALU
MDO
MDI
I. Pipe
D[31:0]

ARM Instruction Set

The load-store architecture

3-address data processing instructions

(2 source registers + 1 destination register)

Conditionally executes every instruction

Multiple data transfer instruction

Single cycle execution of shift and ALU operations

Open instruction set for coprocessors

A very dense 16-bit compressed instruction set (Thumb)

3-stage

fetch

- the instruction is fetched from memory
- it is placed in the instruction pipeline

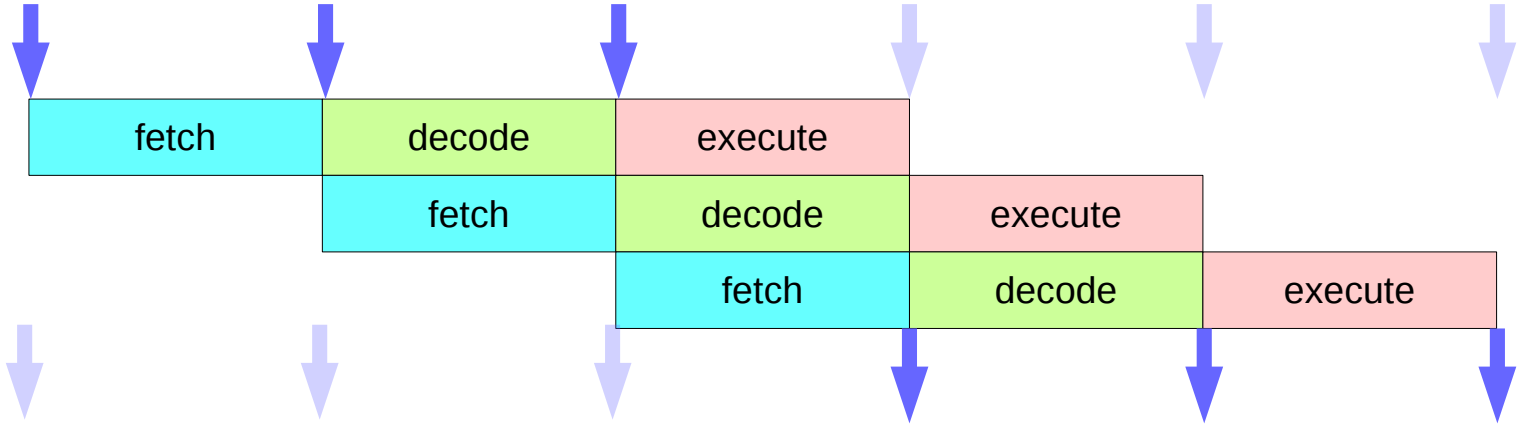
decode

- the instruction is decoded
- next cycle control signal is prepared
- the decode logic but not the datapath is dedicated

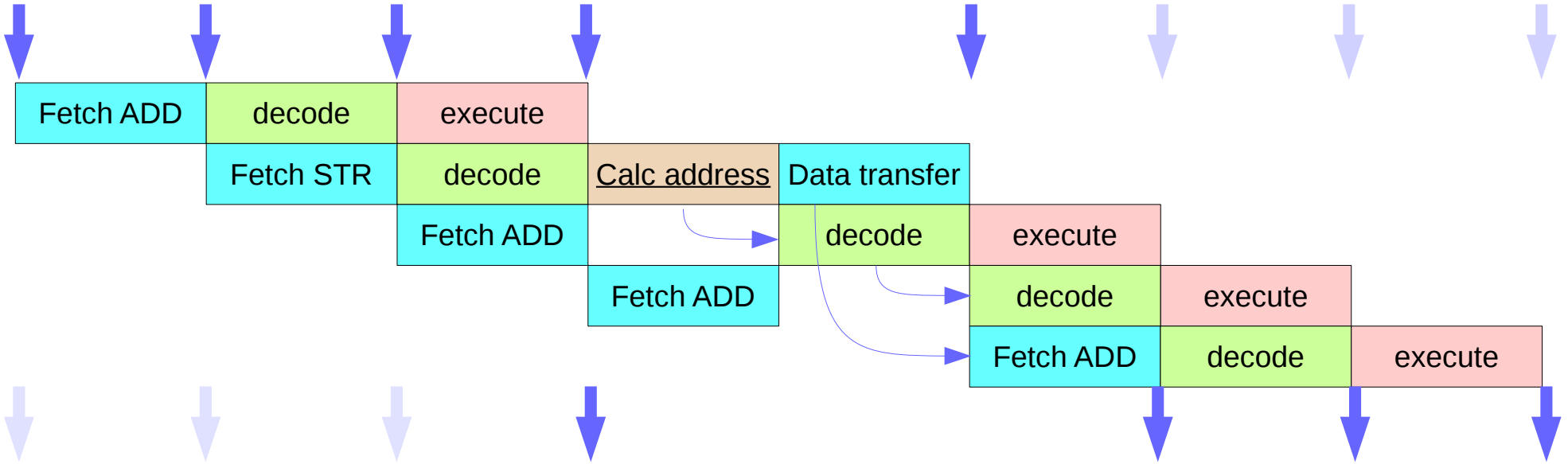
execute

- the datapath is dedicated
  - reading the register bank
  - shifting an operand
  - performing ALU operations
  - writing back the result into the register bank

3 stage pipeline – single cycle



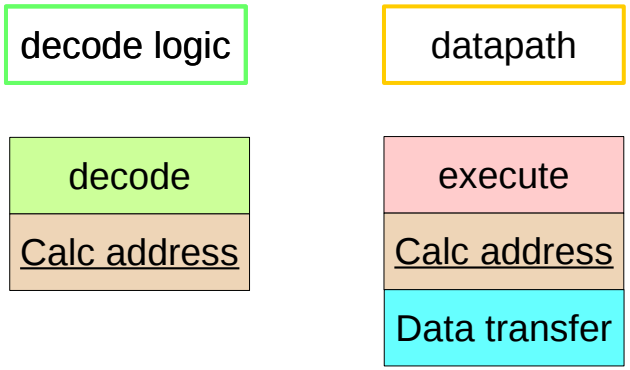
3-stage pipeline – multi-cycle



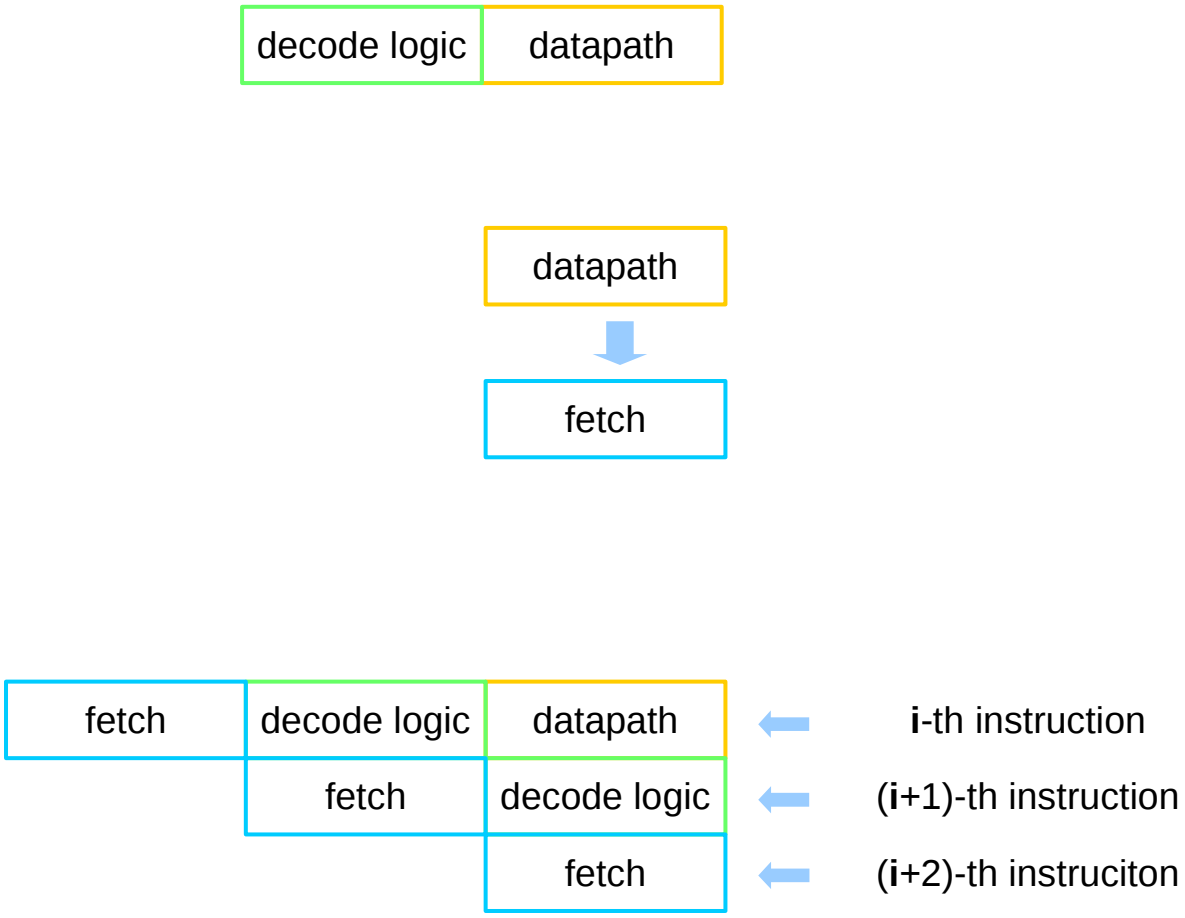
the decode logic is involved in
all the decode cycle
the address calculation

the datapath is involved in
all the execute cycle
the address calculation
the data transfer

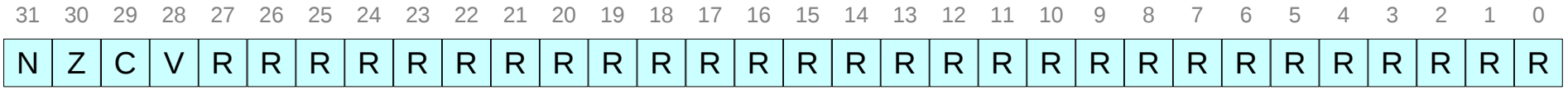
3-stage pipeline – multi-cycle



3-stage pipeline – multi-cycle



ARM Exception Handling



References

[1] ftp://ftp.geoinfo.tuwien.ac.at/navratil/HaskellTutorial.pdf
[2] https://www.umiacs.umd.edu/~hal/docs/daume02yaht.pdf