

CMOS Pass Transistor (H.1)

20151219

Common Gate Mode (Pass Transistor)

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References

Some Figures from the following sites

[1] <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>
Weste & Harris Book Site

[2] en.wikipedia.org

Pass Transistor Configuration

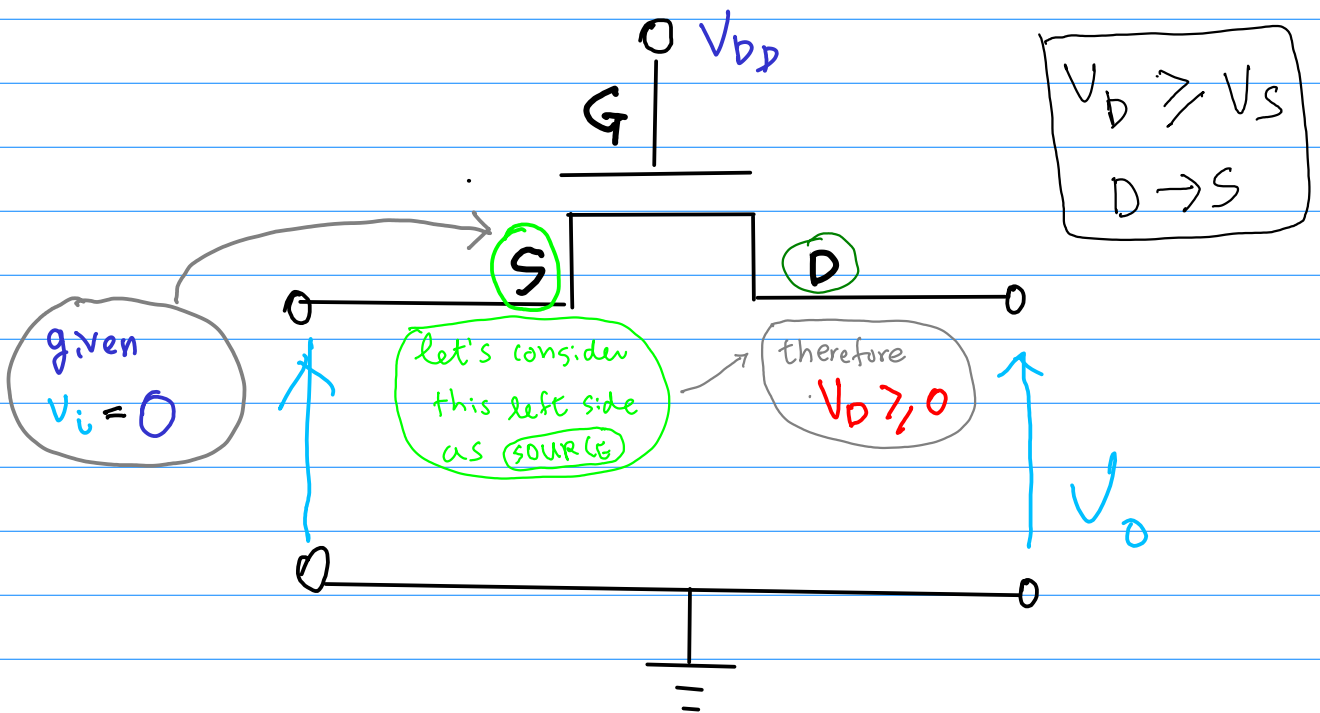
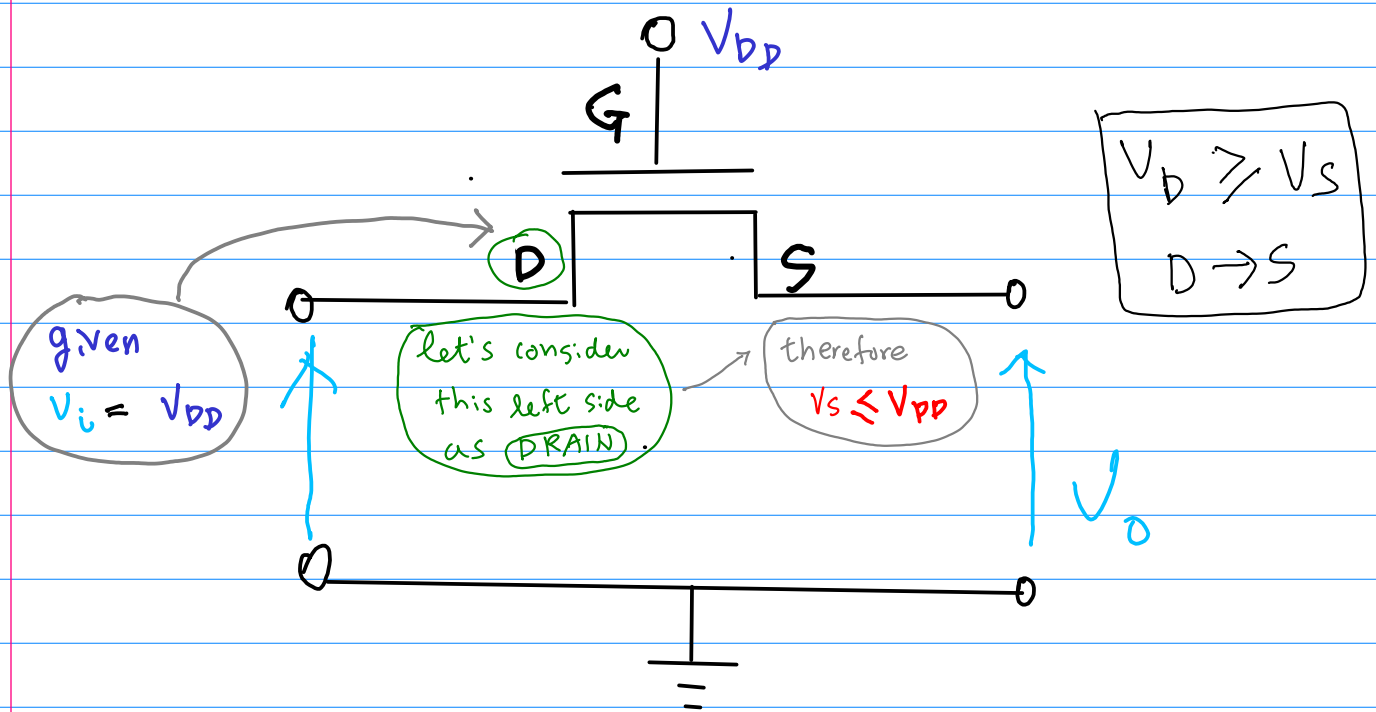
Symmetric (Source & Drain)

n Mos

$I_{ps} (+)$

$D \rightarrow S$

$V_D > V_S$



① Cut off

$$V_{GS} < V_t$$

② Linear

$$\begin{array}{l} S \text{ (shaded)} \text{ D} \\ S \text{ (unshaded)} \text{ D} \end{array} \quad \begin{array}{l} 0 < V_t < V_{GS} \\ 0 < V_t < V_{GD} \end{array} \quad \equiv \quad \begin{array}{l} 0 < V_t < V_{GS} \\ V_{DS} < V_{GS} - V_t \end{array}$$

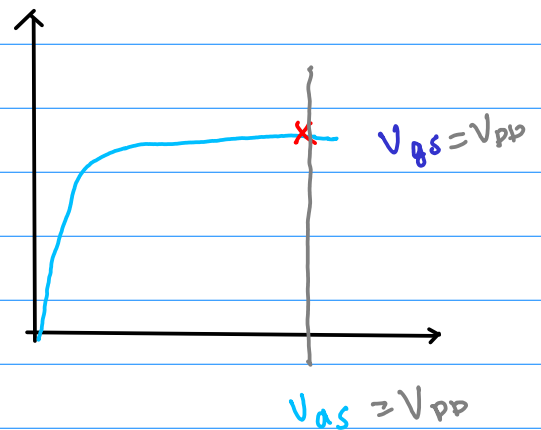
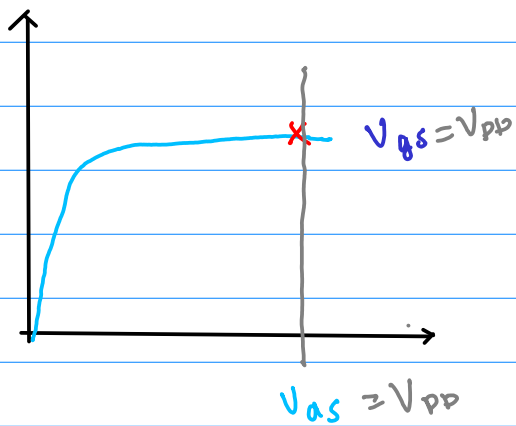
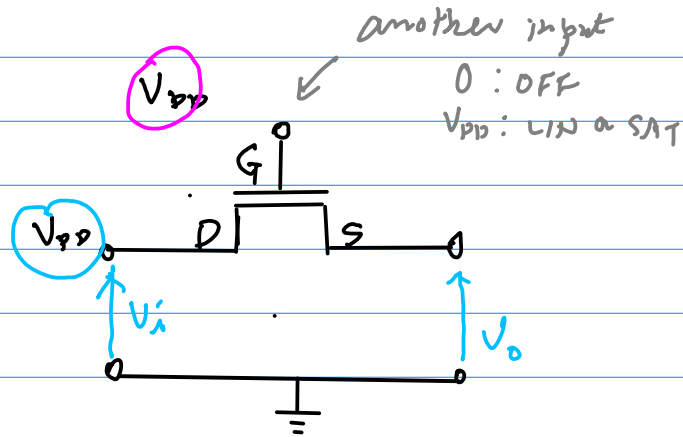
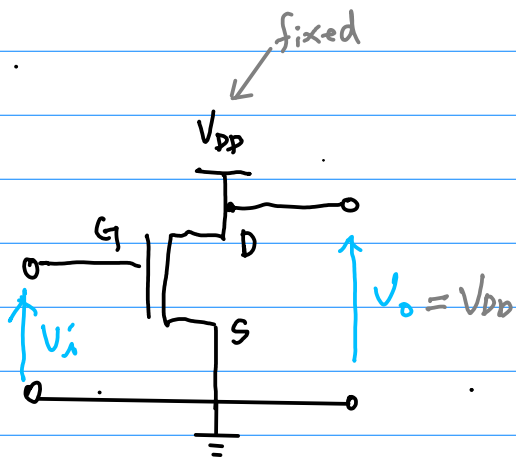
$$V_{GD} = V_{GS} - V_{DS}$$

$$V_{GS} - V_{DS}$$

③ Saturation

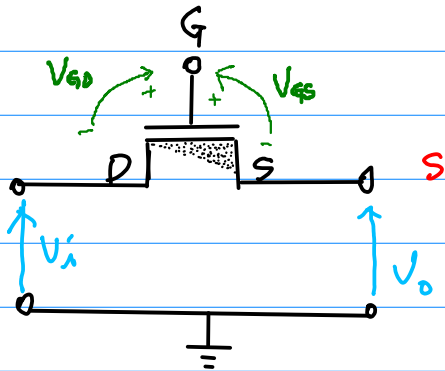
$$\begin{array}{l} S \text{ (shaded)} \text{ D} \\ S \text{ (unshaded)} \text{ D} \end{array} \quad \begin{array}{l} 0 < V_t < V_{GS} \\ V_{GD} < V_t \end{array} \quad \equiv \quad \begin{array}{l} 0 < V_t < V_{GS} \\ V_{GS} - V_t < V_{DS} \end{array}$$

(*) also nMOS pass transistor must be in either SAT or LIN to "pass" v_i to v_o .



$$V_{DS} = V_D - V_S$$

$$= V_{DD} - V_S > V_{th}$$



$$V_{GS} > V_t$$

$$V_{GS} > V_t$$

$$V_{GD} > V_t$$

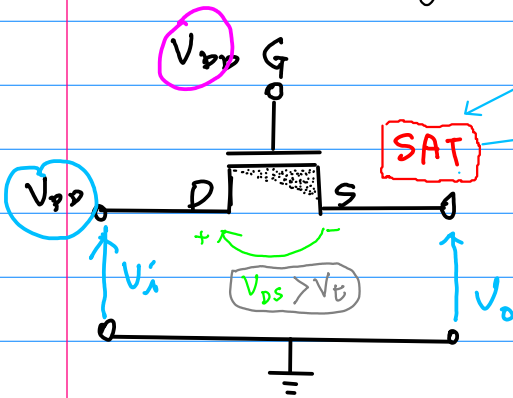
$$V_{GD} < V_t$$

LIN

SAT

$$V_{GD} = V_G - V_D = V_{DD} - V_{DD} = 0$$

$$0 = V_{GD} < V_t$$



$$V_{GS} > V_t$$

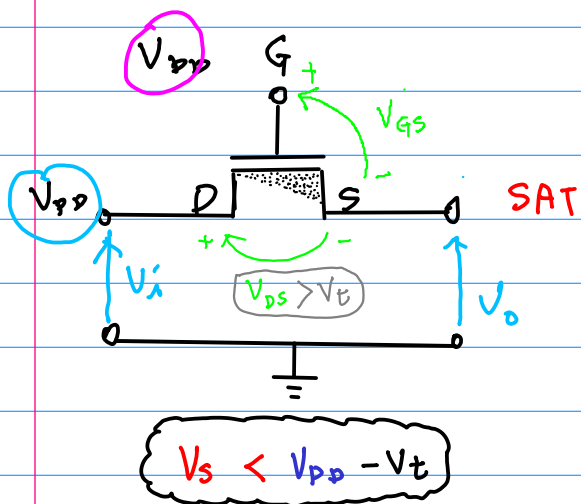
$$V_{GS} = V_G - V_S > V_t$$

$$V_{DD} - V_S > V_t$$

$$V_{DD} - V_t > V_S$$

$$V_S < V_{DD} - V_t$$

Condition: must not turn off



$$\text{SAT} \begin{cases} V_{GS} > V_t \\ V_{DS} > V_{GS} - V_t \end{cases}$$

$V_{GS} = V_G - V_S$ $= V_{DD} - V_S > V_t$
$V_{DS} = V_D - V_S$ $= V_{DD} - V_S > V_t$

$$V_{S,\min} = 0$$

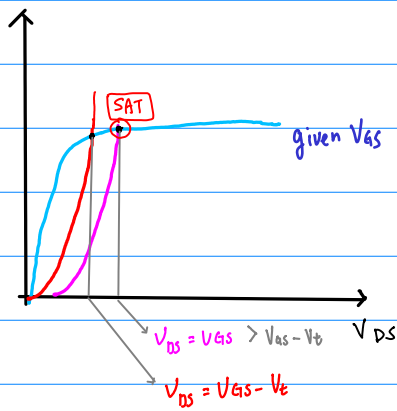
$$V_{S,\max} = V_{DD} - V_t$$

$$V_S \in [0, V_{DD} - V_t]$$

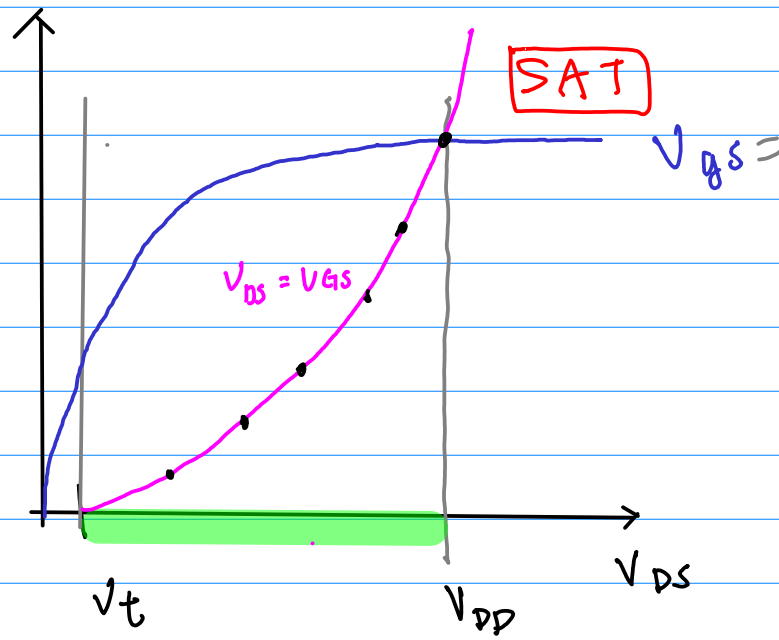
$$V_{DS,\max} = V_{GS,\max} = V_{DD}$$

$$V_{DS,\min} = V_{GS,\min} = V_t$$

$$V_{DS} = V_{GS} \in [V_t, V_{DD}]$$

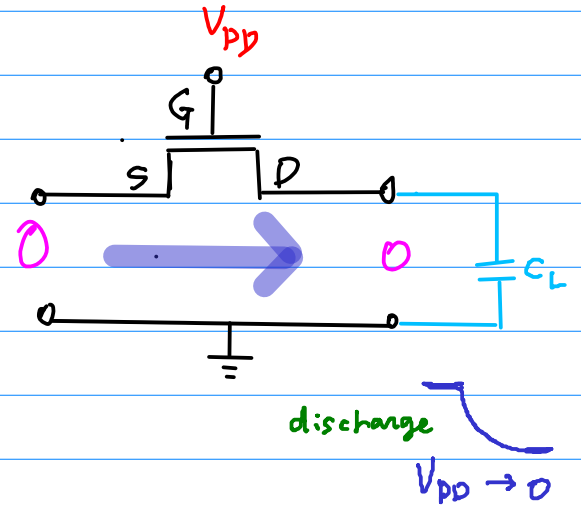
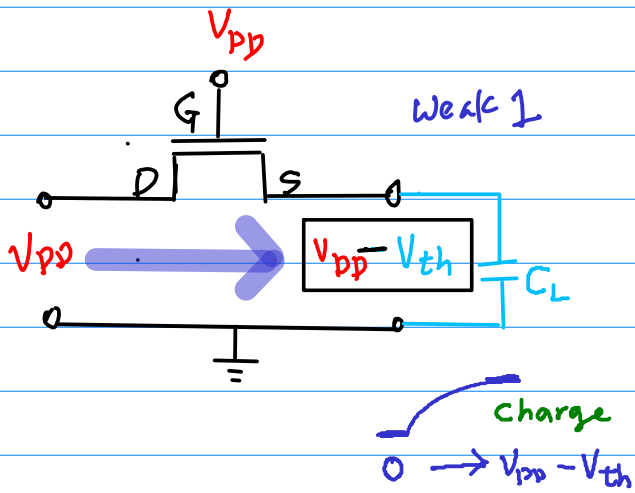


$V_{DS} = V_{GS} > V_{GS} - V_t \iff V_{DS} = V_{GS}$
 $V_{DS} = V_{GS} - V_t \iff V_{DS} > V_{GS} - V_t$

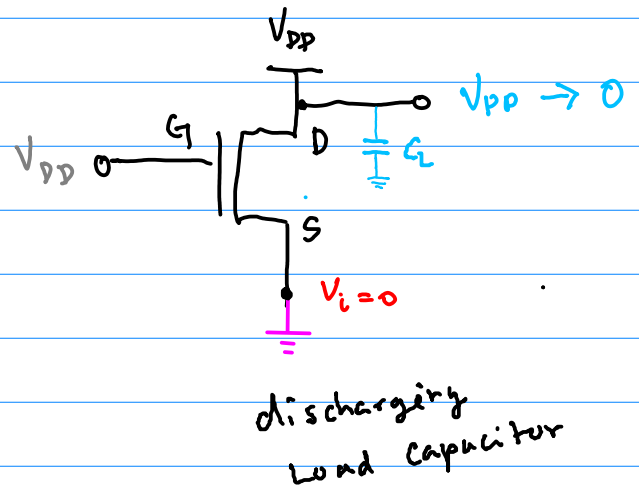
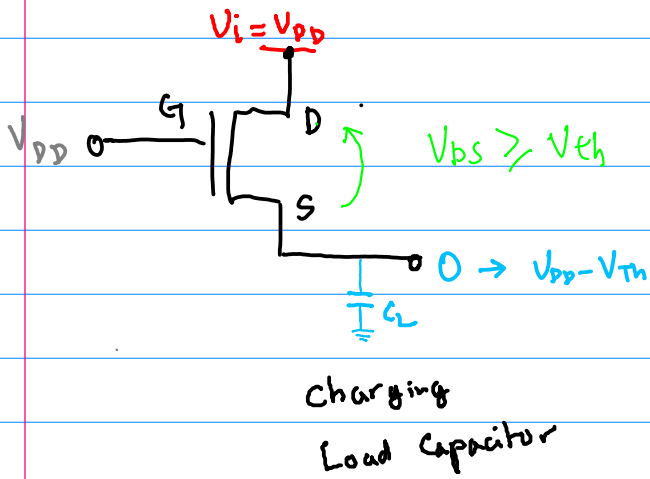


$V_S \in [0, V_{DD} - V_t]$

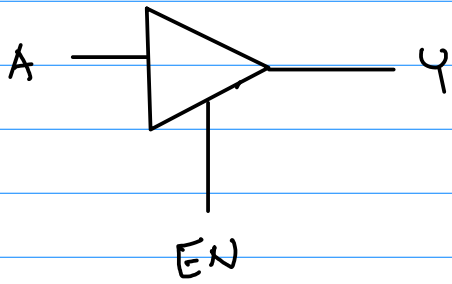
$V_{DS} = V_{GS} \in [V_t, V_{DD}]$



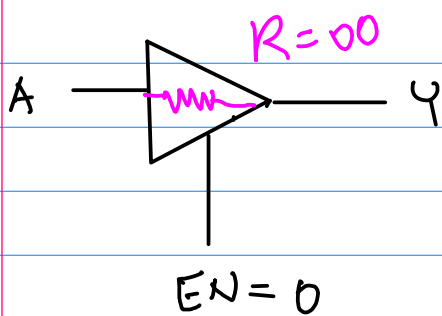
Redraw



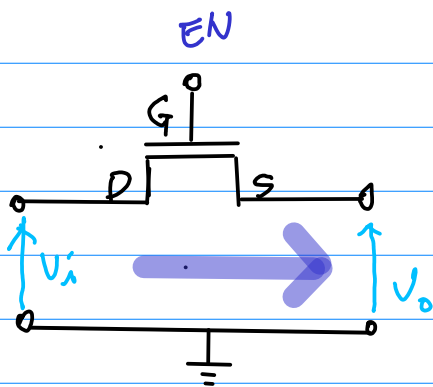
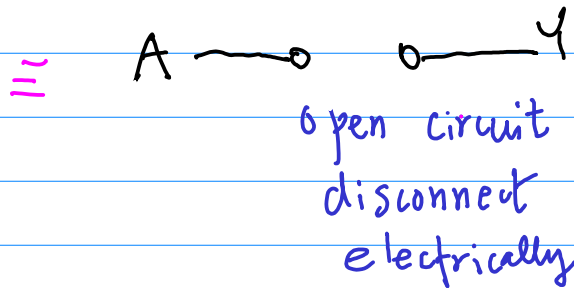
Tristate Buffer



A	EN	Y	
0	0	Z) state
1	0	Z	
0	1	0) state
1	1	1) state

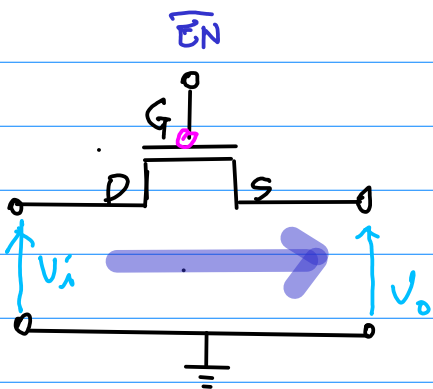


High Impedance Z



nMOS

0 → Strong 0
1 → Weak 1



pMOS

0 → Weak 0
1 → Strong 1

