Virtual Memory & DRAM HW

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Culler, Berkely
http://www-inst.eecs.berkeley.edu/~cs150/fa07/Lectures/lec14-mem-dram.pdf

Basic DRAM Read & Write
DRAM READ Timing
DRAM WRITE Timing

READ Burst (with auto precharge)
WRITE Burst (with auto precharge)

Jacob, ISCA2002
http://www.ece.umd.edu/~blj/talks/DRAM-Tutorial-isca2002.pdf

Basics – Read Timing for Conventional DRAM
DRAM Evolution – Read Timing for Conventional DRAM
DRAM Evolution – Read Timing for Extended Data Out
DRAM Evolution – Read Timing for Burst EDO
DRAM Evolution – Read Timing for Pipeline Burst EDO
DRAM Evolution – Read Timing for Synchronous DRAM

Jacob, ISCA2002
http://www.ece.umd.edu/~blj/talks/DRAM-Tutorial-isca2002.pdf

DRAM Evolution – Read Timing for Burst EDO
DRAM Evolution – Read Timing for Pipeline Burst EDO

> In early generations of DRAM devices such as FPM DRAM devices, the direct control of the internal circuitry of the DRAM device by the external memory controller and the asynchronous nature of the device interface means that the DRAM device could not be well pipelined, and new commands to the DRAM device may not be initiated until the movement of data for the previous command is completed * . The asynchronous nature of the interface means that system design engineers can implement different memory controller that operated at different frequencies, and designers of the memory controller are solely responsible to ensure that the controller can correctly control different DRAM devices from different DRAM device and module manufacturers, possibly with subtle timing variations.
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> * For every rule, there are exceptions to the rule. **Pipeline burst EDO** devices were designed to have some limited pipelining capability with an implicit clocking scheme.
>
> From Wang's PhD dissertation
> http://www.ece.umd.edu/~blj/papers/thesis-PhD-wang--DRAM.pdf

Memory Controller : Synchronous FSM
Burst EDO : aysnchronous FSM inside, difficult to pipeline access
Pipeline Burst EDO : some modification to the async FSM inside, to enable easy pipeline access

Koopman, CMU
https://www.ece.cmu.edu/~ece548/handouts/05vmarch.pdf

1-Level Page Table Example
2-Level Page Table Example

Harris, Computer Architecutre
http://booksite.elsevier.com/9780123944245/

Page Table Example

References

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[8] Digital Systems, Hill, Peterson, 1987