

# Min Max Timing

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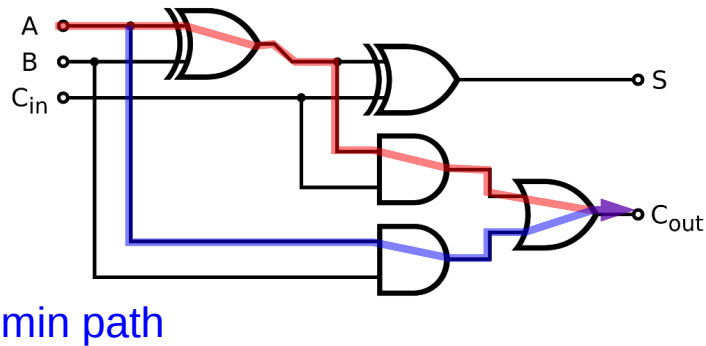
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# Max Path / Min Path

Max path



Max delay

min delay

min path

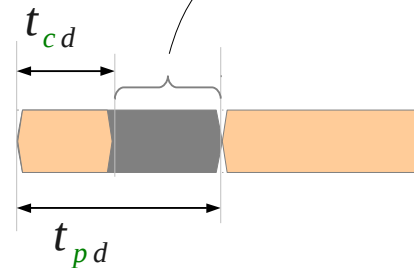
$$t_{cd} \leq t_{delay} \leq t_{pd}$$

min delay

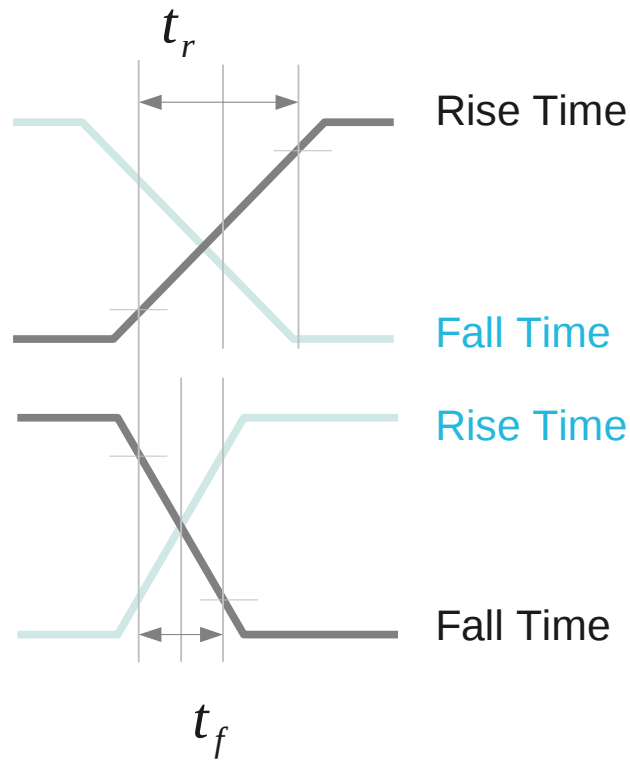
Max delay



the output is changing

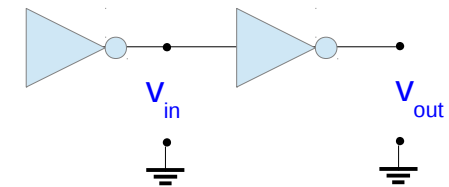
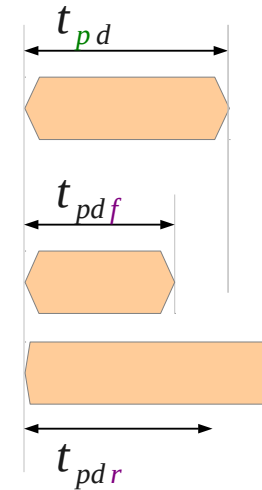


# Rise / Fall Times



Max delay

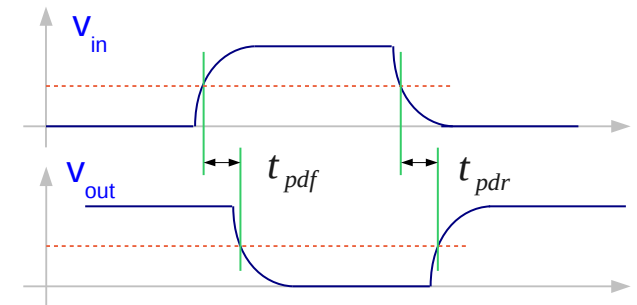
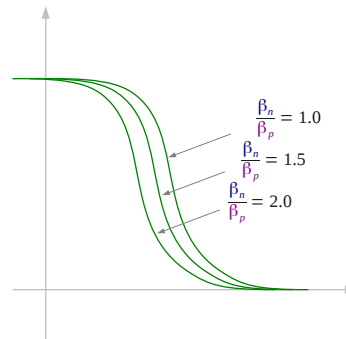
min delay



$$\frac{t_f}{t_r} = \frac{2.2\tau_n}{2.2\tau_p}$$

$$\frac{\beta_n}{\beta_p} > 1 \quad \frac{R_n}{R_p} < 1$$

$$\frac{\tau_n}{\tau_p} = \frac{R_n C_{out}}{R_p C_{out}} = \frac{R_n}{R_p} < 1$$



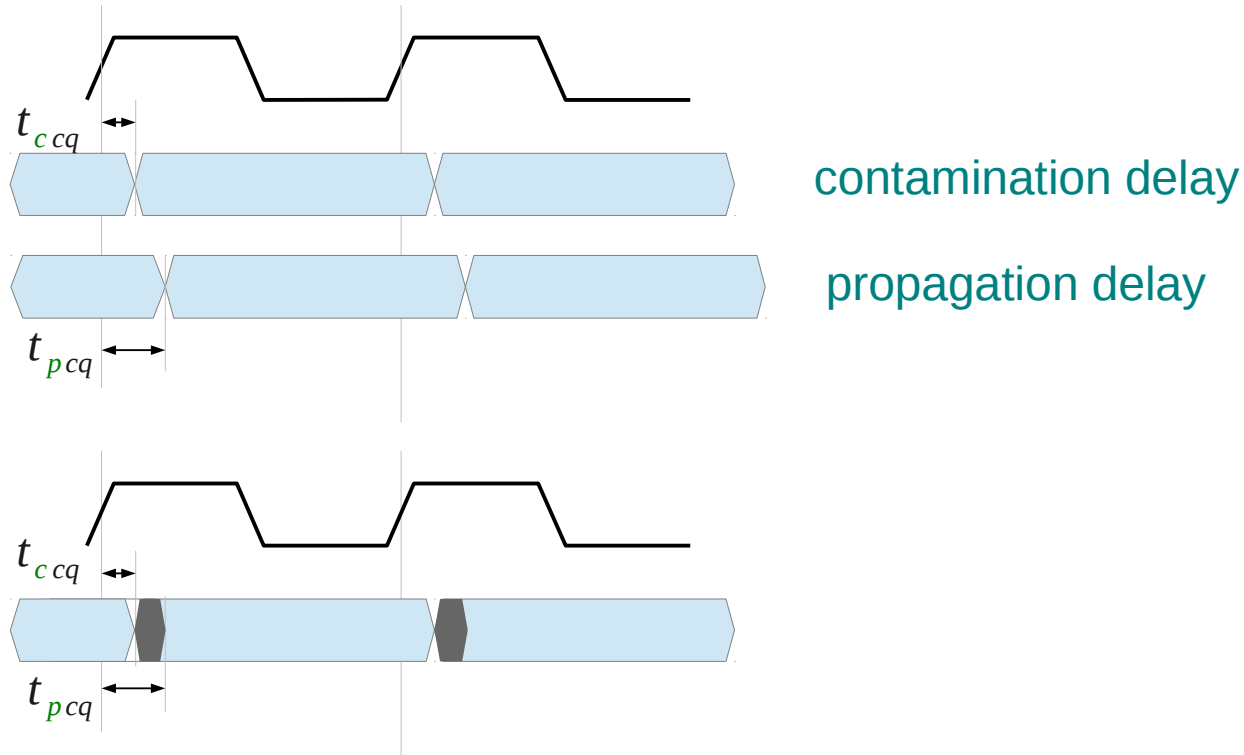
# PVT Variation

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{ Process  
Voltage  
Temperature

High temperature    **Max delay**  
Low temperature    **min delay**

# FF Output Delay



contamination delay

propagation delay

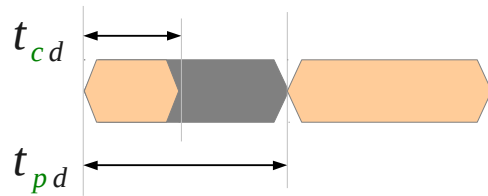
flipflop clock-to-q

$$t_{ccq} \leq t_{delay} \leq t_{pcq}$$

min delay

Max delay

# Path Delay



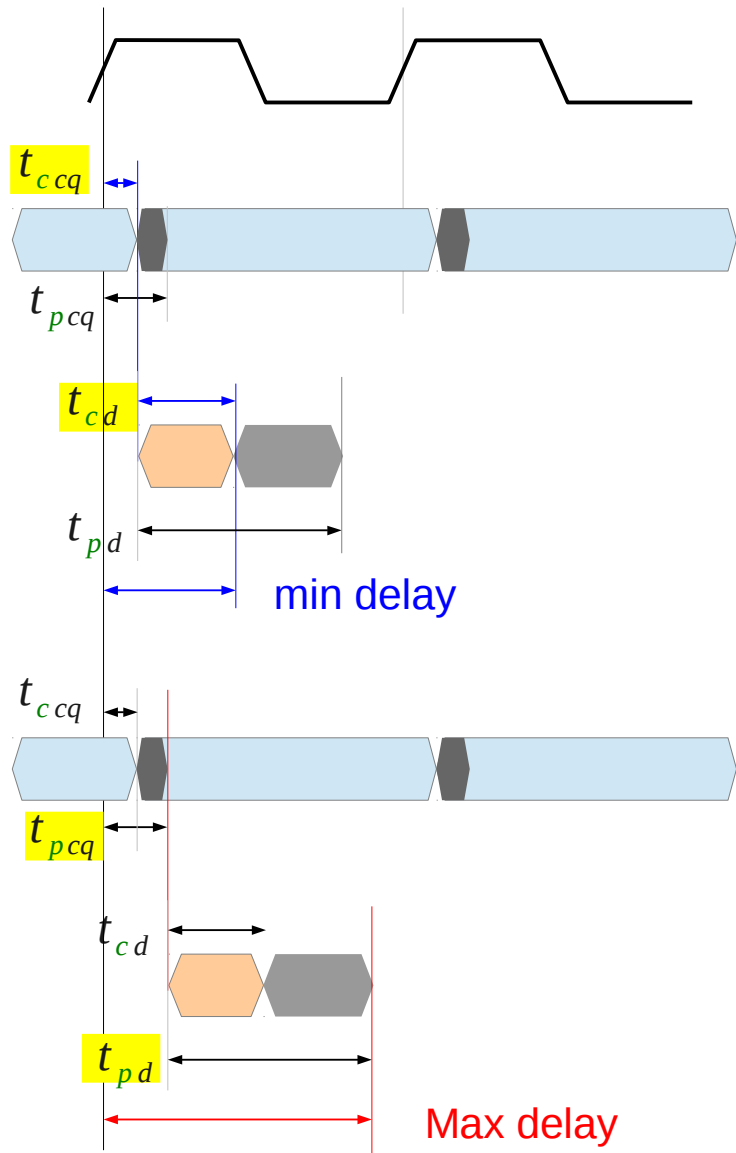
combinational logic delay

$$t_{cd} \leq t_{delay} \leq t_{pd}$$

min delay

Max delay

# Reg-to-Reg Delay (1)



$$t_{ccq} \leq t_{FF} \leq t_{pcq}$$

min delay

Max delay

$$t_{cd} \leq t_{comb} \leq t_{pd}$$

min delay

Max delay

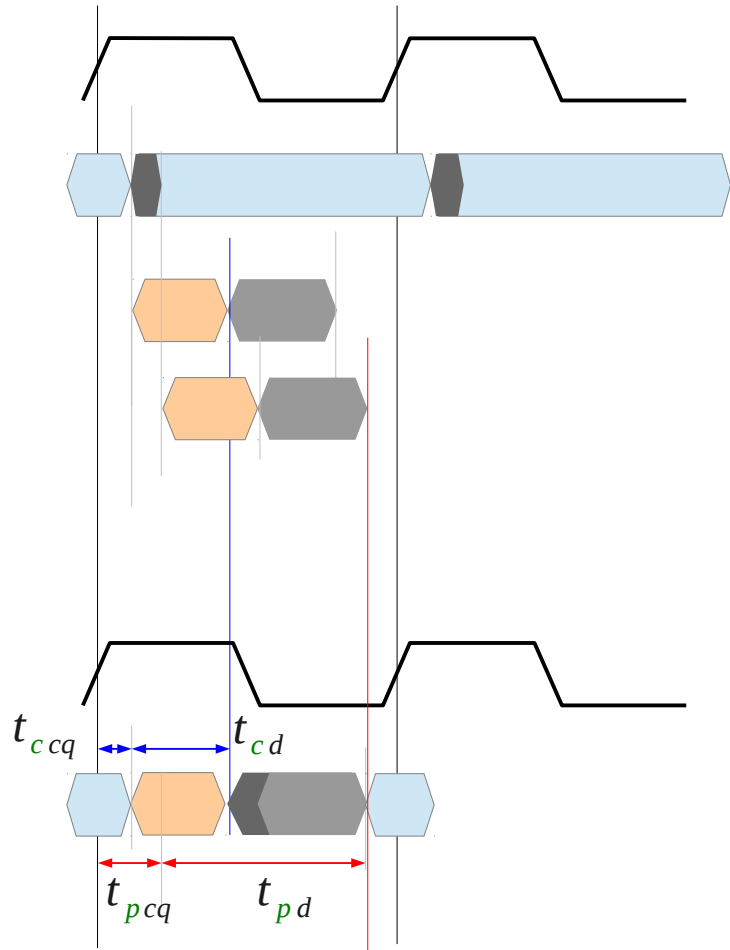
$$t_{ccq} + t_{cd} \leq t_{delay} \leq t_{pcq} + t_{pd}$$

min delay

Max delay



# Reg-to-Reg Delay (2)



$$t_{cq} \leq t_{FF} \leq t_{pcq}$$

min delay

Max delay

$$t_{cd} \leq t_{comb} \leq t_{pd}$$

min delay

Max delay

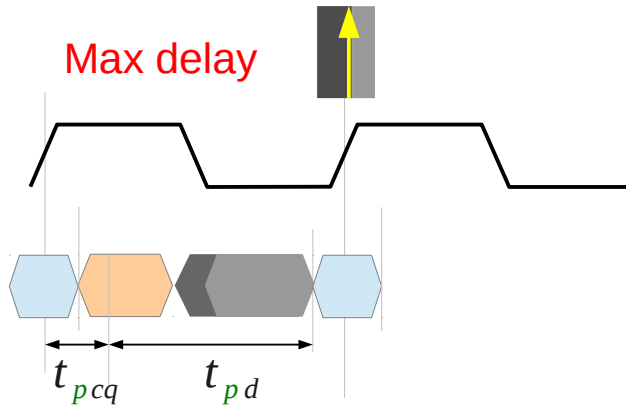
$$t_{cq} + t_{cd} \leq t_{delay} \leq t_{pcq} + t_{pd}$$

min delay

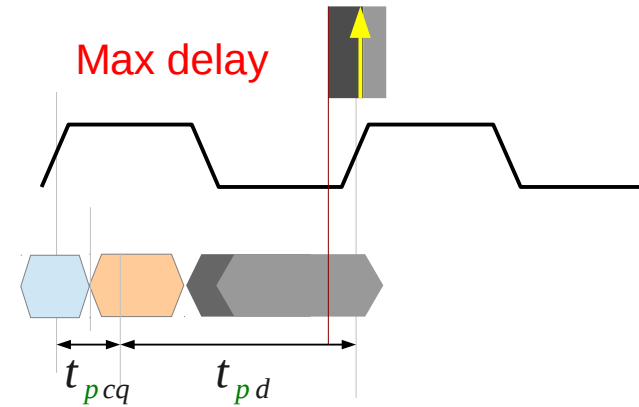
Max delay

# Setup Time / Hold Time

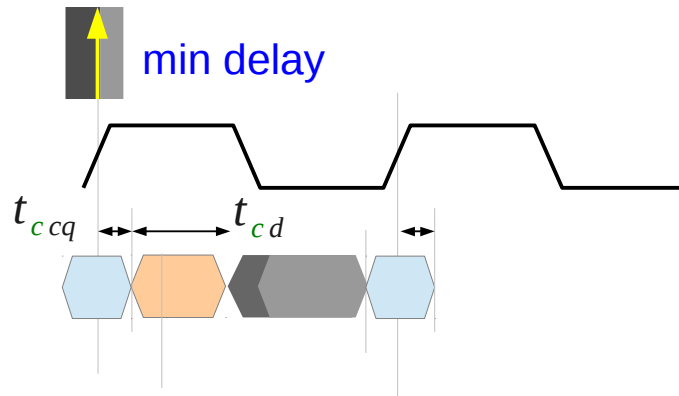
## Setup Time OK



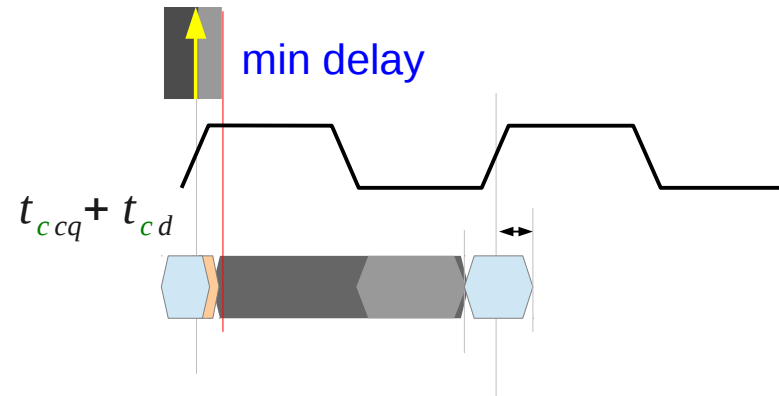
## Setup Time Violation



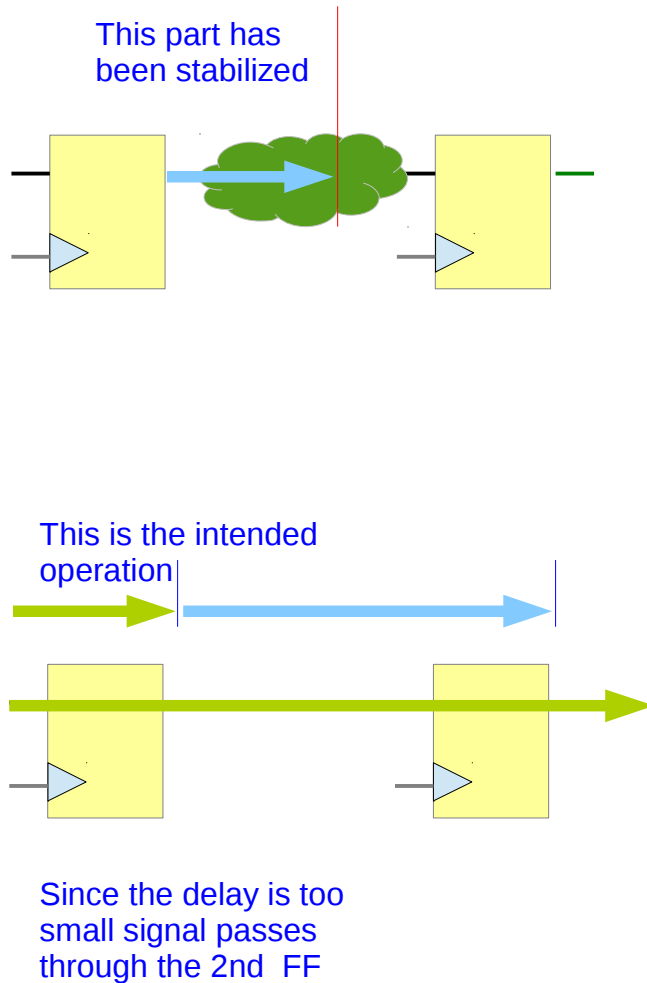
## Hold Time OK



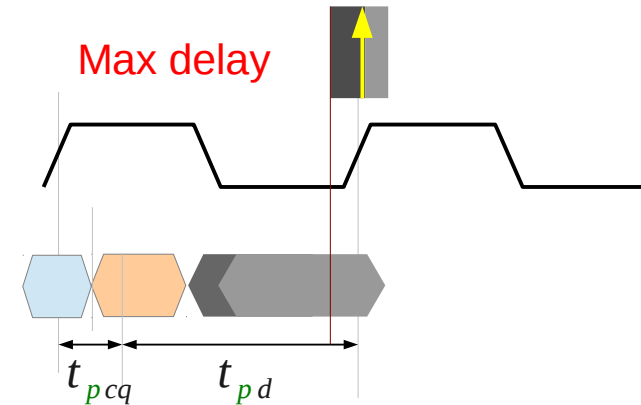
## Hold Time Violation



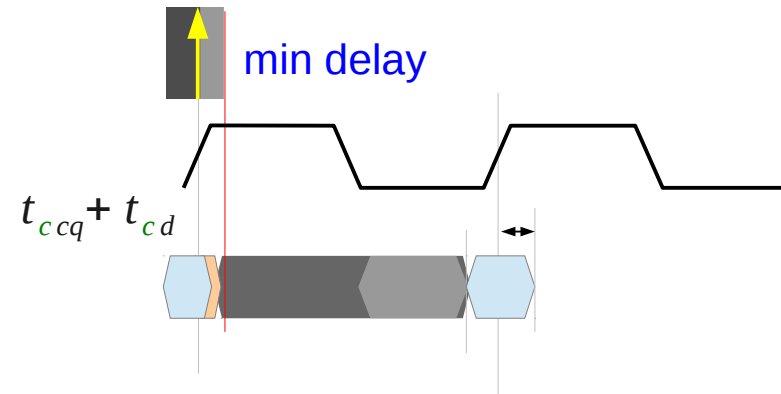
# Setup Time / Hold Time



## Setup Time Violation



## Hold Time Violation



# Resolution Time

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## References

- [1] <http://en.wikipedia.org/>
- [2] M. M. Mano, C. R. Kime, "Logic and Computer Design Fundamentals", 4<sup>th</sup> ed.
- [3] J. Stephenson, Understanding Metastability in FPGAs. Altera Corporation white paper. July 2009.